Greetings from the CSE Chair

Dear CSE Students,

Our Department of Computer Science and Engineering celebrated its 40th anniversary this semester by inviting our alumni to tour our labs and a dinner at Apogee Stadium. As you, our current students, graduate from our program, we hope you will continue your ties with our CSE Department, just like these alumni have done in coming back to celebrate 40 years. Alumni support is very important for the success of our department.

I want to share the news of many of our research groups in our CSE Department. We have a new NSF grant to support PhD students in our Center for Information and Computer Security. The Language and Information Technologies group is growing with the addition of Dr. Rodney Nielsen. Dr. Krishna Kavi’s Net-Centric Software and Systems Industry/University Cooperative Research Center is also growing and
Dr. Ram Dantu's research featured on NSF website

The National Science Foundation has featured CSE Professor Dr. Ram Dantu’s "Mobile Life Guard" on the front page of its website. Dr. Dantu and his team created this app that keeps drivers focused and safe on the roads. A year ago, Dr. Dantu was among the first group of scientists to receive a $50,000 National Science Foundation Innovation Corps (I-Corps) award which help scientists and engineers extend their focus beyond the laboratory into the commercial award. The safe driving app is a result of this work.

The app is not commercially available yet but it is currently undergoing a field trial with the insurance industry. If it is successful, safe drivers could receive safe driver discounts. Dr. Dantu says, "Insurance companies see it as an investment in lowering their costs long term."

For more information, see this NSF article.

Professor Mohanty Publishes a Book on Memory Design

Professor Saraju P. Mohanty recently published a book titled "Robust SRAM Designs and Analysis". This book provides a guide to Static Random Access Memory (SRAM) bitcell design and analysis to meet the nano-regime challenges for CMOS devices. In addition, emerging devices, such as Tunnel FETs are discussed in detail for their applicability for memory design.

Discussions are included to cover nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis. Emphasis is placed throughout the book on the various trade-offs for achieving a best SRAM design. The book discusses in detail the most important SRAM bitcell topologies to mitigate nanoscale process variations, as process variations is an ongoing challenge in memory design.

The following are key features of the book:

- It provides a complete introduction to SRAM bitcell design and analysis.
- It presents techniques to face nano-regime challenges such as process variation, leakage, and NBTI for SRAM design and analysis.
- It discusses simulation set-ups for extracting different design metrics for CMOS technology and emerging technology devices.
- It emphasizes different trade-offs for achieving the best possible SRAM design.