

# **ILP Models for Energy and Transient Power Minimization During Behavioral Synthesis**

**Saraju P. Mohanty, N. Ranganathan and S. K. Chappidi**

Dept. of Computer Science and Engineering

University of South Florida

**{smohanty, ranganat, chappidi}@csee.usf.edu**

# Outline of the Presentation

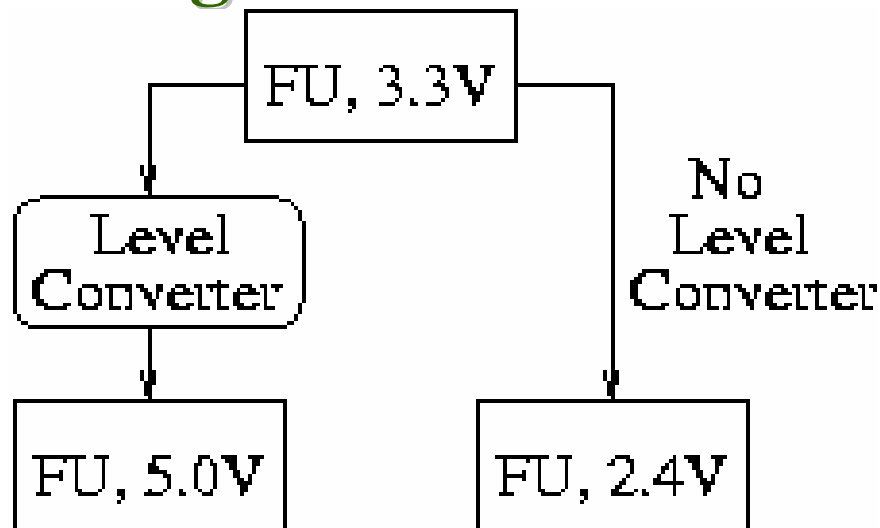
- Introduction
- Related Works
- Target Architecture
- Proposed Datapath Scheduling Scheme
- Conclusions

# Peak Power Reduction at Behavioral Level

Proposed Work	Synthesis Tasks Performed	Methods Used	Time Complexity	% Power Reduction
Martin and Knight [41, 44]	Scheduling Assignment	Genetic Algorithms	NA	40.3-60.0
Shiue and et. al. [119, 120, 121, 108]	Scheduling	ILP Force Directed	Exponential $O(cn^3)$	50.0 – 75.0
Raghunathan, and et. al. [47]	Scheduling	Data Monitor Operations	NA	17.42-32.46

- Do not handle multiple voltage based design
- High time penalty
- Do not minimize other forms of power.

# Target Architecture



- ❑ Level converters are used when a low-voltage functional unit is driving a high-voltage functional unit.
- ❑ Each functional unit has one register and one multiplexer.
- ❑ The register and the multiplexor operate at the same voltage level as that of the functional units.
- ❑ Operational delay of a FU :  $(d_{FU} + d_{Mux} + d_{Reg} + d_{Conv})$ .
- ❑ Time for voltage conversion equals to time for frequency change.
- ❑ Controller has a storage unit to store the cycle frequency index ( $cfi_c$ ).
- ❑ Datapath is represented as a sequencing DFG.
- ❑ Operating frequencies are calculated from the delays.

# Different Power and Energy Parameters

Aim at simultaneous minimization of:

- Average Power
- Peak power
- Cycle difference power
- Peak power differential
- Total Energy

**NOTE:** The peak power, the cycle difference power, and the peak power differential drive the **transient** characteristic of a CMOS circuit.

# Power Definitions

- **Cycle Power ( $P_c$ ):** power consumption of any control step.
- **Peak Power ( $P_{peak}$ ):** maximum power consumption of any control step i.e. maximum ( $P_c$ ).
- **Mean Cycle Power ( $P$ ):** mean of the cycle powers (an estimate for the average power consumption of a DFG).
- **Cycle Difference Power ( $DP_c$ ):** quantifies variation of power consumption of a cycle  $c$  from the mean /average power consumption. This determines the power profile of a DFG over all the control steps.
- **Peak power differential ( $DP_{peak}$ ):** the maximum of the cycle difference power for any control step.
- **Mean Cycle Difference Power ( $DP$ ):** mean of the cycle difference powers (a measure of overall power fluctuation)

# Cycle Power Function Minimization

- **We Define:** A new parameter called “cycle power function” (CPF) as an equally weighted sum of the normalized mean cycle power and the normalized mean cycle difference power.
- **We claim:** The minimization of CPF using multiple supply voltages and dynamic frequency clocking (MVDFC), under resource constraints will lead to the reduction of energy and all different forms of power.

## CPF-DFC Model as Proposed in [4]

□ Cycle power function is defined as :

$$\text{CPF-DFC} = P_{\text{norm}} + DP_{\text{norm}} \quad (1)$$

□ In terms of peak cycle power and peak cycle difference power,

$$\text{CPF-DFC} = \frac{\frac{1}{N} \sum_{c=1}^N P_c}{P_{\text{peak}}} + \frac{\frac{1}{N} \sum_{c=1}^N |P - P_c|}{DP_{\text{peak}}} \quad (2)$$

□ Using the switching capacitance, voltage and frequency,

$$\text{CPF} = \frac{\frac{1}{N} \sum_{c=1}^N \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c}{\max \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right)_{V_c}} + \frac{\frac{1}{N} \sum_{c=1}^N \left( \left| \frac{1}{N} \sum_{c=1}^N \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right) - \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right| \right)}{\max \left( \left| \frac{1}{N} \sum_{c=1}^N \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right) - \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right| \right)_{V_c}}$$



## CPF-DFC Minimization

- **Aim:** to provide ILP-based minimization for the CPF-DFC defined in [4].
- **Observations** about CPF-DFC:
  - CPF-DFC is a *non-linear* function.
  - A function of four parameters, such as,  $P$ ,  $P_{\text{peak}}$ ,  $DP$  and  $DP_{\text{peak}}$ .
  - The absolute function in the numerator contributes to the nonlinearity.
  - The complex behavior of the function is also contributed by the two different denominator parameters,  $P_{\text{peak}}$  and  $DP_{\text{peak}}$ .
- Non-linear programming may be more suitable, but will be large space and time complexity. We are addressing linear programming of the non-linear function.

# CPF-DFC Minimization

## (Linear Modeling of Nonlinearity)

- The objective function CPF-DFC has both types of nonlinearities.
- **In case of a fraction:** remove the denominator and introduce as constraints.
- **In case of absolute:** change difference in objective function to sum and introduce the difference as constraints.

## CPF-DFC\* Minimization (Modified Cycle Power Function)

- The CPF-DFC has two different denominators which may lead to increase in number of constraints and hence the overall solution space.
- We assume that  $|P-P_c|$  is upper bounded by  $P_c$  for all  $c$ , since  $|P-P_c|$  is a measure of the mean difference error of  $P_c$ . So, instead of normalizing DP with  $DP_{peak}$ , we will normalize it with  $P_{peak}$ . This reduces the number of denominator to one.
- We have the following Modified Cycle Power Function which is the objective function for the ILP formulation.

$$\begin{aligned}
 CPF-DFC^* &= \frac{P + DP}{P_{peak}} = \frac{\frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c|}{P_{peak}} \\
 &= \frac{\frac{1}{N} \sum_{c=1}^N \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c}{\max \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right)_{\forall c}} + \frac{\frac{1}{N} \sum_{c=1}^N \left( \left| \frac{1}{N} \sum_{c=1}^N \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right) - \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right| \right)}{\max \left( \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \right)_{\forall c}}
 \end{aligned}$$

# ILP Formulation: Notations used

- $M_{k,v}$  : maximum number of functional units of type  $F_{k,v}$
- $S_i$  : as soon as possible time stamp for the operation  $o_i$
- $E_i$  : as late as possible time stamp for the operation  $o_i$
- $P(C_{swi}, v, f)$  : power consumption of any  $F_{k,v}$  used by operation  $o_i$
- $x_{i,c,v,f}$  : decision variable, which takes the value of 1 if operation  $o_i$  is scheduled in control step  $c$  using  $F_{k,v}$  and  $c$  has frequency  $f$
- $y_{i,v,l,m}$  : decision variable which takes the value of 1 if operation  $o_i$  is using the functional unit  $F_{k,v}$  and scheduled in control steps  $l \rightarrow m$
- $L_{i,v}$  : latency for operation  $o_i$  using resource operating at voltage  $v$  (in terms of number of clock cycles)

**NOTE:** The effective switching capacitance is a function of the average switching activity at the input operands of a functional unit and  $C_{swi}$  is a measure of effective switching capacitance  $FU_i$ .

$$\alpha_i C_i = C_{swi}(\alpha_i^1, \alpha_i^2)$$

# CPF-DFC\* Minimization: ILP Formulation

•**Objective Function:** Minimize the CPF-DFC\* for the whole DFG over all the control steps. Using the previous expressions we have,

$$\text{Minimize : } \frac{\frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c|}{P_{peak}} \quad (1)$$

The denominator is removed and introduced as a constraint.

$$\begin{aligned} \text{Minimize : } & \frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c| \\ \text{Subject to : } & \text{Peak power constraints} \end{aligned} \quad (2)$$

The absolute is replaced with sum and the appropriate constraints.

$$\begin{aligned} \text{Minimize : } & \frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N (P + P_c) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (3)$$

After simplification,

$$\begin{aligned} \text{Minimize : } & \left( \frac{3}{N} \right) \sum_{c=1}^N P_c \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (4)$$

Using decision variables,

$$\begin{aligned} \text{Minimize : } & \sum_c \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * \left( \frac{3}{N} \right) * P(C_{swi,v}, f) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (5)$$

# CPF-DFC\* Minimization: ILP Formulation

❖ **Uniqueness Constraints** : ensure that every operation  $o_i$  is scheduled to one unique control step and represented as,

$$\forall i, 1 \leq i \leq O, \sum_c \sum_v \sum_f x_{i,c,v,f} = 1$$

❖ **Precedence Constraints** : guarantee that for an operation  $o_i$ , all its predecessors are scheduled in an earlier control step and its successors are scheduled in an later control step and are;  $\forall i,j, o_i$  belong to  $\text{Pred}(o_j)$ ,  $\sum_v \sum_f \sum_{\{d=S_i \rightarrow E_j\}} dx_{i,c,v,f} - \sum_v \sum_f \sum_{\{d=S_j \rightarrow E_j\}} ex_{j,c,v,f} \leq -1$

❖ **Resource Constraints** : make sure that no control step contains more than  $F_{k,v}$  operations of type  $k$  operating at voltage  $v$  and are enforced as,  $\forall c, 1 \leq c \leq N$  and  $\forall v, \sum_{\{i \in F_{k,v}\}} \sum_f x_{i,c,v,f} \leq M_{k,v}$

❖ **Frequency Constraints** : lower operating voltage functional unit can not be scheduled in a higher frequency control step; these constraints are expressed as,

$$\forall i, 1 \leq i \leq O, \forall c, 1 \leq c \leq N, \text{ if } f < v, \text{ then } x_{i,c,v,f} = 0.$$

# CPF-DFC\* Minimization: ILP Formulation

- **Peak Power Constraints** : introduced to eliminate the fractional non-linearity of the objective function and are enforced as, for all  $c$ ,  $1 \leq c \leq N$ ,

$$\sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) \leq P_{peak}$$

- **Modified Peak Power Constraints** : To eliminate the non-linearity introduced due to the absolute function introduced as, for all  $c$ ,  $1 \leq c \leq N$ ,

$$\frac{1}{N} \sum_c \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) - \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) \leq P_{peak}^*$$

**NOTE:** The unknowns  $P_{peak}$  and  $P_{peak}^*$  is added to the objective function and minimized alongwith it.

## **CPF-DFC\* Minimization: Scheduling Algorithm**

- Step 1:** Construct a look up table for (effective switching capacitance, average switching activity) pairs.
- Step 2:** Calculate the switching activities at the inputs of each node through behavioral simulation of the DFG.
- Step 3:** Find ASAP schedule for the UDFG.
- Step 4:** Find ALAP schedule for the UDFG.
- Step 5:** Determine the mobility graph of each node.
- Step 6:** Model the ILP formulations of the DFG for using AMPL.
- Step 7:** Solve the ILP formulations using LP-Solve.
- Step 8:** Find the scheduled DFG.
- Step 9:** Determine the cycle frequencies, cycle frequency index and base frequency.
- Step 10:** Estimate power and energy consumptions of the scheduled DFG.



# CPF-DFC\* Minimization: Results

## (Benchmarks and Resource Constraints used)

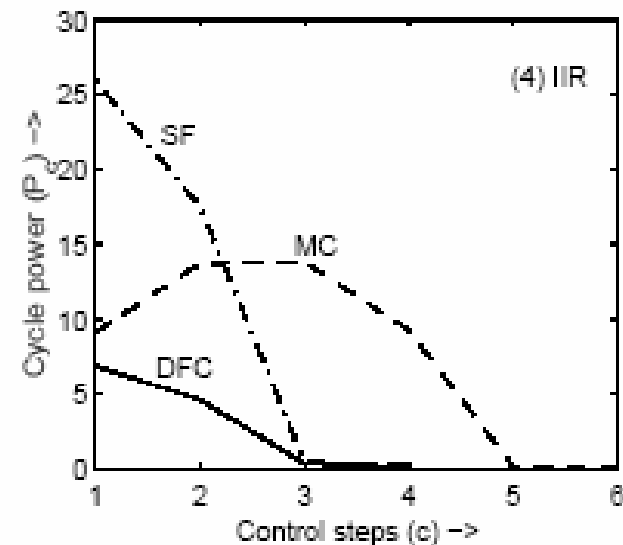
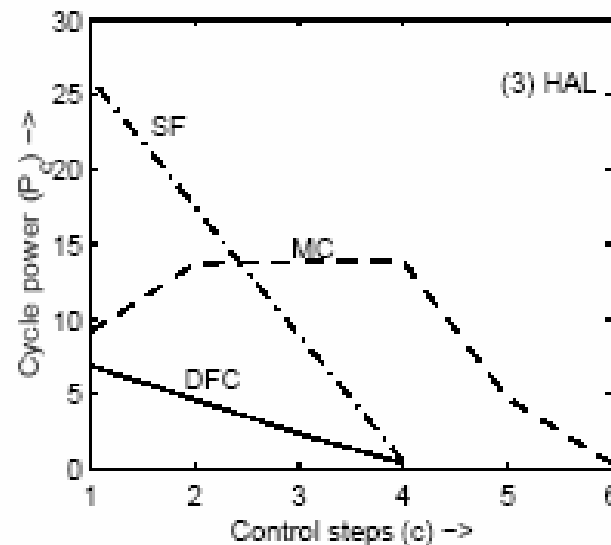
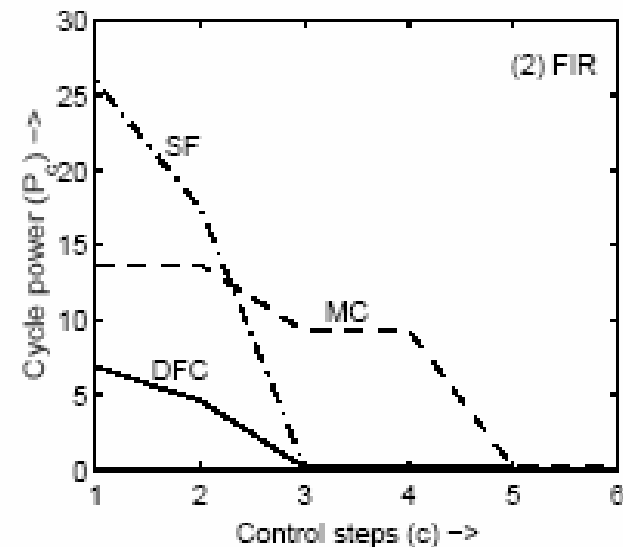
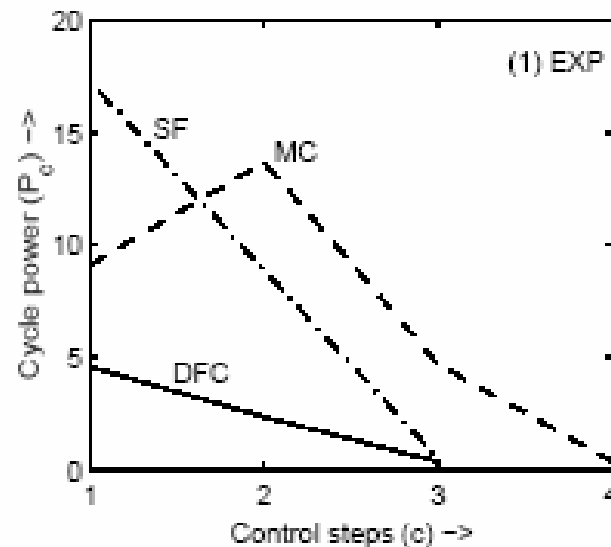
1. Example circuit (EXP) (8 nodes, 3\*, 3+, 9 edges)
2. FIR filter (11 nodes, 5\*, 4+, 19 edges)
3. IIR filter (11 nodes, 5\*, 4+, 19 edges)
4. HAL differential eqn. solver (13 nodes, 6\*, 2+, 2-, 1 <, 16 edges)
5. Auto-Regressive filter (ARF) (15 nodes, 5\*, 8+, 19 edges )

Multipliers		ALUs		Serial No
2.4V	3.3V	2.4V	3.3V	
2	1	1	1	RC1
3	0	1	1	RC2
2	0	0	2	RC3

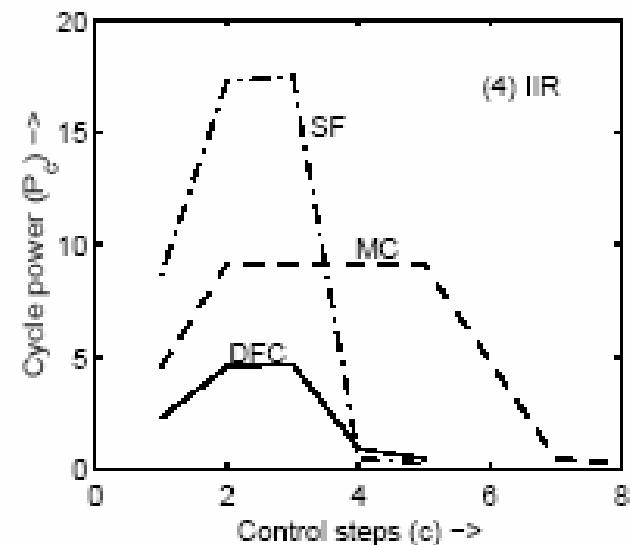
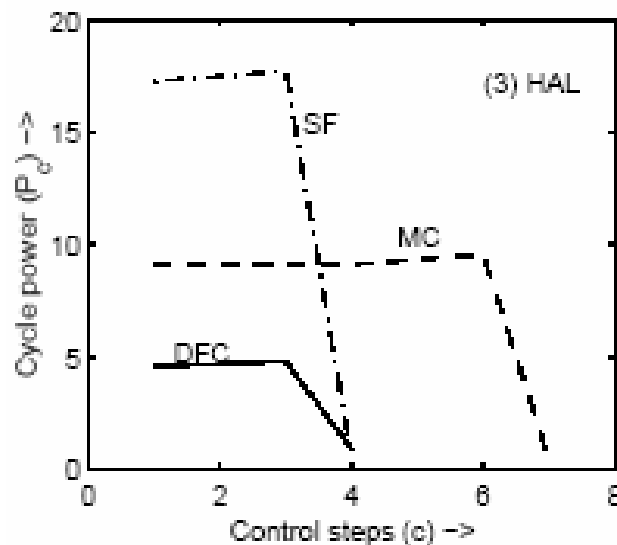
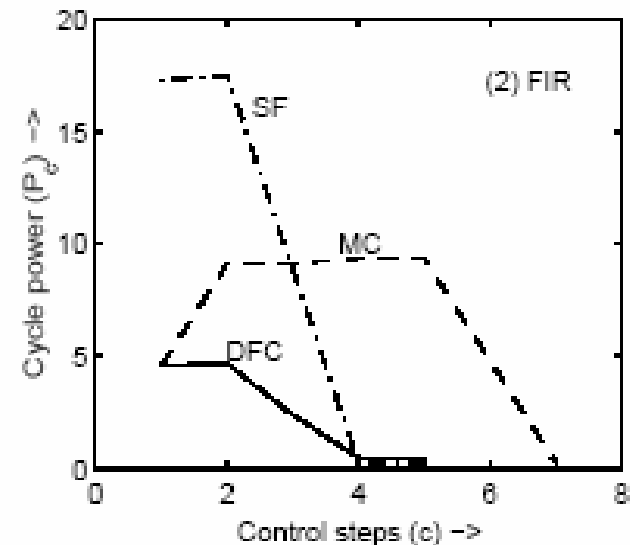
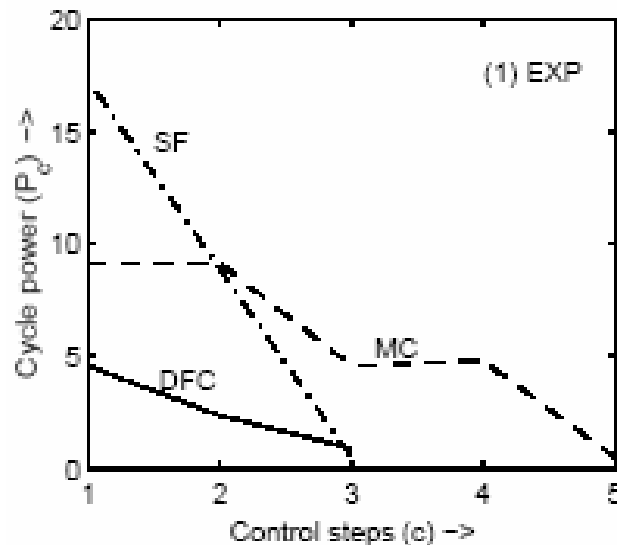
## CPF-DFC\* Minimization: Results ....

Power	% Reduction
Peak Power	71.70
Peak Power Differential	74.00
Average Power	70.82
Energy	44.36
Energy Delay Product	17.31

# CPF-DFC\* Min: Power Profile for RC2



# CPF-DFC\* Min: Power Profile for RC3



# Conclusions

- ❑ The reduction of peak power, peak power differential, average power and energy are equally important.
- ❑ The function CPF-DFC could capture all the different forms of power and its minimization using heuristic or ILP could yield significant reductions in all the different forms of power.
- ❑ The MVDFC approach found out to be better alternative. For the circuits having almost equal number of addition and multiplier operations in the critical path the savings are maximum with no time penalty for MVDFC case.
- ❑ The scheduling schemes are useful for data intensive applications.