Abstract

Replacement of SiO₂ as gate dielectric with alternative high-K dielectric materials, is considered as a method to contain the gate leakage current.

This paper provides novel attempts to evaluate the gate leakage current and propagation delay of basic logic gates comprising of such non-classical nano-CMOS transistors.

High-K Dielectrics in CMOS Technology

• Several materials have been investigated for use in nano-CMOS technology, such as ZrO₂, TiO₂, BST, HfO₂, Al₂O₃, SiON, and Si₃N₄.
• Intel has recently prototyped a processor called Penryn using such transistors of 45nm technology.
• For compact modeling based study of high-K non-classical transistors using BSIM4/5, two possible options can be considered:
  (i) varying the model parameter in the model card that denotes relative permittivity (EPSROX)
  (ii) finding the equivalent oxide thickness (EOT) for a dielectric under consideration.

Analysis of Logic Gates

• Calculated by evaluating both the source and drain components.
• For a MOS, \( I_{ox} = (I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}) \).
• Values of individual components depends on states: ON, OFF, or transition.

Four different states for 2-input NAND:

\[
I_{oc}(\text{State}) = \sum_{i=0}^{3} I_{oc}(\text{State } i)
\]

While characterizing the gate leakage current we present its average value over various switching states of the device.

\[
I_{oc} = \frac{1}{4} \left( I_{00} + I_{01} + I_{10} + I_{11} \right)
\]

The effect of varying dielectric material was modeled by calculating an equivalent oxide thickness \( T_{ox} \) according to the formula:

\[
T_{ox} = \frac{K_{gate}}{K_{ox}} T_{gate}
\]

Effect of capacitive load

• We presented a comprehensive analysis of the transient behavior of a CMOS logic gate for a 45nm BSIM4 model.
• A first principle physics based approach will be used followed by TCAD based simulations for validation.

Conclusions

• We performed curve-fitting for the data for each attribute viz. K, Tgate, and VDD for their effect on gate tunneling current and propagation delay.
• The results of this modeling can be used in back-end tools of design and automatic synthesis frameworks for on-the-fly calculation.

Table 1. Curve Fitting for effect of Process and Design Variations in 2-input NAND

| Parameter | Formula
<table>
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<tbody>
<tr>
<td>Tgate</td>
<td>( T_{gate} = a \cdot \exp(b \cdot V_{DD}) + c )</td>
</tr>
<tr>
<td>K</td>
<td>( K = a \cdot \exp(b \cdot V_{DD}) + c )</td>
</tr>
<tr>
<td>VDD</td>
<td>( V_{DD} = a \cdot \exp(b \cdot T_{gate}) + c )</td>
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• The effect of process variation on the gate tunneling current and propagation delay for various dielectric is studied.
• Among the dielectrics considered, HfO₂ has the highest dielectric constant (K=22) while SiO₂ has the lowest (K=3.9).
• Supply voltages varied from 0.5V to 1.0V.
• Tgate varied from 1.4nm to 2.0nm.
• Loading condition also varied for analysis.

Evaluation of selected gate dielectrics