Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation

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Abstract

Analysis of Effects of Scaling on Power Components

Accounting for Process Variation

The provided statistical information for each input corner is used to generate N = 1000 Monte Carlo runs (per corner) which provides statistical distributions of the output parameter

Process Variation Aware Power and Performance Characterization

A hierarchical methodology is followed to characterize architectural level units for gate leakage, subthreshold leakage, and dynamic power, as well as their propagation delay.

Introduction

Current flow paths in a nano-CMOS transistor during power dissipation in different states of operation:

- \( I_1 \): drain to source active current (ON state), \( I_2 \): drain to source short circuit current (OFF state), \( I_3 \): gate oxide leakage current (both ON and OFF states), \( I_4 \): gate current due to hot carrier injection (both ON and OFF states), \( I_5 \): gate-induced drain leakage (OFF state), and \( I_6 \): reverse bias PN junction leakage (both ON and OFF states).

The functional units are synthesized into a network of 2-input NAND gates. Since the total current in the functional unit can be defined as the sum of currents in the individual NAND gates, and the distributions for each gate are statistically independent of each other, the mean and variance of the currents can be derived as:

\[
\mu_{\text{FU}} = N \cdot \mu_{\text{NAND}}, \quad \sigma_{\text{FU}} = \sqrt{N} \cdot \sigma_{\text{NAND}}
\]

where there are \( N \) NAND gates in the implementation of the functional unit.

Conclusions

- The effect of scaling of three parameters, \( \text{Tox}, \ V\text{th}, \ \text{and VDD} \) on various power (current) components was studied.
- It was observed that simultaneous scaling of all three may not result in expected power-performance tradeoff, with the expectation derived simply from the effect of individual parameter variations.
- Hence, power optimization techniques in circuit or process design employing parameter selection or assignment need to do so judiciously based on multivariate effects.

Characterization data for various corners:

Corner 5: \( \text{Tox} = 1.4\text{nm}, \ V\text{th} = 0.22\text{V}, \ \text{VDD} = 0.9\text{V} \)

Corner 4: \( \text{Tox} = 1.7\text{nm}, \ V\text{th} = 0.25\text{V}, \ \text{VDD} = 0.7\text{V} \)

Nominal results showing individual components of power consumption for different output corners. It may be noted that the total current values are reduced and the proportion of different components in the total current have changed. Only two corners are shown for brevity. In corner 5 vs. corner 4, all parameters have been scaled i.e. \( \text{Tox} \) and \( \text{Vth} \) are increased and \( \text{VDD} \) is decreased.

We refer to “scaling” as the process of reduction of power. In that sense, scaling \( \text{VDD} \) implies reduction in its value but scaling \( \text{Tox} \) and \( \text{Vth} \) implies an increase in their values.