A 45nm Flash Analog to Digital Converter for Low Voltage High Speed System-on-Chips

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Introduction and Motivation

- ADCs are interfaced with digital circuits in mixed signal chips, where digital signal processing is performed.
- Supply voltage decreasing rapidly for digital circuits as technology scales.
- Analog to digital converters required to be operating with these devices at the same voltages.
- The proposed design meets both criteria: Low supply voltage ($0.7V$) and technology ($45nm$).
Specifications

- Resolution: 6 bits.
- Technology: 45nm.
- Speed: 1Gs/sec.
- $V_{\text{LSB}}$: 500μV.
- $V_{\text{DD}}$: 0.7V.
- INL: 0.46LSB.
- DNL: 0.70LSB.
- SNDR: 31.9dB.
## Related Research Works

<table>
<thead>
<tr>
<th>Reference</th>
<th>Resolution (bits)</th>
<th>Technology (nm)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
<th>SNDR (dB)</th>
<th>VDD (V)</th>
<th>Power (mW)</th>
<th>Samples/s</th>
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<th>SNDR (dB)</th>
<th>VDD (V)</th>
<th>Power (mW)</th>
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Design of flash ADC

- High level block diagram of ADC.
- Input is analog (generally ramp or sine wave).
- Output of Comparator Bank is thermometer code.
- Converted to 1-out of n code using 1-out of n code generators.
- NOR ROM converts the 1-out of n code to binary code.
Design of flash ADC

- For an n-bit ADC we need: $2^n - 1$ Comparators.
- 1-out of n code generators.
- NOR ROM : $2^n - 1 \times n$.
- For discussion purposes, 3-bit flash ADC is shown. 6-bit ADC has similar structure.
Threshold Inverter Quantization Principle

- TIQ comparator.
- Formed by cascading of digital inverters.
- Sizing of transistors determine switching point.

- Differential comparator.
- Require resistive ladder network.
- Area overhead increases.
TIQ Comparator

- Formed by four cascaded inverters.
- Provide a sharper switching for the comparator and full voltage swing.
- Sizes of PMOS and NMOS in a comparator are same, but different for different comparators.
Transistor sizing

- DC parametric sweep is used to determine the transistor sizes.
- Input voltage varied from 0 to 0.7V in steps of 500µV.
- W/L for NMOS transistors kept as 90nm/90nm. L for PMOS transistors kept as 90nm. W for PMOS transistors was given a parametric sweep in steps of 1nm. Minimum width=51nm, maximum width=163nm.
Transient analysis carried out.

Ramp generated from 296.3\,mV to 327.8\,mV. Digital codes going from 0 to 63 are obtained at the output.
Ideal vs Actual Characteristics

- Ideal vs actual transfer function
- Due to transistor implementation, actual transfer function never equal to ideal transfer function.
- Characterized using DNL and INL.
Max DNL of ADC = 0.7LSB

- Differential Non-Linearity. Difference between actual step width and ideal value of 1LSB.

- Modeled as Verilog-A block. Uses histogram method. DNL<1LSB ensures monotonicity.
Max INL of ADC = 0.46 LSB

- Integral No-linearity. Deviation of actual transfer function from a straight line. expressed in LSB.
- Verilog-A block used. Slowly varying ramp given as input, covering full scale range in 4096 steps.
SNDR = 31.9 dB

Signal to noise and distortion ratio.
ADC output fed to Ideal DAC. FFT of DAC output obtained. SNDR calculated from this.

\[
SNDR = 20 \cdot \log_{10} \left( \frac{A_{\text{RMS,Signal}}}{A_{\text{RMS,noise+harmonics}}} \right) dB
\]
Instantaneous Power Plot

- Peak Power = 45.42 μW.
- Avg. Power = 8.8 μW.
- Low power design.
Conclusion and Future Works

- Successful ADC design at nano-scale (45nm) technology.
- DNL = 0.7 LSB, INL = 0.46 LSB.
- SNDR = 31.9 dB, Low power design (Avg. Power = 8.8 $\mu W$).
- Layout using 90nm general process design kit.
- Scaling the layout rules to perform layout at 45nm.