Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs. PMOS Perspective

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Outline of the Talk

- CMOS scaling – Trends and Effects
- Leakage dissipation in Nano-CMOS
- Gate leakage analysis – 3 Proposed Metrics
- Impact of process variation on the metrics
- Monte Carlo Simulations: Modelling Variations
- Summary and Conclusions
Almost the entire electronic appliance industry today is driven by CMOS technology.
CMOS Technology Scaling and Leakage Dissipation
Scaling Trend – Transistor Count

VLSI technology is the fastest growing technology in the human history.
Gate length of the transistor has been decreasing with technology scaling.

All the other dimensions including gate oxide thickness have been scaled down to support this trend.

Source: Pedram ASPDAC 2004, Osburn IBM JRD Mar2002
Other Parameters Scaled?

Source: Taur IBM JRD MAR 2002
Power Dissipation in Nano-CMOS

Total Power Dissipation

Static Dissipation
- Sub-threshold Leakage
- Gate Leakage
- Reverse-biased diode Leakage

Dynamic Dissipation
- Capacitive Switching Current
- Transient Gate Leakage
- Short Circuit Current
Leakages in Nanoscale CMOS

I₁ : reverse bias pn junction (both ON & OFF)
I₂ : subthreshold leakage (OFF)
I₃ : oxide tunneling current (both ON & OFF)
I₄ : gate current due to hot carrier injection (both ON & OFF)
I₅ : gate induced drain leakage (OFF)
I₆ : channel punch through current (OFF)

Contributions of Our Paper and Related Research
Contributions of Our Paper

1. Both ON and OFF state gate leakage are significant.
2. During transition of states there is transient effect is gate tunneling current.
3. Three metrics: $I_{ON}$, $I_{OFF}$, and $C_{tunneling}$
4. $C_{tunneling}$: Manifests to intra-device loading effect of the tunneling current.
5. NMOS Vs PMOS in terms of three metrics.
6. Study process/supply variation on three metrics.
Contributions of Our Paper
(Salient Feature)

The metric, effective tunneling capacitance essentially quantifies the intra-device loading effect of the tunneling current and also gives a qualitative idea of the driving capacity of a Nano-CMOS transistor.
Gate Capacitance of a Transistor (Intrinsic)
We propose that transient in gate tunneling current due to state transitions are manifested as capacitances.
Related Research Works (Gate Leakage Analysis)

- **Ghibaudo 2004**: Characterization and modeling issues of ultra thin oxide devices
- **Mukhopadhyay 2003**: Characterization methodology is proposed along with reduction
- **Yang 1999**: Direct tunneling current and CV measurements in MOS devices used to model
- **Hertani 2005**: Provide leakage analysis of NAND, NOR, XOR gates
Related Research Works

- No work characterize both ON and OFF
- No work examine the device or a logic gate when it changes stated:
  
  ON $\rightarrow$ OFF or OFF $\rightarrow$ ON
Analysis in a Nano-CMOS Transistor
Outline: Nano-CMOS Transistor

- Dynamics of gate oxide tunneling in a transistor
- SPICE model for gate leakage
- ON, OFF, and transition states of a transistor
- Gate leakage in ON, OFF, and transition states of a transistor
Gate Leakage Components
(BSIM4 Model)

- $I_{gs}$, $I_{gd}$: tunneling through overlap of gate and diffusions
- $I_{gcs}$, $I_{gcd}$: tunneling from the gate to the diffusions via channel
- $I_{gb}$: tunneling from the gate to the bulk via the channel
ON State: NMOS Transistor
ON State: PMOS Transistor
OFF State: NMOS Transistor
OFF State: PMOS Transistor
Transition State: PMOS Transistor
NMOS Gate Leakage Current (For a Switching Cycle)

Fig. 1

Fig. 2
PMOS Gate Leakage Current (For a Switching Cycle)

Fig. 1

Fig. 2
Three Metrics for Tunneling Current
Gate Leakage: Observation

The behavior of the device in terms of gate tunneling leakage must be characterized not only during the steady states but also during transient states.
Gate Leakage: Metrics

- Gate leakage happens in ON state: $I_{ON}$
- Gate leakage happens in OFF state: $I_{OFF}$
- Gate leakage happens during transition: $C^{tun}_{eff}$
Gate Leakage for a Transistor

- Calculated by evaluating both the source and drain components

- For a MOS, $I_{ox} = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$

- Values of individual components depend on states: ON, OFF, or transition
Gate Leakage Current (For a Switching Cycle)

For NMOS

For PMOS
Inverter: Gate Leakage Paths 
(Putting NMOS and PMOS together)

Negligible Channel and Body components

Low Input

High Input

Negligible Body component
Inverter: Gate Leakage Current (For a Switching Cycle)
Transient Gate Leakage: 

\[ C_{eff}^{tun} = \begin{pmatrix} C_{gs}^{tun} \\ C_{gd}^{tun} \\ C_{gcs}^{tun} \\ C_{gcd}^{tun} \\ C_{gb}^{tun} \end{pmatrix} \]

5 components

We propose to quantify as:

\[ C_{eff}^{tun} = \frac{I_{ON} - I_{OFF}}{\frac{dV_g}{dt}} \]

\[ = \frac{I_{ON} - I_{OFF}}{V_{DD}} \cdot t_r \] (for equal rise/fall time)
Effect of Process and Design Parameter Variation
$I_{ON} / I_{OFF}$ Versus $T_{ox}$: NMOS

Oxide Thickness ($T_{ox}$) →

Gate Leakage (A/μm) →

$I_{ON}$

$I_{OFF}$

$I_{ON}$ [A/μm] →

$I_{OFF}$ [A/μm] →
$I_{ON} / I_{OFF}$ Versus $T_{ox}$: PMOS

- Gate Leakage ($A/\mu m$)
- Oxide Thickness ($T_{ox}$)

Graph showing $I_{ON}$ and $I_{OFF}$ as functions of oxide thickness ($T_{ox}$).
$I_{\text{ON}} / I_{\text{OFF}}$ Versus $T_{\text{ox}}$: Inverter
$C_{\text{eff}}^{\text{tun}}$ Versus $T_{\text{ox}}$: NMOS

Gate Leakage (A/μm) $\rightarrow$

Oxide Thickness ($T_{\text{ox}}$) $\rightarrow$
$C_{\text{eff}}^{\text{tun}}$ Versus $T_{\text{ox}}$: PMOS

Gate Leakage ($\text{A/}\mu\text{m}$) $\uparrow$

Oxide Thickness ($T_{\text{ox}}$) $\rightarrow$

Oxide Thickness ($T_{\text{ox}}$) $\rightarrow$
$C_{\text{eff}}^{\text{tun}}$ Versus $T_{\text{ox}}$: Inverter

Oxide Thickness ($T_{\text{ox}}$) $\rightarrow$

Gate Leakage (A/μm) $\uparrow$
Summary and Conclusions
Monte Carlo Simulations: (Modeling Variations)

Monte Carlo (N=1000) results.

- 10% variation in gate oxide and supply assumed.

\[ I_{ON} \]
\[ \mu = 174.5 \text{nA} / \mu \text{m} \]
\[ \sigma = 292.9 \text{nA} / \mu \text{m} \]

\[ I_{OFF} \]
\[ \mu = 105.2 \text{nA} / \mu \text{m} \]
\[ \sigma = 184.8 \text{nA} / \mu \text{m} \]

\[ C_{eff} \]
\[ \mu = 279.7 \text{aF} / \mu \text{m} \]
\[ \sigma = 477.6 \text{aF} / \mu \text{m} \]
Monte Carlo Simulations: (Modeling Variations)

- All three metrics follow lognormal distribution.
- This is expected since gate $T_{ox}$ and $V_{dd}$ are assumed normally distributed and $I_{ox}$ depends exponentially on both.
- Small parameter variation (10%) leads to large deviance in the metrics (2-3 sigma).
Both ON and OFF states contribute to gate oxide leakage.

Transient effect is significant and can be captured via effective tunneling capacitance.

$I_{ON}$ and $I_{OFF}$ metrics to quantify gate leakage current during steady state.

$C_{eff_{tun}} \equiv$ Effective tunneling capacitance at the input of a logic gate.
Usefulness of the Proposed Metrics

- The metrics allow designers to account for gate tunneling effect in nano-CMOS based circuit designs.

- $I_{ON}$ and $I_{OFF}$ - additive to static power consumption.

- $C_{eff}^{tun}$ – additive to intrinsic gate capacitance
  
  $C_{logic} = C_{eff}^{tun} + C_{intrinsic}$

- All three needs to be taken into account for effective total (switching, subthreshold, gate leakage) power optimization
Thank You

For more information:
http://www.cse.unt.edu/~smohanty