Power Dissipation

CMOS VLSI Design

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Outline of the Talk

- Power and Energy
- Dynamic Power
- Static Power
- Low Power Design
Power Dissipation Trend
Power delivery and dissipation will be prohibitive
Power density Trend

Power density too high to keep junctions at low temp
Power Dissipation in CMOS

Power Dissipation

Static Dissipation

- Sub-threshold current
- Gate Leakage
- Reverse-biased diode Leakage
- Contention current

Dynamic Dissipation

- Capacitive Switching
- Gate Leakage
- Short circuit

Source: Weste and Harris 2005
Leakages in CMOS

$I_1$: reverse bias pn junction (both ON & OFF)
$I_2$: subthreshold leakage (OFF)
$I_3$: Gate Leakage current (both ON & OFF)
$I_4$: gate current due to hot carrier injection (both ON & OFF)
$I_5$: gate induced drain leakage (OFF)
$I_6$: channel punch through current (OFF)

Source: Roy 2003
Power Dissipation Redistribution

Source: Hansen Thesis 2004
Dynamic and Static Power Sources
Power Dissipation in CMOS: Dynamic

**Capacitance Switching Current:** This flows to charge and discharge capacitance loads during logic changes.

**Short-Circuit Current:** This is the current due to the DC path between the supply and ground during output transition.
Power Dissipation in CMOS: Static

- **Subthreshold Current**: Sub-threshold current that arises from the inversion charges that exists at the gate voltages below the threshold voltage.
- **Tunneling Current**: There is a finite probability for carrier being pass through the gate oxide. This results in tunneling current thorough the gate oxide.
- **Reverse-biased Diode Leakage**: Reverse bias current in the parasitic diodes.
- **Contention Current in Ratioed Circuits**: Ratioed circuits burn power in fight between ON transistors.
Power Dissipation in CMOS: Dynamic

- Dynamic power is required to charge and discharge load capacitances when transistors switch.
- One cycle involves a rising and falling output.
- On rising output, charge $Q = CLV_{DD}$ is required.
- On falling output, charge is dumped to GND.

A general CMOS transistor circuit
Power Dissipation in CMOS: Dynamic

\[ E_{0 \rightarrow 1} = \int_0^T P(t) \, dt = V_{dd} \int_0^T i_{\text{supply}}(t) \, dt = V_{dd} \int_0^T C_L \, dV_{out} = C_L V_{dd}^2 \]

\[ E_{\text{out}} = \int_0^T P_{\text{out}}(t) \, dt = \int_0^T V_{out} i_{out}(t) \, dt = \int_0^T C_L V_{out} \, dV_{out} = \frac{1}{2} C_L V_{dd}^2 \]

**Note:**
1. the difference between the two is the loss
2. Energy doesn’t depend on frequency
Power Dissipation in CMOS: Dynamic

For $N_c$ clock cycles energy loss:

$$E_{N_c} = C_L V_{dd}^2 n(N_c)$$

$n(N_c)$: is the number of 0->1 transitions in $N_c$ clock cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_{N_c}}{N_c} f = \lim_{N \to \infty} \frac{n(N_c)}{N_c} C_L V_{dd}^2 f$$

$$= \alpha_{0 \to 1} C_L V_{dd}^2 f$$

Note: Power depends on frequency
Short Circuit Current

• When transistors switch, both nMOS and pMOS networks may be momentarily ON at once.
• Leads to a blip of “short circuit” current.
• < 10% of dynamic power if rise/fall times are comparable for input and output.
Static Power : Subthreshold Current

• In OFF state, undesired leakage current flow.
• It contributes to power dissipation of idle circuits.
• Drain-Induced-Barrier-Lowering (DIBL) an prominent effect for short channel transistors also impacts subthreshold conduction by lowering $V_T$.
• This current increases as the $V_T$ increases.
• It also increases as the temperature increases.
• If $v_t$ is the thermal voltage and $I_0$ is the current at $V_T$ then the subthreshold current is:

$$I_{ds} = I_0 \left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off}'}{n v_t}\right)$$
Static Power : Junction Leakage

• The pn junctions between diffusion, substrate and well are all junction diodes.
• These are reversed biased as substrate is connected to GND and well connected to $V_{dd}$.
• However, reversed biased diode also conduct small amount of current.

Reverse-biased diodes in CMOS circuits
Static Power : Junction Leakage

• The reverse-biased junction current is expressed as follows: (D is not for drain, S is not for source)

\[ I_D = I_S \left[ \exp \left( \frac{V_D}{V_T} \right) - 1 \right] \]

• \( I_S \) depends on the doping level, the area, and perimeter of the diffusion region.

• \( V_D \) is the diode voltage e.g. \( V_{sb} \) or \( V_{db} \).
Static Power: Tunneling

- There is a finite probability for carrier being pass through the gate oxide.

- This results in tunneling current thorough the gate oxide.

- The effect is predominately for lower oxide thickness.

BSIM4 Model
Static Power : Tunneling

• The gate oxide leakage current can be expressed as follows [Kim2003, Chandrakasan2001] (K and \( \alpha \) are experimentally derived factors).

\[
I_{gate} = K \cdot W_{gate} \left( \frac{V_{dd}}{T_{gate}} \right)^2 \exp \left( -\alpha \frac{T_{gate}}{V_{dd}} \right)
\]

• Options for reduction of gate leakage power :
  – Decreasing of supply voltage \( V_{dd} \) (will play its role)
  – Increasing gate SiO\(_2\) thickness \( T_{gate} \) (opposed to the technology trend !!)
  – Decreasing gate width \( W_{gate} \) (only linearly dependent)
Low-Power Design
Why Low Power?

Packaging costs

Chip and system cooling cost

Power supply rail

Power affects

Noise and reliability

Environmental

Battery life

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Various forms of Power Profile

• Average Power
• Total Energy
• Energy-Delay-Product (EDP)
• Power-Delay-Product (PDP)
• Power-Square-Delay-Product (PSDP)
• Peak Power
• Transient Power
• Cycle Difference Power
• Peak Power Differential
• Cycle-to-Cycle Power Gradient (Fluctuation)
• and many more ……
Why peak power reduction?

- To maintain supply voltage levels
- To increase reliability
- To use smaller heat sinks
- To make packaging cheaper
Why Average Power/ Energy reduction?

- To increase battery life time
- To enhance noise margin
- To reduce energy costs
- To reduce use of natural resources
- To increase system reliability
Why Transience / Fluctuation Minimization?

- To reduce power supply noise
- To reduce cross-talk and electromagnetic noise
- To increase battery efficiency
- To increase reliability
Low-power design: Key Principles

- using the lowest possible supply voltage
- using the smallest geometry, highest frequency devices, but operating them at lowest possible frequency
- using parallelism and pipelining to lower required frequency of operation
- power management by disconnecting the power source when the system is idle
Voltage, Frequency and Power Trade-offs

- **Reduce Supply Voltage** ($V_{dd}$): delay increases; performance degradation

- **Reduce Clock Frequency** ($f$): only power saving

- **Reduce Switching Activity** ($N$ or $E(sw)$): no switching no power loss !!! Not in fully under designers control. Switching activity depends on the logic function. Temporal/and spatial correlations difficult to handle.

- **Reduce Physical Capacitance**: done by reducing device size reduces the current drive of the transistor making the circuit slow
How much we save ?? Varying $V_{dd} / f$

<table>
<thead>
<tr>
<th>Voltage ($V_{dd}$)</th>
<th>Frequency ($f$)</th>
<th>Power ($P_d$)</th>
<th>Energy ($E_d$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>$f_{\text{max}}$</td>
<td>$P_d$</td>
<td>$E_d$</td>
</tr>
<tr>
<td>$V_{dd} / 2$</td>
<td>$f_{\text{max}}^*$</td>
<td>$P_d / 4$</td>
<td>$E_d / 4$</td>
</tr>
<tr>
<td>$V_{dd} / 2$</td>
<td>$f_{\text{max}} / 2$</td>
<td>$P_d / 8$</td>
<td>$E_d / 4$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$f_{\text{max}} / 2$</td>
<td>$P_d / 2$</td>
<td>$E_d$</td>
</tr>
</tbody>
</table>

* Note: $f_{\text{max}}$ Vs $f$
Low Power Design: Static Reduction

• Reduce static power
  – Selectively use ratioed circuits
  – Selectively use low $V_t$ devices
  – Leakage reduction:
    stacked devices, body bias, low temperature