P3 (Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP

Garima Thakral¹, Saraju P. Mohanty², Dhruva Ghai³, Dhiraj K. Pradhan⁴

Computer Science and Engineering, University of North Texas, USA.¹,²,³
Department of Computer Science, University of Bristol, UK.⁴
Email-ID: saraju.mohanty@unt.edu², pradhan@compsci.bristol.ac.uk⁴.

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A novel design flow is presented for simultaneous P3 (power minimization, performance maximization and process variation tolerance) optimization of nano-CMOS circuits.

For demonstration of the effectiveness of the flow, a 45 nm single-ended 7-transistor SRAM is used as example circuit.

The SRAM cell is subjected to a dual-$V_{Th}$ assignment based on a novel statistical Design of Experiments-Integer Linear Programming (DOE-ILP) approach.

Experimental results show 44.2% power reduction (including leakage) and 43.9% increase in the read static noise margin compared to the baseline design.

The process variation analysis of the optimized cell is carried out considering the variability in 12 parameters.
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Garima Thakral1, Saraju P. Mohanty2, Dhruba Ghai3, and Dhiraj K. Pradhan4
Department of Computer Science and Engineering, University of North Texas, USA.1,2,3
Department of Computer Science, University of Bristol, UK.4
Email-ID: saraju.mohanty@unt.edu2, pradhan@compsci.bristol.ac.uk4.

Abstract

• In this research paper, a novel design flow is presented for simultaneous P3 (power minimization, performance maximization and process variation tolerance) optimization of nano-CMOS circuits.
• The SRAM cell is subjected to a dual-VThs assignment based on a novel statistical Design of Experiments-Integer Linear Programming (DOE-ILP) approach.
• A 45nm single-ended 7-transistor SRAM is used as example circuit.
• Experimental results show 44.2% power reduction (including leakage) and 43.9% increase in the read static noise margin (SNM) during the read operation. The “read SNM” required to flip the state of the SRAM cell as the minimum DC noise voltage which is a well-established process-level technique, called dual-VThs, is used for reduction of power consumption.
• It is very important to choose appropriate transistors for high-VTh assignment, thus, the statistical DOE-ILP methodology is proposed.
• Further, ILP is useful for optimizing the linear objective function subjected to constraints and obtain a bound on the optimal value to solve the predictive equations formed using DOE. Minimum sized transistors are taken for the baseline design.

Design of Seven Transistor SRAM

The baseline 7-transistor SRAM cell is shown in Figure 3. The SRAM cell operates on a single bit line instead of the traditional two bit lines as in case of 6-transistor SRAM cell performing both read and write operations.

Statistical DOE-ILP Optimization Algorithm

Algorithm 1: P3 optimization in nano-CMOS SRAM
1. Input: Baseline PDR and SNM of the SRAM cell; Baseline model file; High-threshold model file
2. Output: Optimized objective set \( f_{opt} = \{ f_{SNM}, f_{PDR} \} \) optimal SRAM cell with transistors identified for high-VTh assignment
3. Setup experiment for transistors of SRAM cell using 2-Level Taguchi L8 array, where the factors are the VThs, states of transistors of SRAM cell, the response for average power consumption \( p(V_{TH}, V_{dd}) \), and for the response for read-SNM is \( \mu_{SNM}, \sigma_{SNM} \)
4. For each L8 experiments of 2-Level Taguchi L8 array do
5. Run 100 Monte Carlo simus
6. Record \( p_{opt}, \mu_{SNM}, \sigma_{SNM} \)
7. end for
8. Form linear predictive equations \( \mu_{V_{TH}, V_{dd}}, \sigma_{V_{TH}, V_{dd}} \) for power \( p(V_{TH}, V_{dd}) \) and SNM
9. Solve \( f_{opt} \) using ILP: Solution set \( S_{PDR, SNM} \)
10. Solve \( f_{opt} \) using ILP: Solution set \( S_{PDR, SNM} \)
11. Solve \( f_{opt} \) using ILP: Solution set \( S_{PDR, SNM} \)
12. Solve \( f_{opt} \) using ILP: Solution set \( S_{PDR, SNM} \)
13. Form \( S_{opt} = S_{PDR} \cap S_{PDR} \cap S_{PDR} \cap S_{PDR} \)
14. Assign high VThs to transistors based on \( S_{opt} \)
15. Re-simulate SRAM cell to obtain optimized objective set

Figure 1 presents novel design flow for P3-optimal SRAM. The optimizing cell is arranged using P3 optimized SRAM cell to study the feasibility of P3-optimal SRAM array construction.

The proposed methodology for P3 optimality

For each DOE experiments measure Power and SNM

Form predictive equations \( \mu_{PDR}, \sigma_{PDR}, \mu_{SNM}, \sigma_{SNM} \)

Solve predictive equations using ILP

Obtain \( S_{opt} = \{ f_{PDR}, f_{SNM} \} \) optimal SRAM cell

Assign high VThs to transistors based on \( S_{opt} \)

P3-optimal SRAM cell

Figure 1. Proposed flow for P3-Optimal SRAM.

Figure 2. Power and SNM Measurement

Figure 3. A 7-transistor SRAM cell [12].

The optimized butterfly curve is shown in Fig. 9(b). Fig. (a) shows the effect of process variations on the butterfly curve of the P3 optimized SRAM. Fig. (b) shows the distributions for “SNM High” and “SNM Low” extracted from the Monte Carlo simulations. “SNM Low” is treated as the actual SNM. Fig. (c) shows the distribution of average power of the P3 optimized SRAM cell under process variations.

Summary, Conclusions, and Future Works

• A statistical DOE-ILP approach has been presented in this paper for simultaneous P3 optimization of SRAM cell.
• As part of extension of this research, a P4 optimal methodology is under consideration, where the 4th “P” would be parasitics. Thermal effects will also be incorporated in the future which will lead to what is envisioned as P4VT optimal; V stands for voltage and T stand for temperature.
• Also, array-level optimization of SRAM with mismatch and process variation will be considered as part of the design flow.