Design and Modeling of a Continuous-Time Delta-Sigma Modulator for Biopotential Signal Acquisition: Simulink Vs Verilog-AMS Perspective

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Agenda

- Motivation
- Continuous-time (CT) delta-sigma modulator (DSM) design overview
- Modeling tools and languages selection in each design step
- Conclusions
Motivation

- Analog and mixed-signal systems-on-a-Chip (AMS-SoC) are becoming more complex
- Simulating an entire AMS system with transistor-level netlists is infeasible
- Behavioral level simulations are crucial in AMS design and verification
- Simulink and Verilog-AMS are two well-known tools for behavioral modeling
CT DSM Design Overview

Design specifications
- Resolution: 10-bit
- Bandwidth: 10 kHz
- … …

DSM design parameters
- Order, OBG, OSR, etc.

Time-domain simulation, numerical fitting required

DT DSM design tools are quite mature compared to CT DSM
System-Level CT DSM Design Flow

Start

System Design Parameters

DT DSM Synthesis

DT DSM Design

DT-to-CT Conversion

CT DSM Design

Dynamic Range Scaling

Building Block Implementation

CT DSM Simulation with Non-idealities

CT DSM Building Block Specifications and Component Values

End

MATLAB

SIMULINK

Verilog-AMS

AMS Designer
DSM Structures

Required components
• Op amps
• Sampler/Quantizer
• … …
Order = 3; 
OSR = 128; 
nlev = 2; 
OBG = 1.3; 
f0 = 0; 
opt = 0; 
form = 'CIFF'; 
td = 0.2;

MATLAB DSM Design Toolbox

\[ L(z) = \frac{0.5217(z^2 - 1.756z + 0.7826)}{(z-1)^3} \]

\[ NTF(z) = \frac{1}{1 + L(z)} \]
MATLAB DT DSM Simulation

• MATLAB simulation shows that the DT DSM design satisfies the SNR requirement

\[ \text{SNR}_{\text{DT}} = 100.5 \text{ dB} \]
DT-to-CT Conversion

Find coefficients $a_0$ to $a_3$ and $d_1$ to $d_3$?
DT-to-CT Conversion

• Finding the coefficients requires behavioral models, time-domain simulations, and numerical fitting

• Built-in libraries in SIMULINK provide a comprehensive collection of fundamental building blocks

• Writing codes and creating symbols for fundamental building blocks are necessary if Verilog-AMS is used
SIMULINK CT DSM Simulation

• The CT DSM simulation result is compared with the DT DSM result
Building Block Implementation with Non-idealities

Two criteria when deciding the tool/language for this step:

- The modeling language should be able to describe the non-idealities and allow them to be integrated into the ideal model without a great deal of time and effort.

- The tool should allow the designer to switch each individual building block between ideal model, non-ideal model, and actual circuit implementation.
CT DSM Implementation

Two important non-idealities:
- Finite Gain-Bandwidth Product (GBW)
- Clock Jitter
Verilog-AMS (AMS Designer) is chosen:

- Actual circuit schematics and layouts are to be done in CADENCE
- SIMULINK requires extra effort for configuration on both sides, and the simulation procedure is not as convenient
- Modeling clock jitter in Verilog-AMS is relatively easier
Finite GBW

\[ V(\text{outd}) \leftarrow \text{laplace}_\text{nd}( (V(\text{inp, inm}) - V(\text{fbp, fbm})), \{-1\}, d); \]

![Graph showing PSD vs. \( \omega/\pi \) with Signal band, SNR_{GBW(Lo)} = 81.7 dB, SNR_{GBW(Optimal)} = 96.9 dB, and SNR_{Ideal} = 97.6 dB.]}
Clock Jitter

Function $\text{rdist\_normal}$ for RMS jitter:
- 1 ps, 10 ps, and 100 ps

![Graph showing PSD and SNR values for different jitters.]

- $\text{SNR}_{\text{jitter(100 ps)}} = 80.0$ dB
- $\text{SNR}_{\text{jitter(10 ps)}} = 95.5$ dB
- $\text{SNR}_{\text{jitter(1 ps)}} = 95.6$ dB
- $\text{SNR}_{\text{Ideal}} = 97.6$ dB

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Simulator Settings

Accuracy vs Speed
- Start with conservative settings to find out the theoretical limit and then gradually increase the tolerance to get a good tradeoff

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<th>Simulator</th>
<th>Settings</th>
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<td>Voltage Absolute tolerance: $1 \times 10^{-6}$</td>
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<td>Current Absolute tolerance: $1 \times 10^{-12}$</td>
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</table>
Conclusions

- A CT DSM design flow along with modeling tools and languages for each step has been presented.

- The choice of modeling tools and languages depends on the objective, design cycle time, and budget.
Questions?

Thank You!!!