Ultra-Fast Design Exploration of Nanoscale Circuits through Metamodelling

Presenter:

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Outline of the Talk

- Nanoscale Design Challenges
- The Proposed Ultra-Fast Solution
- Metamodel Types and Proposed Techniques
- Algorithms for Optimization over Metamodels
- Experiments Using Case Studies
- Conclusions and Future Research
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A typical consumer electronics is an Analog/Mixed-Signal System-on-a-Chip (AMS-SoC).

Individual subsystems can also be mixed-signal, e.g. Phase-Locked Loop (PLL).
Nano-CMOS Circuit: Design Space

- Variability
- Power
- Leakage
- Performance
- Area
- Thermal
- Reliability
- Yield
One of the Key Issues: Time/Effort

- The simulation time for a Phase-Locked-Loop (PLL) lock on a full-blown (RCLK) parasitic netlist is of the order of many days!

- Issues for AMS-SoC components:
  - How fast can design space exploration be performed?
  - How fast can layout generation and optimization be performed?
Standard Design Flow – Very Slow

- Standard design flow requires multiple manual iterations on the back-end layout to achieve parasitic closure between front-end circuit and back-end layout.
- Longer design cycle time.
- Error prone design.
- Higher non-recurrent cost.
- Difficult to handle nanoscale challenges.
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Automatic Optimization on Netlist
(Faster than manual flow; still slow)

- Automatic iteration over netlist improves design optimization.
- Still needs multiple simulations using analog simulator (SPICE).
- SPICE is slow.
Ultra-Fast Design Exploration Through Metamodeling

Baseline Design → Exhaustive Optimization → Optimized Design

The Actual Circuit (Netlist) Optimization -- Slow Approach

Baseline Design → Accurate Metamodeling → Fast Optimization → Optimized Design

The Metamodel-Based Approach -- Ultra-Fast Approach
Two Tier Speed Up

Baseline Mixed-Signal Circuit Layout-Aware Netlist

Metamodels of Baseline Mixed-Signal Circuit

Tradational – Slow Approach

Parameter \text{i}

Technology Constraints

Parameter \text{j}

Specification Constraints

Optimization over Metamodels

9000x Speedup

300x Speedup
Proposed Flow: Key Perspective

- Novel design and optimization methodology that will produce robust AMS-SoC components using **ultra-fast automatic iterations over metamodels** (instead of netlist) and two manual layout steps.

- The methodology easily accommodates multidimensional challenges, reduces design cycle time, improves circuit yield, and reduces chip cost.
Metamodel-Based Design Flow

- **Input Specifications of the Mixed-Signal IC**
  - Create Logical Design
  - Create Layout of the Mixed-Signal IC
  - Perform DRC/LVS/RCLK Extraction
    - Specifications met?
      - Yes: Mixed-Signal Design Schematic, Mixed-Signal Design Layout, Parasitic-Aware Mixed-Signal IC Netlist
      - No: Parameterize the Parasitic-Aware Netlist with Design Variables
        - Perform Fast and Accurate Sampling of Mixed-Signal IC Design Space
          - Create Metamodels of Figures-of-Merits of the Mixed-Signal IC
            - Metamodels of the FoMs of the Mixed-Signal IC
              - Use an Algorithm to Perform Optimization Over Polynomial Metamodels
                - Specifications met?
                  - Yes: Optimal Physical-Design Variables, Optimized Mixed-Signal IC Layout
                  - No: Create New Layout of the Mixed-Signal IC
                    - Perform DRC/LVS/RCLK Extraction
                      - Done

**Baseline Mixed-Signal IC Component Design**

**Metamodelling of Mixed-Signal IC Components**

**Optimization over Metamodels**

**Optimal Mixed-Signal IC Components**
Metamodeling vs. Macromodeling

**Macromodeling**
- Simplified version of the circuit.
- Used in the same simulation tool.
- Hard to create.

**Metamodeling**
- Mathematical representation of output.
- Based on prediction equation or algorithm.
- Language and tool independent.
- Reusable for different specifications.
- Can be applied using non-EAD tools like MATLAB.
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Metamodels: Selected Types

Nanoscale-CMOS Circuit Metamodels

- Polynomial
  - Regular Polynomial
  - Piece-wise Polynomial
- Nonpolynomial
  - Neural Networks
  - Kriging Methods
Metamodels: Polynomial Example

Actual Circuit (SPICE netlist) of AMS-SoC Components

Statistical Sampling

Polynomial Function Fitting

\[ f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p. \]
Metamodelling – Key Points

- **Accuracy** -- Capability of predicting the system response over the design space.

- **Efficiency** -- Computational effort required for constructing the metamodel.

- **Transparency** -- Capability of providing the information concerning contributions and variations of design variables and correlation among the variables.

- **Simplicity** -- Simple methods should require less user input and be easily adapted to different problem.
Metamodels: Performance Analysis

- **Root-Mean Square Error (RMSE):** Represents departure of metamodel from real-simulation (golden). Smaller RMSE means more accurate:

\[
RMSE = \sqrt{\left(\frac{1}{N}\right)\sum_{k=1}^{N} \left(FoM(x_k) - \overline{FoM}(x_k)\right)^2}
\]

- **Relative Average Absolute Error (RAAE):** Smaller RAAE means more accurate metamodel:

\[
RAAE = \left(\frac{\sum_{k=1}^{N}|FoM(x_k) - \overline{FoM}(x_k)|}{N \times \text{Standard Deviation}}\right)
\]

- **R-Square:** Larger R-square means more accurate metamodel:

\[
R^2 = \left(1 - \frac{MSE}{\text{Variance}}\right)
\]
Different flow is used for nonpolynomial metamodel generation.
Sampling Techniques: 45nm Ring Oscillator Circuit (5000 points)

Monte Carlo

MLHS

LHS

DOE
Sampling Comparison: RO / LC-VCO

RMSE Comparison for Ring Oscillator

RMSE Comparison for LC-VCO

Number of Simulations

Number of Samples
Polynomial Metamodels

- The generated sample data can be fitted in many ways to generate a metamodel.
- The choice of fitting algorithm can affect the accuracy of the metamodel.
- A simple metamodel has the following form:

  \[ y = \sum_{i,j=0}^{k} (\alpha_{ij} \times x_1^i \times x_2^j) \]

- \( y \) is the response being modeled (e.g. frequency), \( x = [W_n, W_p] \) is the vector of variables and \( \alpha_{ij} \) are the coefficients.
# Metamodel: Polynomial Comparison

<table>
<thead>
<tr>
<th>Case Study Circuits</th>
<th>Polynomial Order</th>
<th>$\mu$ error (in MHz)</th>
<th>$\sigma$ error (in MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ring Oscillator</strong></td>
<td>1</td>
<td>571.0</td>
<td>286.7</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>195.4</td>
<td>78.1</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>37.2</td>
<td>18.0</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>20.0</td>
<td>10.7</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>17.1</td>
<td>9.6</td>
</tr>
<tr>
<td><strong>45nm CMOS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Target $f$ : 10GHz</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LC-VCO</strong></td>
<td>1</td>
<td>42.3</td>
<td>40.1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>39.4</td>
<td>37.8</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>35.4</td>
<td>33.9</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>30.5</td>
<td>29.3</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>26.5</td>
<td>25.2</td>
</tr>
<tr>
<td><strong>180nm CMOS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Target $f$ : 2.7GHz</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Ring oscillator – Order 1**

\[
 f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p. 
\]

**LC-VCO – Order 1**

\[
 f(W_n, W_p) = 2.38 \times 10^9 - 3.49 \times 10^{12} W_n - 6.66 \times 10^{12} W_p. 
\]
Feed-forward dual layer NNs (FFDL) are considered.

FFDL network created for each FoM:

- Nonlinear hidden layer functions are considered each varying hidden neurons 1-20:
  \[ b_j(v_j) = \tanh(\lambda v_j) \]
Metamodel Comparison: Polynomial Vs Nonpolynomial

- Nonpolynomial (Neural Network) is more suitable for large circuits.

180nm CMOS PLL with Target Specs: $f = 2.7$GHz, $P = 3.9$mW, $8.5 \mu s$.

<table>
<thead>
<tr>
<th>Figures-of-Merits (FoM)</th>
<th>Polynomial</th>
<th>Nonpolynomial (Neural Network)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of Coefficients</td>
<td>RMSE</td>
</tr>
<tr>
<td>Frequency</td>
<td>48</td>
<td>77.96 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>50</td>
<td>2.6mW</td>
</tr>
<tr>
<td>Locking Time</td>
<td>56</td>
<td>1.9$\mu$s</td>
</tr>
</tbody>
</table>

- 56% increase in accuracy over polynomial metamodels.
- On average 3.2% error over golden design surface.
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Selected Algorithms for Optimization over Metamodels

Algorithms Applied Over Metamodels

Traditional Heuristics
- Simulated Annealing
- Tabu Search

Intelligent Algorithms
- Artificial Bee Colony (ABC)
- Ant Colony
Exhaustive Search: 45nm RO

- Searches over two parameter space.
- Parameters incremented over specified steps.
DOE Assisted Tabu Search: 45nm RO

- Search space is recursively divided into rectangles and each time the rectangle with superior result is selected.
Comparison of the Running Time of Heuristic Algorithms: 45nm RO

- **Optimization without metamodels**: the tabu search optimization is faster by ~1000× than the exhaustive search and ~4× faster than the simulated annealing optimization.

- **Optimization with metamodels**: the simulated annealing optimization is faster by ~1000× than the exhaustive search and ~6× faster than the tabu search optimization.
Bee-Colony Optimization: Overview

1. **Initial** food sources are produced for all worker bees.

2. **Do**
   1) Each worker bee goes to a food source and evaluates its nectar amount.
   2) Each onlooker bee watches the dance of worker bees and chooses one of their sources depending on the dances and evaluates its nectar amount.
   3) Determine abandoned food sources and replace with the new food sources discovered by scout bees.
   4) Best food source determined so far is recorded.

3. **While** (requirements are met)

A food source → a solution; A position of a food source → a design variable set; Nectar amount → Quality of a solution; Number of worker bees → number of quality solutions.
Bee Colony Optimization: States

- **Worker**
  - $F_{oM} > F_{oM}$
  - $P_{on} = \text{high} \& \ F_{oM} > F_{oM}$
  - $F_{oM} < F_{oM}$

- **Scout**
  - $F_{oM} = \text{low}$

- **Onlooker**
  - $P_{on} = \text{low}$
  - $F_{oM} < F_{oM}$
  - $P_{on} = \text{high} \& \ F_{oM} < F_{oM}$
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Case Study Circuit: 180nm PLL

Block diagram of a PLL.

- PLL circuit is characterized for frequency, power, vertical and horizontal jitter (for simple phase noise), and locking time.

- Metamodels are created for each FoM from same sample set.
PLL: Polynomial Metamodels ...

- PLL circuit is characterized for output frequency, power, vertical and horizontal jitter (to simplify the phase noise calculations), and locking time (or settling time).
- A separate metamodel is created for each FoM from the same sample set.
- The Root Mean Square Error (RMSE) and coefficient of determination $R^2$ are the metrics used for goodness of fit.

Generated $R^2$ and $R^2_{\text{adj}}$ for various orders of the polynomial metamodel for settling time. Notice possible overfitting.
PLL: Polynomial Metamodells ... 

- The number of coefficients corresponding to the order of the generated metamodel for settling time.
- This means that the model is over fitted, therefore for the metamodel that represents settling time, a polynomial order of 4 will be used.
The Artificial Bee-Colony (ABC) Optimization algorithm progression for the selected FoM.

Power and Jitter Results of the PLL

<table>
<thead>
<tr>
<th>Metric</th>
<th>Before Optimization</th>
<th>After Optimization</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>9.29 mW</td>
<td>0.87 mW</td>
<td>90.6%</td>
</tr>
<tr>
<td>Jitter Vertical</td>
<td>168.35 μV</td>
<td>3.28 nV</td>
<td>~100%</td>
</tr>
<tr>
<td>Jitter Horizontal</td>
<td>189 ps</td>
<td>180 ps</td>
<td>4.8%</td>
</tr>
</tbody>
</table>
PLL parameters with constraints and optimized values.

- An exhaustive search of the design space of 21 parameters with 10 intervals per parameter requires $10^{21}$ simulations.
- $10^{21}$ SPICE simulations is slow; 10min per one.
- $10^{21}$ simulations using polynomial metamodels is fast.
- Time savings: $\approx 10^{20} \times$ SPICE simulation time.
PLL: ABC Optimization: Poly. Vs NN

Figure-of-Merit used for optimization objective function of PLL: \( F_{oM} = \left( \frac{1}{\text{Power} \times \text{Locking Time}} \right) \).
## PLL: ABC Optimization: Poly. Vs NN

### Optimization Results

<table>
<thead>
<tr>
<th>FoM</th>
<th>Poly. Metammodel</th>
<th>ANN Metammodel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power</td>
<td>3.9 mW</td>
<td>3.9 mW</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.6909 GHz</td>
<td>2.7026 GHz</td>
</tr>
</tbody>
</table>

### Optimization Time Comparison

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Circuit Netlist</th>
<th>Poly. Metammodel</th>
<th>ANN Metammodel</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABC (100 iterations)</td>
<td>#bees(20) * 5 min * 100 iteration = 10,000 minutes = 7 days (worst case)</td>
<td>5 mins</td>
<td>0.12 mins</td>
</tr>
<tr>
<td>Metamodel Generation</td>
<td>0</td>
<td>11 hours for LHS + 1 min creation</td>
<td>11 hours for LHS + 10mins training and verification.</td>
</tr>
</tbody>
</table>
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Related Prior Research

Fast Design Exploration

- Neural Networks
  - Xia 2009
  - Wolfe 2003
  - Xu 2003

- Intelligent Algorithms
  - Delican 2010
  - Thakker 2009
  - Fernando 2008

- Macromodeling
  - Basu 2009
  - Ding 2006
  - Agarwal 2005

- Metamodeling
  - Samanta 2010
  - Lamecki 2008
  - Wong 2006

- Actual SPICE netlist
- Simplified SPICE
- Functions
Conclusions …

- Polynomial/nonpolynomial metamodels are explored.
- Use of metamodels and optimization algorithm speed up the design-space exploration for AMS circuits.
- LHS was identified as an accurate sampling method.
- Polynomial metamodels are easier create but can be applied for small circuits.
- 56% increase in accuracy is observed using feed forward NN over polynomial metamodels.
- On average 3.2% error is observed using NN.
Conclusions

- As a case study, a 180nm PLL, the circuit was parameterized with 21 parameters and optimized using the ABC algorithm.
- The final outcome of the design flow was 90% power savings and an average of 52% jitter minimization.
- Only 100 simulations are used to generate the accurate metamodels and ABC converged faster.
- An exhaustive search of the design space of 21 parameters with 10 intervals per parameter would require $10^{21}$ simulations. The time savings are enormous ($\approx 10^{20} \times$ SPICE simulation time).
Our Selected Publication on this Research


Future Research

- Capturing statistical process variations using metamodels
- Kriging metamodeling
  - Effective handle correlations
  - Accurately model process variations
- Integration in HDLs
  - Used for accurate behavioral simulations
- Application to MEMS/NEMS
  - Unified simulation and design exploration of heterogeneous components
Thank you !!!