DfX for Nanoelectronic Embedded Systems

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Computing Evolution
Ancient Computing Machines -- Mechanical

2400 BC
-- The abacus
-- The first known calculator
-- Invented in Babylonia

1832 AD
-- The Babbage Difference Machine
-- Tabulated polynomial functions
-- Invented in Britain
The First Electronic Computer

1946

-- ENIAC -- The first electronic general-purpose computer.
-- Turing-complete, digital, and programmable.
-- Invented in USA.
Current Computing Systems

- Desktop PC
- Laptop or Notebook PC
- Tablet
- Slate PC
- Smart Phone
Smallest Single-Board Computers

Raspberry Pi

BeagleBone
The Workhorses
Variety of Integrated Circuits or Chips?

- Low-Cost ASIC
- Communication Chip
- Secure Media Processor

Intel Core i7 LGA1366 processor has 1366 pins.

ADC Chip
Intel Haswell Chip -- 2013

4th Generation Intel® Core™ Processor Die Map

22nm Tri-Gate 3-D Transistors

Quad core die shown above  |  Transistor count: 1.4 Billion  |  Die size: 177mm²

** Cache is shared across all 4 cores and processor graphics
GPU with Highest Transistor Count

Nvidia GK110 has 7.1 billion transistors of a 28nm technology.

Processor for Mobile Systems: Essentially AMS-SoCs

NVIDIA’s Tegra 2 die
Source: http://www.anandtech.com

Snapdragon S4 Block Diagram
Source: http://www.cnx-software.com
The Drivers
- Technology Miniaturization (aka Technology Scaling)
- New Technology (Alternative Devices)
How Small in Nano??

- "nano" means one-billionth, or $10^{-9}$

- A sheet of paper is about 100,000 nanometers thick

- A human hair is approx. 100,000 nanometers wide

A Typical Nanoelectronic System

Heterogeneous components with millions of nanoscale devices.

High-K nano-CMOS

Triple Gate

Graphene Nanoribbon
Good and Bad, and DFX
Scaling Reduces Power Dissipation

1 Virtex-7 2000T = 4 Largest Monolithic FPGAs
19 Watts = 112 Watts

Source: http://low-powerdesign.com/sleibson
Scaling Reduces Cost of Electronics

In 1986: 1.3 megapixels CCD sensor Kodak camera was $13,000. You can buy now for few dollars.

Source: http://www.lensrentals.com/blog/2012/04/d7000-dissection

Nikon D7000 DSLR camera.

16 MP → $700
Nanoelectronics: Challenges

- Nanoelectronic Design Space
  - Power
  - Leakage
  - Delay
  - Area
  - Thermal
  - Reliability
  - Yield
  - Variability
  - Cost
  - Testability
  - Manufacturability
DfX -- Design for X  
(aka Design for Excellence)

X = set of IC design challenges
- **Manufacturability**
- **Power**
- **Variability**
- **Cost**
- **Yield**
- **Reliability**
- **Test**
- **Debug**

Source: ISVLSI 2012 Andrew Kahng Keynote
Design for Power (DfP)
Consumer Electronics Demand
More and More Energy

Energy consumption in homes by end uses
quadrillion Btu and percent

1993
- Total 10.01
  - Space heating: 24.0%
  - Air conditioning: 18.3%
  - Water heating: 4.6%

2009
- Total 10.18
  - Appliances, electronics, and lighting: 41.5%
  - Water heating: 17.7%
  - Space heating: 6.2%

Source: U.S. Energy Information Administration.

Quadrillion BTU (or quad): 1 quad = $10^{15}$ BTU ≈ 1.055 Exa Joule (EJ).
Different Electronic Systems: Common Story

- Smarter … Faster … High Throughput …

→ Power Hungry !! Battery Hungry !!

A green light to greatness:
Battery Dependency: Not Overstated

- Boeing 787’s across the globe were grounded in early 2013.

One 787 Battery:
12 Cells / 32 V DC

Source: [http://www.newairplane.com](http://www.newairplane.com)
Battery Dependency: Not Overstated

- **Great idea**: Smartwatch with functioning like smartphone.
- **Big Problem**: Battery life of one time charging is only 1 day.

Source: [http://www.businessinsider.com](http://www.businessinsider.com)
A Typical Electronic System: Where Energy Consumed??

Power of a Mobile System

- **WiFi**: 63%
- **Other**: 20%
- **CPU**: 7%
- **SDRAM**: 4%
- **Bluetooth**: 6%

Power dissipation breakdown in idle mode of a connected mobile device

Source: Pering MobiSys 2006
DfP: Possible Solution Fronts

Energy Efficient Portable Systems

- Energy Efficient Software
  - System
  - Application
- Energy Efficient Hardware
  - Digital
  - Analog
- Smart Battery
  - Mixed-Signal
DfP: Design of an Universal Level Converter for Dynamic Power Management
One Example Electronic System: Secure Digital Camera

- Lens / Shutter/Mirror
- Active Pixel Sensors
- Analog-to-Digital Converter
- Scratch Memory
- Liquid Crystal Display (User Interface)
- System Controller
- Encryption Unit
- Bar Code Unit
- Watermark Unit
- Compression Unit
- DSP
- USB Port
- Flash Storage

Power Management Unit (PMU)
Universal Voltage-Level Converter: One Topology

- 20 transistor area efficient design.
- Energy hungry transistors are circled.

- Energy hungry transistors have thicker oxide.
- 90nm CMOS dual-oxide physical design of ULC.
Universal Voltage-Level Converter: Operations

Operations of the ULC:

- Level-up conversion
- Level-down conversion
- Blocking of input signal

<table>
<thead>
<tr>
<th>Select Signal</th>
<th>Type of Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Block Signal</td>
</tr>
<tr>
<td>0</td>
<td>Up Conversion</td>
</tr>
<tr>
<td>1</td>
<td>Down Conversion</td>
</tr>
</tbody>
</table>

![Diagram showing input, upconverted voltage, and downconverted voltage]
## Universal Voltage-Level Converter: Has Minimal Overhead

<table>
<thead>
<tr>
<th>Designs</th>
<th>Technology (nm)</th>
<th>Power</th>
<th>Delay</th>
<th>Conversion</th>
<th>Design Approach</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ishihara 2004</td>
<td>130nm</td>
<td>---</td>
<td>127 ps</td>
<td>Level-up and down</td>
<td>Level converting flip flops</td>
</tr>
<tr>
<td>Yu 2001</td>
<td>350nm</td>
<td>220.57 µW</td>
<td>---</td>
<td>Level-up</td>
<td>SDCVS</td>
</tr>
<tr>
<td>Sadeghi 2006</td>
<td>100nm</td>
<td>10 µW</td>
<td>1 ns</td>
<td>Level-up</td>
<td>Pass transistor and Keeper transistor</td>
</tr>
<tr>
<td>ULC</td>
<td>90 nm</td>
<td>12.26 µW</td>
<td>113.8 ps</td>
<td>Level-up/down and block</td>
<td>All conversion types and Programmable</td>
</tr>
</tbody>
</table>
Design for Variability (DfV)
Nanoelectronics Variability?

- Discrepancy between the chip parameters -- Design Time versus Actual Post Fabrication

Source: [http://apcmag.com/picture-gallery-how-a-chip-is-made.htm](http://apcmag.com/picture-gallery-how-a-chip-is-made.htm)
Source–drain resistance is different for different chips in a same die.

Gate-to-source and gate-to-drain overlap capacitance is different for different chips in a same die.

Process Variation: The Impact

• Yield Loss
• Reliability Issue
• Higher Cost
Process Variation: Sources

- oxidation
- photoresist removal (ashing)
- photoresist coating
- stepper exposure
- process step
- spin, rinse, dry
- acid etch
- optical mask
- photoresist development

Sophisticated Lithography
Process Variations : Solution

Customer Specifications

- System Design
  - Architecture Design
    - Logic Design
      - Circuit Design
        - Physical Design

Silicon Specifications

- Silicon Ingot
  - Slicing
    - Blank Wafers
      - Lithography
        - Etching, Deposition
          - Wafer with circuit printed

Feedback for DfV
Process Variations Aware Optimization: Key Idea

Histograms

Standard-Deviation ($\sigma$)

Power / Performance Values

A green light to greatness.
DfV: Statistical Nano-CMOS RTL Optimization for Power
Nano-CMOS RTL Statistical Optimization

Input Generation Engine

Compilation

Transformation

DFG

Behavioral Scheduling

Resource Allocation and Binding

Datapath and Control Generation Engine

Power Delay Estimation Engine

Characterization Engine

Process Parameter Extractor

Resource Table

Process Variation Engine

Output Generation Engine

RTL Description
Statistical RTL Optimization: Formulation

Minimize: $FOM_{Total}^{DFG} \left( \mu_I^{DFG}, \sigma_I^{DFG} \right)$

Subjected to (Resource/Time Constraints):

Allocated $(FU_{k,i}) \leq$ Available $(FU_{k,i})$, $\forall$ cycle $c$

$D_{CP}^{DFG} \left( \mu_D^{DFG}, \sigma_D^{DFG} \right) \leq D_{Con} \left( \mu_D^{Con}, \sigma_D^{Con} \right)$
Statistical RTL Optimization: Results on DSP Benchmarks

(For ARF Benchmark)

(For BPF Benchmark)
Design for Cost ($) (DfC)
Chip Cost

Total Chip Cost

Non-recurring (NRE)
- Design
- Plant Capitalization
- Masks

Recurring
- Fabrication
- Packaging
- Testing

Non-recurring (NRE)
- $0.5B
- $5B
- $2M

Source: http://www.ami.ac.uk/courses/ami4202_mdesign/u02/
One of the Key Issues: Time/Effort

- The simulation time for a Phase-Locked-Loop (PLL) lock on a full-blown (RCLK) parasitic netlist is of the order of many days! → High NRE cost.

- Issues for AMS-SoC components:
  - How fast can design space exploration be performed?
  - How fast can layout generation and optimization be performed?
Standard Design Flow – Very Slow

- Standard design flow requires multiple manual iterations on the back-end layout to achieve parasitic closure between front-end circuit and back-end layout.
- Longer design cycle time.
- Error prone design.
- Higher non-recurrent cost.
- Difficult to handle nanoscale challenges.
Automatic Optimization on Netlist
(Faster than manual flow; still slow)

- Automatic iteration over netlist improves design optimization.
- Still needs multiple simulations using analog simulator (SPICE).
- SPICE is slow.
Two Tier Speed Up Through Metamodel

Baseline Mixed-Signal Circuit Layout-Aware Netlist

Metamodels of Baseline Mixed-Signal Circuit

9000x Speedup

Optimization over Metamodels

300x Speedup

Traditional – Slow Approach

Technology Constraints

Specification Constraints
Proposed Flow: Key Perspective

- Novel design and optimization methodology that will produce robust AMS-SoC components using ultra-fast automatic iterations over metamodels (instead of netlist) and two manual layout steps.
- The methodology easily accommodates multidimensional challenges, reduces design cycle time, improves circuit yield, and reduces chip cost.
Metamodel-Based Design Flow

Input Specifications of the Mixed-Signal IC

Create Logical Design → Mixed-Signal Design Schematic

Specifications met? (Yes/No)

Create Layout of the Mixed-Signal IC → Mixed-Signal Design Layout

Perform DRC/LVS/RCLK Extraction → Parasitic-Aware Mixed-Signal IC Netlist

Specifications met? (Yes/No)

Parameterize the Parasitic-Aware Netlist with Design Variables → Parasitic-Aware Parameterized Mixed-Signal IC Netlist

Perform Fast and Accurate Sampling of Mixed-Signal IC Design Space → Sampled Data Points for Metamodel Generation

Create Metamodels of Figures-of-Merits of the Mixed-Signal IC → Metamodels of the FoMs of the Mixed-Signal IC

Use an Algorithm to Perform Optimization Over Polynomial Metamodels → Optimal Physical-Design Variables

Specifications met? (Yes/No)

Create New Layout of the Mixed-Signal IC → Optimized Mixed-Signal IC Layout

Done

A green light to greatness
Metamodels: Selected Types

Nanoscale-CMOS Circuit Metamodels

Polynomial
- Regular Polynomial
- Piece-wise Polynomial

Nonpolynomial
- Artificial Neural Networks
- Kriging Methods
Metamodels: Polynomial Example

Actual Circuit (SPICE netlist) of AMS-SoC Components

Statistical Sampling

Polynomial Function Fitting

\[ f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p. \]
Sampling Techniques: 45nm Ring Oscillator Circuit (5000 points)

Monte Carlo

MLHS

LHS

DOE
Polynomial Metamodels

- The generated sample data can be fitted in many ways to generate a metamodel.
- The choice of fitting algorithm can affect the accuracy of the metamodel.
- A simple metamodel has the following form:

\[ y = \sum_{i,j=0}^{k} \left( \alpha_{ij} \times x_1^i \times x_2^j \right) \]

- \( y \) is the response being modeled (e.g. frequency), \( x = [W_n, W_p] \) is the vector of variables and \( \alpha_{ij} \) are the coefficients.
## Metamodel: Polynomial Comparison

<table>
<thead>
<tr>
<th>Case Study Circuits</th>
<th>Polynomial Order</th>
<th>( \mu ) error (in MHz)</th>
<th>( \sigma ) error (in MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ring Oscillator</strong></td>
<td>1</td>
<td>571.0</td>
<td>286.7</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>195.4</td>
<td>78.1</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>37.2</td>
<td>18.0</td>
</tr>
<tr>
<td><strong>45nm CMOS</strong></td>
<td>4</td>
<td>20.0</td>
<td>10.7</td>
</tr>
<tr>
<td><strong>Target ( f ): 10GHz</strong></td>
<td>5</td>
<td>17.1</td>
<td>9.6</td>
</tr>
<tr>
<td><strong>LC-VCO</strong></td>
<td>1</td>
<td>42.3</td>
<td>40.1</td>
</tr>
<tr>
<td><strong>180nm CMOS</strong></td>
<td>2</td>
<td>39.4</td>
<td>37.8</td>
</tr>
<tr>
<td><strong>Target ( f ): 2.7GHz</strong></td>
<td>3</td>
<td>35.4</td>
<td>33.9</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>30.5</td>
<td>29.3</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>26.5</td>
<td>25.2</td>
</tr>
</tbody>
</table>

**Ring oscillator – Order 1**

\[
f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p.
\]

**LC-VCO – Order 1**

\[
f(W_n, W_p) = 2.38 \times 10^9 - 3.49 \times 10^{12} W_n - 6.66 \times 10^{12} W_p.
\]
Feed-forward dual layer (FFDL) ANNs are considered.

FFDL ANN created for each FoM:

- Nonlinear hidden layer functions are considered each varying hidden neurons 1-20:

\[ b_j(v_j) = \tanh(\lambda v_j) \]
Metamodel Comparison: Polynomial Vs Nonpolynomial

- Nonpolynomial (Artificial Neural Network) is more suitable for large circuits.

180nm CMOS PLL with Target Specs: \( f = 2.7\text{GHz}, P = 3.9\text{mW}, 8.5\mu\text{s}. \)

<table>
<thead>
<tr>
<th>Figures-of-Merits (FoM)</th>
<th>Polynomial</th>
<th>Nonpolynomial (Neural Network)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of Coefficients</td>
<td>RMSE</td>
</tr>
<tr>
<td>Frequency</td>
<td>48</td>
<td>77.96 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>50</td>
<td>2.6mW</td>
</tr>
<tr>
<td>Locking Time</td>
<td>56</td>
<td>1.9\mu\text{s}</td>
</tr>
</tbody>
</table>

- 56% increase in accuracy over polynomial metamodels.
- On average 3.2% error over golden design surface.
Selected Algorithms for Optimization over Metamodels

Algorithms Applied Over Metamodels

Traditional Heuristics
- Simulated Annealing
- Tabu Search

Intelligent Algorithms
- Artificial Bee Colony (ABC)
- Ant Colony
Exhaustive Search: 45nm RO

- Searches over two parameter space.
- Parameters incremented over specified steps.
- Search space is recursively divided into rectangles and each time the rectangle with superior result is selected.
Comparison of the Running Time of Heuristic Algorithms: 45nm RO

- **Optimization without metamodels**: the tabu search optimization is faster by $\sim 1000 \times$ than the exhaustive search and $\sim 4 \times$ faster than the simulated annealing optimization.

- **Optimization with metamodels**: the simulated annealing optimization is faster by $\sim 1000 \times$ than the exhaustive search and $\sim 6 \times$ faster than the tabu search optimization.
Case Study Circuit: 180nm PLL

- PLL circuit is characterized for frequency, power, vertical and horizontal jitter (for simple phase noise), and locking time.
- Metamodels are created for each FoM from same sample set.
PLL: Polynomial Metamodels ...

- The number of coefficients corresponding to the order of the generated metamodel for settling time.
- This means that the model is over fitted, therefore for the metamodel that represents settling time, a polynomial order of 4 will be used.
Artificial Bee-Colony: Overview

1. **Initial** food sources are produced for all worker bees.

2. **Do**
   1) Each worker bee goes to a food source and evaluates its nectar amount.
   2) Each onlooker bee watches the dance of worker bees and chooses one of their sources depending on the dances and evaluates its nectar amount.
   3) Determine abandoned food sources and replace with the new food sources discovered by scout bees.
   4) Best food source determined so far is recorded.

3. **While** (requirements are met)

   A food source $\rightarrow$ a solution; A position of a food source $\rightarrow$ a design variable set; Nectar amount $\rightarrow$ Quality of a solution; Number of worker bees $\rightarrow$ number of quality solutions.
An exhaustive search of the design space of 21 parameters with 10 intervals per parameter requires $10^{21}$ simulations.

$10^{21}$ SPICE simulations is slow; 10min per one.

$10^{21}$ simulations using polynomial metamodels is fast.

Time savings: $\approx 10^{20} \times$ SPICE simulation time.
PLL: ABC Optimization: Poly Vs ANN

### Optimization Results

<table>
<thead>
<tr>
<th>FoM</th>
<th>Poly. Metamodell</th>
<th>ANN Metamodell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power</td>
<td>3.9 mW</td>
<td>3.9 mW</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.6909 GHz</td>
<td>2.7026 GHz</td>
</tr>
</tbody>
</table>

### Optimization Time Comparison

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Circuit Netlist</th>
<th>Poly. Metamodell</th>
<th>ANN Metamodell</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABC (100 iterations)</td>
<td>#bees(20) * 5 min * 100 iteration = 10,000 minutes = 7 days (worst case)</td>
<td>5 mins</td>
<td>0.12 mins</td>
</tr>
<tr>
<td>Metamodel Generation</td>
<td>0</td>
<td>11 hours for LHS + 1 min creation</td>
<td>11 hours for LHS + 10mins training and verification.</td>
</tr>
</tbody>
</table>
Conclusions

- Nanoelectronic circuits and systems have multifold design challenges.
- DfX is design for X – Power, Variability, Cost …
- DfP:
  - 35% of total energy in USA is consumed by electronics.
  - Battery is an critical constraint for portable systems.
  - Energy efficient hardware, software at the same time better battery design needed for effective solutions.
- DfV: Reduce the variability in chip and enhance yield.
- DfC: Reduce NRE, yield, and time to market.
- Much more research is needed for combined consideration of issues, e.g. X ← Variability and Cost
References


Thank You !!!

Slides Available at:
http://www.cse.unt.edu/~smohanty