Geostatistics Inspired Fast Layout Optimization of Nanoscale CMOS Phase Locked Loop

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Presented By
Oghenekarho Okobiah
Outline of the talk

- Background and Motivation
- Related Prior Research
- Geostatistics Based Metamodelling
- Proposed Design Flow and GSA Optimization
- Case Study Circuit and Experimental Setup
- Results
- Conclusions
Background and Motivation

- Computer simulations are expensive
- Pronounced effects of process variations in deep nanometer regions
  - Increase in number of design parameters
  - Current modeling techniques not effective at capturing effects of process variation
- Complex and high density designs
- Designs for low power consumption
Novel Contributions

- Exploring Kriging for high dimensional metamodeling
- Design flow methodology
  - Kriging metamodeling and gravitational search algorithm optimization.
Prior Related Research

- Exploration of optimization algorithms for NanoCMOS designs
- Kriging Based Techniques
  - O. Okobiah --- simple and ordinary kriging metamodels
  - G. Yu --- re-iterative Pareto fronts
  - H. You --- kriging metamodeling
Fundamentals of Kriging

- Originally used in geostatistics for mining purposes.
  
  \[ y(x_0) = \sum_{j=1}^{L} \lambda_j B_j(x) + z(x), \]  

- Each point is predicted based on a set of unique weights (\( \lambda_j \)).
  
  \[ \sum_{j=1}^{n} \lambda_j = 1. \]
Fundamentals of Kriging...

\[
\begin{pmatrix}
\lambda_1 \\
\vdots \\
\lambda_n \\
\mu
\end{pmatrix}
= \Gamma^{-1}
\begin{pmatrix}
\gamma(x_1, x_0) \\
\vdots \\
\gamma(x_n, x_0) \\
1
\end{pmatrix},
\] (3)

\[
\Gamma =
\begin{pmatrix}
\gamma(x_1, x_1) & \cdots & \gamma(x_1, x_n) & 1 \\
\vdots & \ddots & \vdots & \vdots \\
\gamma(x_n, x_1) & \cdots & \gamma(x_n, x_n) & 1 \\
1 & 1 & \gamma(x_n, x_n) & 0
\end{pmatrix},
\] (4)

\[
\widehat{P}_{PLL}(Wn_0) = \sum_{j=1}^{L} \lambda_j B_j(wn) + \varepsilon(wn),
\] (7)
Gravitational Search Algorithm

- Part of swarm Intelligence family
  - population based heuristic algorithms
- Based on gravitational laws of attraction and motion

\[
F_{ij}^d(t) = G(t) \frac{M_{pi}(t) \times M_{aj}(t)}{R_{ij}(t) + \epsilon} (x_j^d(t) - x_i^d(t)),
\]

where \( F_{ij}^d(t) \) is design objective, \( M \) is the quality of solution at search location \( i \) or \( j \), \( x_i \) is the set of design parameters at location \( i \).
Gravitational Search Algorithm

Design Space

- $M_w$
- $F_{wy}$
- $F_{xy}$
- $a_y$
- $M_y$
- New $M_y$
- $F_{yz}$
- $F_{xz}$
- $M_x$
- $M_z$
- Best solution so far
Gravitational Search Algorithm

Start

Generate initial search agent \((W_n, W_p)\)

Evaluate objective of interest (power)

Optimization or Termination criteria met?

Best Solution

End

Calculate velocity and update agent location (new \(W_n, W_p)\)

Rank quality of solution

Update gravity constant and calculate attraction

Update mass of each location
Case Study Circuit: 180nm PLL

Fig. 3. System level diagram of the PLL

Fig. 4. 180nm layout of the PLL
Proposed Design Flow

1. Input Specifications of PLL Design
2. Create Logical Design
   - Specifications met?
     - no: Create Layout of PLL
     - yes: PLL Design Schematic
3. Perform DRC/LVS/RLCK Extraction
   - Paraphitic-Aware PLL Netlist
4. Specifications met?
   - no: Parameterize the parasitic-aware netlist!
     - Parameterized Parasitic-Aware PLL Netlist
     - Perform LHS sampling of Design Space
       - Sample Points for Metamodel generation
     - Generate Kriging metamodels
       - Metamodels for PLL Design
     - Use GSA for optimization
       - Optimal design variables
     - Create New Layout for Final Design
       - Optimized PLL design
   - yes: Done
Design Flow Components

- Design and netlist optimization
  - Baseline design
    - (schematic and layout)
  - Extract parasitic netlist

Design Flow Diagram:

1. Input Specifications of PLL Design
2. Create Logical Design
3. Specifications met?
   - No: Continue
   - Yes: Create Layout of PLL
4. Perform DRC/LVS/RLCK Extraction
5. Specifications met?
   - No: Parameterize the parasitic-aware netlist
   - Yes: Parameterized Parasitic-Aware PLL Netlist
6. Perform LHS sampling of Design Space
7. Generate Kriging metamodels
8. Use GSA for optimization
9. Create New Layout for Final Design
10. Done
**Design Flow Components**

- **Sampling and Metamodel Generation**
  - Parameterize parasitic netlist
    - Identify performance objectives
  - LHS sampling
    - L, W as sampling corners
  - Process variation
  - Metamodel for each design objective is generated
    - Using mGstat (MATLAB Kriging tool)
  - Design objectives are functions of design parameters
    - e.g. $P_{PLL}(W_n) = \sum_{j=1}^{L} \lambda_j B_j(w_n) + z(w_n)$, (7)
Design Flow Components

- Design Optimization
  - Kriging metamodels optimized with GSA algorithm
  - Conflicting design objectives used as goal and constraint
  - Final physical design is drawn
## Experimental Results

### TABLE III
**OPTIMIZED PARAMETER VARIABLES**

<table>
<thead>
<tr>
<th>PLL Components</th>
<th>Parameter</th>
<th>Min (m)</th>
<th>Max (m)</th>
<th>Optimal (m)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$W_{PD1}$</td>
<td>400n</td>
<td>2µ</td>
<td>1.53µ</td>
</tr>
<tr>
<td></td>
<td>$W_{PD1}$</td>
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<td>2µ</td>
<td>0.95µ</td>
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<td>$W_{PD1}$</td>
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<td>Phase Detector</td>
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<td>Charge Pump</td>
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<td>LC-VCO</td>
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<td>0.43µ</td>
</tr>
</tbody>
</table>

### Metric | Value
---|---
RMSE | $6.46 \times 10^{-10}$
$R^2$ | 0.9959

<table>
<thead>
<tr>
<th>Metric</th>
<th>Power (mW)</th>
<th>Locking Time (ns)</th>
<th>Area (µm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline Design</td>
<td>8.27</td>
<td>2.74</td>
<td>525 x 326</td>
</tr>
<tr>
<td>Optimal Design</td>
<td>1.67</td>
<td>2.63</td>
<td>525 x 326</td>
</tr>
<tr>
<td>Reduction</td>
<td>79 %</td>
<td>4 %</td>
<td>0 %</td>
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</table>
Experimental Results

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</tbody>
</table>

Fig. 5. Optimization Steps of the PLL
## Related Comparison

<table>
<thead>
<tr>
<th>Research</th>
<th>Test Circuits</th>
<th>Metamodeling Technique</th>
<th>Accuracy</th>
<th>Optimization Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>You</td>
<td>Integrated Op-Amp</td>
<td>Kriging</td>
<td>0.5658</td>
<td>-</td>
</tr>
<tr>
<td>Yu</td>
<td>Ring Oscillator</td>
<td>Kriging</td>
<td>0.5325% (MSE)</td>
<td>-</td>
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<tr>
<td></td>
<td>LC-VCO</td>
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<td>0.5563% (MSE)</td>
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<td>Okobiah</td>
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<td>Kriging</td>
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<td>Garitselov</td>
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<td>Polynomial</td>
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<td>ABC</td>
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<td>0.5658</td>
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<td>This work</td>
<td>PLL</td>
<td>Kriging</td>
<td>6.46 x10^-9</td>
<td>GSA</td>
</tr>
</tbody>
</table>
Conclusions

- A novel design flow methodology was presented
  - Incorporating Kriging metamodeling
  - Demonstrating GSA algorithm based optimization
- Optimized PLL power by 79%
Thank you !!!