Dopingless Transistor based Hybrid Oscillator Arbiter Physical Unclonable Function

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Outline of the talk

- IoT and Attacks
- Novel Contributions
- Physical Unclonable Functions
- Proposed Designs of Physical Unclonable Function
- Results and FoMs
- Conclusion and Future Research
In the IoT era, the number of devices connected to the internet is exponentially increasing.
Security in the Internet of Things

Secure Network under lock and key
Security in the Internet of Things
Novel Contributions

- Two designs of Hybrid Oscillator Arbiter Physical Unclonable Functions are implemented using DL-FETs.
- Comparative analysis with FinFETs is presented for the same designs.
- To the authors’ best knowledge, this is the first paper using DL-FETs.
Technology Scaling

90nm CMOS → 32nm CMOS → 14nm FinFET

CMOS

FinFET
Dopingless Transistor

Structure of Dopingless FET

Symbols of n-type and p-type Dopingless FET
Dopingless Transistor

• An undoped single uniform structure is used from source to drain.
• In the DL-FET, a thin intrinsic silicon nanowire is used between metal electrodes and gate, source and drain regions.
• The p-type and the n-type doping regions can be formed using work function engineering inside the undoped thin silicon.
<table>
<thead>
<tr>
<th>Parameters</th>
<th>Dopingless FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Film Thickness ($T_{Si}$)</td>
<td>10 nm</td>
</tr>
<tr>
<td>Effective Oxide Thickness (EOT)</td>
<td>1 nm</td>
</tr>
<tr>
<td>Gate Length ($L_g$)</td>
<td>20 nm</td>
</tr>
<tr>
<td>Width (W)</td>
<td>1 $\mu$m</td>
</tr>
<tr>
<td>Source/Drain extension</td>
<td>10 nm</td>
</tr>
<tr>
<td>Metal work function/doping for source/drain</td>
<td>3.9 EV (Hafnium)</td>
</tr>
<tr>
<td>Metal work function/doping for gate</td>
<td>4.66 eV (TiN)</td>
</tr>
<tr>
<td>Doping</td>
<td>$10^{15}/cm^3$</td>
</tr>
</tbody>
</table>
Physical Unclonable Functions are simple primitives for security.

- PUFs are easy to build and impossible to duplicate (theoretically).

- Input and Output are called Challenge Response Pair.

```
Challenge (C) (100111....0)  
PUF                                          Response (R) (0011101....1)
```
How PUF Works

With the same input to different copies of the same circuit, different outputs are obtained, each unique to each circuit.
How PUF Works

Process Variation

Mismatch Variation
Types of PUF

Based on number of unique challenges

- Strong PUF
  - Optical PUF
  - Arbiter PUF
- Weak PUF
  - RO PUF
  - SRAM PUF
DL-FET Based Conventional RO PUF
Speed Optimized Hybrid Oscillator Arbiter PUF
Power Optimized Hybrid Oscillator Arbiter PUF
Figure of Merits

- **Hamming Distance**: The hamming distance between two keys should be 50%.

- **Reliability**: If the same PUF is run with the same challenge input, with environment variations, the output key should not change – Hamming distance should be 0.

- **Average Power consumption**.
Frequencies of Ring Oscillators

Number of runs

Number of Ring Oscillators

Frequency (Hz)

×10^{-11}
Inter PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF
Inter PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF
Intra PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF
Intra PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF
Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF
Average Power of Power Optimized Hybrid Oscillator Arbiter PUF
## Characterization Table for PUF Designs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FinFET</th>
<th>Dopingless Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power</td>
<td>175.5 μW</td>
<td>121.3 μW</td>
</tr>
<tr>
<td>Hamming Distance</td>
<td>50.1 %</td>
<td>48</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Speed Optimized Hybrid Oscillator Arbiter PUF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power</td>
<td>251.5 μW</td>
</tr>
<tr>
<td>Hamming Distance</td>
<td>48.3 %</td>
</tr>
</tbody>
</table>

Dopingless Transistor
# Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF

<table>
<thead>
<tr>
<th>Research Works</th>
<th>Technology</th>
<th>Architecture Used</th>
<th>Average Power Consumed</th>
<th>Hamming Distance (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rahman et al. [23]</td>
<td>90nm CMOS</td>
<td>--</td>
<td>--</td>
<td>50</td>
</tr>
<tr>
<td>Maiti et al. [19]</td>
<td>180nm CMOS</td>
<td>Traditional Ring Oscillator</td>
<td>--</td>
<td>50.72</td>
</tr>
<tr>
<td>Suh et al. [24]</td>
<td></td>
<td></td>
<td></td>
<td>46.15</td>
</tr>
<tr>
<td>Maiti et al. [18]</td>
<td></td>
<td></td>
<td></td>
<td>47.31</td>
</tr>
<tr>
<td>Yanambaka et al. (Power Optimized)[20]</td>
<td>32nm FinFET</td>
<td>Current Starved Oscillator</td>
<td>175.5 µW</td>
<td>50.1</td>
</tr>
<tr>
<td>Yanambaka et al. (Power Optimized)[10]</td>
<td>32nm FinFET</td>
<td>Traditional Ring Oscillator</td>
<td>285.5 µW</td>
<td>50.9</td>
</tr>
<tr>
<td><strong>This paper (Power Optimized)</strong></td>
<td>10 nm Dopingless FET</td>
<td>Hybrid Oscillator Arbiter</td>
<td>121.3 µW</td>
<td>48.0</td>
</tr>
<tr>
<td><strong>This paper (Speed Optimized)</strong></td>
<td>10nm Dopingless FET</td>
<td>Hybrid Oscillator Arbiter</td>
<td>151 µW</td>
<td>50.0</td>
</tr>
</tbody>
</table>
Conclusion and Future Research

- This paper presents two designs of hybrid oscillator arbiter PUFs, a speed optimized and a power optimized design using DL-FETs.
- A fair comparison of the two technologies, FinFET and DL-FETs is presented to show the power reduction using these transistors.
- As a future research, an ultra low power design of PUF can be implemented.
THANK YOU