Lecture 8: Process Variation Tolerant Sense Amplifier Design

CSCE 6933/5933

Advanced Topics in VLSI Systems

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Outline

• Introduction
• Related Prior Research
• Functional Design of Sense Amplifier Circuits
• Design Optimization – Dual Oxide Technique
• Design Optimization – Dual Threshold Voltage Technique
• Conclusions
Introduction

• Dynamic Random Access Memories (DRAMs) are important parts of computing systems
• Relatively fast but not as fast as SRAMs
• Densely Packed
  – 4 times denser than SRAM
• Memory Hierarchy

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Motivation

- Memory keeps lagging CPU speed performance
Introduction: Background

- Historical background
- 1K DRAM designed in 1970
  - Used 3-T cells
- 4Kb – 64Mb DRAM
  - Used 1T-1C cells
  - CMOS technology
  - Multiplexed addressing
- Gb-SDRAM Era (Current Technology)
  - Access synchronized with master clock
Background

• Basic Organization of DRAM
Memory Array

- Memory cells of a folded bitline array

- The word line selects a whole row of cells
- The bit line reads and writes the capacitor
- The sense amplifier connects two columns, one serves as a reference cell
- All columns are active on a row access
Sense Amplifier: Background and Operation

• Major Functionality:
  • Detect and amplify voltage change
  • Refresh circuit
  • Act as column buffers

• Basic Access Operations
  • To access (read or write to a cell) there are three basic operations performed – the precharge, row and column access.
  • The precharge phase charges all bitlines to a determined voltage, usually $V_{DD}/2$. 
Sense Amplifier: Background and Operation

• For a read operation,
  – The row access activates the wordline of the cell and all the capacitors begin to share charge with the bitlines.
  – Sense amplifiers sense and magnify voltage changes.
  – The data from the sense amplifier is selected by the column bit during the column access.

• Write Operation.
  – The row access activates the wordlines.
  – The bitline drives the cell to a “0” or “1” depending on the value to be written.

• Refresh Operation: This is done by reading every address of the DRAM.
Issues in Nanoscale DRAM Circuit Design

- Variability: Variability in process and design parameters becomes more acute due to scaling technologies and processes.
- Leakage: Leakage is increasing due to scaling of oxide thickness.
- Power Consumption: Current leakage increases the static power consumption.
Process Variation

- Process variations occur due to different manufacturing environments and process difficulty.
- The effects of the process variation result in varying device parameters including:
  - supply voltage,
  - threshold voltages,
  - oxide thickness,
  - transconductance,
  - channel lengths,
  - channel widths, and
  - source and drain doping concentration.
Process Variations Classifications

Global Variations

- Fabrication Process: From plant to plant
- Lot Process: From lot to lot in a plant
- Wafer Process: From wafer to wafer in a lot
Salient Points of this Design Flow

• Analysis of effects of device parameters on FoMs of a sense amplifier.
• Analysis of effect of process variation on the performance of full latch sense amplifier.
• Design process to limit the effects of process variations with optimizations to FoMs.
• Exploring dual-Tox and dual-Vth for sense amplifier optimization.
### Related Prior Research

<table>
<thead>
<tr>
<th>Research</th>
<th>Parameter</th>
<th>Feature</th>
<th>Approach</th>
<th>Result Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sherwin</td>
<td>$V_{DD}$</td>
<td>Voltage gain</td>
<td>Physical measurements</td>
<td>-</td>
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<tr>
<td>Chow</td>
<td>$C_{BL}$</td>
<td>Sense Speed</td>
<td>Spice simulations</td>
<td>Sense speed – 40%</td>
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<tr>
<td>Laurent</td>
<td>$C_{BL}$, $V_{th}$, $\beta$</td>
<td>Signal Margin</td>
<td>Spice Simulations</td>
<td>-</td>
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<tr>
<td>Vollrath</td>
<td>$C_{BL}$, $V_{th}$, $\beta$</td>
<td>Signal Margin</td>
<td>Physical measurements</td>
<td>-</td>
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<td>Choudhary</td>
<td>$V_{th}$, $L$, $W$</td>
<td>Yield</td>
<td>Monte Carlo analysis</td>
<td>Improved Yield</td>
</tr>
<tr>
<td>Hong</td>
<td>-</td>
<td>Sense scheme</td>
<td>Spice simulations</td>
<td>Improved sense amplifier cell ration</td>
</tr>
<tr>
<td>Singh</td>
<td></td>
<td>SE rise time</td>
<td>Spice simulations</td>
<td>Eliminated offset voltage</td>
</tr>
<tr>
<td>This research</td>
<td>Dual-$V_{th}$</td>
<td>Process variability</td>
<td>Optimization</td>
<td>Sense delay – 80.2% Sense margin – 61.9%</td>
</tr>
</tbody>
</table>
Sense Amplifiers Topologies

• Voltage Based Sense Amplifiers
  – Sense and amplify a small differential voltage
  – Variations include cross couple and full latch cross couple

• Current Based Sense Amplifiers
  – Sense and amplify small differential currents
  – Lower input capacitance
  – Includes current-mirror, clamped bitline current amplifier
Functional Design of Sense Amplifier

- Two cross coupled inverters
- The major parts of the full latch voltage sense amplifier are
  - Nsense Amps
  - Psense Amps
  - Precharge and Equalization Circuits
Nsense and Psense Amplifiers

- Nsense amplification

- Psense amplification

- Nsense amplifiers activated by SE through N3
- N2 begins to conduct and eventually pulls $V_{bl}$ to ground

- Psense amplifiers activated by SEbar through P1
- P2 begins to conduct and eventually pulls $V_{bl}$ to ground
When PRE signal goes high, Vbl and Vblbar are charged to VDD/2 through M1 and M2. Psense amplifiers activated by P1.

- M3 Helps to speed up the process
Functional Design of Sense Amplifier

Equations for Charge Sharing

\[ \Delta V = \frac{C_S}{C_S + C_{BL}} \left( V_{CS} - \frac{V_{DD}}{2} \right) \]

when bit cell value is 1, \( V_{CS} = V_{DD} - V_{th} \)

\[ \Delta V \approx \frac{C_S}{C_{BL}} \left( \frac{V_{DD}}{2} - V_t \right) \]

when bit cell value is 1, \( V_{CS} = 0 \)

\[ \Delta V \approx -\frac{C_S}{C_{BL}} \left( \frac{V_{DD}}{2} \right) \]
Physical Layout for 45nm Sense Amplifier
Waveform Simulation

Sensing Waveform

- BL
- BLBAR

Sense "0"

VDD/2

Sense "1"

Signal Control

- WL
- PRE
- SE

Volt(V)

0 50 100 150 200 250
time(ns)

Volt(V)

0 0.5 1 1.5
time(ns)
Figures of Merit

- Precharge and Equalization Time
- Average Power Consumption
- Sense Delay
- Sense Margin

Table for Figures of Merit Characterization

<table>
<thead>
<tr>
<th>FoM</th>
<th>Precharge</th>
<th>Power</th>
<th>Sense Delay</th>
<th>Sense Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>7.50 ns</td>
<td>153.101 mW</td>
<td>4.39 ns</td>
<td>43.46 mV</td>
</tr>
</tbody>
</table>
Parametric Analysis

The following parameters analysed

- Gate Lengths and Widths \((L_n, L_p, W_n, W_p)\)
- Voltage Supply \((V_{DD})\)
- Cell Capacitance \((C_S)\)
- Bitline Capacitance \((C_{BL})\)
- Oxide Thickness \((T_{oxn}, T_{oxp})\)
- Threshold Voltage \((V_{thn}, V_{thp})\)
Sensitivity of FoMs on Ln

- **Precharge time with Ln Variation**
- **Power consumption with Ln Variation**
- **Sense delay with Ln Variation**
- **Sense margin with Ln Variation**

**Labels:**
- Low
- High

**Axes:**
- Ln (nm)
- Time (ns)
- Power (nw)
- Voltage (mV)
Sensitivity of FoMs on Lp

1. **Precharge time with Lp Variation**
   - Graph showing time (ns) on the y-axis and Lp (nm) on the x-axis.
   - Two lines indicate low and high scenarios.

2. **Power consumption with Lp Variation**
   - Graph showing power (nw) on the y-axis and Lp (nm) on the x-axis.
   - A single line shows the trend with Lp variation.

3. **Sense delay with Lp Variation**
   - Graph showing time (ns) on the y-axis and Lp (nm) on the x-axis.
   - A single line shows the constant time for low and high scenarios.

4. **Sense margin with Lp Variation**
   - Graph showing voltage (mV) on the y-axis and Lp (nm) on the x-axis.
   - A single line shows a constant voltage for low and high scenarios.
Sensitivity of FoMs on Wn

Precharge time with Wn Variation

Power consumption with Wn Variation

Sense delay with Wn Variation

Sense margin with Wn Variation
Sensitivity of FoMs on Wp

Precharge time with Wp Variation

Power consumption with Wp Variation

Sense delay with Wp Variation

Sense margin with Wp Variation

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### Summary of Effects of Parameter Variations on FoMs

- **Table of Parameter Variations**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Precharge</th>
<th>Power</th>
<th>Sense Delay</th>
<th>Sense Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_n$</td>
<td>decrease</td>
<td>increase</td>
<td>mild decrease</td>
<td>mild increase</td>
</tr>
<tr>
<td>$L_p$</td>
<td>increase</td>
<td>decrease</td>
<td>mild decrease</td>
<td>mild decrease</td>
</tr>
<tr>
<td>$W_n$</td>
<td>decrease</td>
<td>increase</td>
<td>decrease</td>
<td>decrease</td>
</tr>
<tr>
<td>$W_p$</td>
<td>increase</td>
<td>increase</td>
<td>mild decrease</td>
<td>decrease</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>decrease</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
</tr>
<tr>
<td>$C_S$</td>
<td>increase</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
</tr>
<tr>
<td>$C_{BL}$</td>
<td>increase</td>
<td>increase</td>
<td>mild increase</td>
<td>decrease</td>
</tr>
<tr>
<td>$V_{thn}$</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
<td>mild decrease</td>
</tr>
<tr>
<td>$V_{thp}$</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
<td>mild decrease</td>
</tr>
<tr>
<td>$t_{oxn}$</td>
<td>decrease</td>
<td>increase</td>
<td>decrease</td>
<td>increase</td>
</tr>
<tr>
<td>$t_{oxp}$</td>
<td>decrease</td>
<td>decrease</td>
<td>mild decrease</td>
<td>mild increase</td>
</tr>
</tbody>
</table>
Dual Oxide Technology

• A Monte Carlo analysis of the effects of process variation of design parameters on FoMs
  – Parameters were varied at +/- 10% of selected values from parametric analysis

• A Monte Carlo analysis of the FoMs reaction to variation of individual parameters

• Transistors are assigned different oxide thickness for optimizing design
  – $T_{\text{ox, high}} = 3\text{nm}$
  – $T_{\text{ox, low}} = 2.4\text{nm}$

• FoM’s are analyzed with different oxide thickness
Monte Carlo Analysis: PDF of FoMs

Monte Carlo Analysis of Precharge Time

Monte Carlo Analysis of Power Consumption

Monte Carlo Analysis of Sense Delay

Monte Carlo Analysis of Sense Margin
## Probability Density Function of Different FoMs of the Sense Amplifier

<table>
<thead>
<tr>
<th>Params</th>
<th>Precharge PDF</th>
<th>Power PDF</th>
<th>Sense Delay PDF</th>
<th>Sense Margin PDF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>µ (ps)</td>
<td>σ(ps)</td>
<td>µ (nW)</td>
<td>σ(nW)</td>
</tr>
<tr>
<td>$L_n$</td>
<td>773.65</td>
<td>13.81</td>
<td>191.67</td>
<td>0.56</td>
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<tr>
<td>$L_p$</td>
<td>773.44</td>
<td>2.40</td>
<td>191.67</td>
<td>0.06</td>
</tr>
<tr>
<td>$W_n$</td>
<td>773.18</td>
<td>5.04</td>
<td>191.71</td>
<td>0.50</td>
</tr>
<tr>
<td>$W_p$</td>
<td>774.08</td>
<td>6.34</td>
<td>190.69</td>
<td>2.07</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>772.72</td>
<td>123.68</td>
<td>190.85</td>
<td>27.25</td>
</tr>
<tr>
<td>$C_S$</td>
<td>772.61</td>
<td>0.20</td>
<td>191.68</td>
<td>0.25</td>
</tr>
<tr>
<td>$C_{BL}$</td>
<td>773.48</td>
<td>14.76</td>
<td>191.73</td>
<td>6.38</td>
</tr>
<tr>
<td>$t_{oxn}$</td>
<td>774.15</td>
<td>11.68</td>
<td>191.32</td>
<td>1.47</td>
</tr>
<tr>
<td>$t_{oxp}$</td>
<td>773.74</td>
<td>2.05</td>
<td>192.06</td>
<td>1.93</td>
</tr>
</tbody>
</table>
Algorithm 1: Heuristic algorithm for sense amplifier optimization using Dual Oxide Based Technology

1. Create the netlist of the sense amplifier circuit.
2. Number each of the transistors in the netlist from 1 to N.
3. for Each of the transistors i = 1 to N do
4. Rank the transistors for a figure of merit. For example, contributions to precharge.
5. Identify the significant transistors from the ranks, e.g. 30% or 50%
6. end for
7. Start with the highest ranked transistor as i = 0
8. while Design constraint of the sense amplifier is met and the transistor $M_i$ is a significant transistor that contributes to the overall FoM value of the sense amplifier do
9. Increase thickness oxide of the the transistor $M_i$
10. Move to the next ranked transistor
11. endwhile
Dual Threshold Voltage Technology

• A Monte Carlo analysis of the effects of process variation of design parameters on FoMs
  – Parameters were varied at +/- 10% of selected values from parametric analysis
• A Monte Carlo analysis of the FoMs reaction to variation of individual parameters
• Transistors are assigned different threshold voltages for optimizing design
  – \( V_{\text{th,high}} = 0.36 \text{V} \)
  – \( V_{\text{th,low}} = 0.18 \text{V} \)
• FoM’s are analyzed with different threshold voltages
## Probability Density Function of Different FoMs of the Sense Amplifier

<table>
<thead>
<tr>
<th>Params</th>
<th>Precharge PDF</th>
<th>Power PDF</th>
<th>Sense Delay PDF</th>
<th>Sense Margin PDF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>μ (ps)</td>
<td>σ(ps)</td>
<td>μ (nW)</td>
<td>σ(nW)</td>
</tr>
<tr>
<td>$L_n$</td>
<td>598.01</td>
<td>4.22</td>
<td>94.93</td>
<td>3.13</td>
</tr>
<tr>
<td>$L_p$</td>
<td>597.92</td>
<td>4.12</td>
<td>94.20</td>
<td>3.08</td>
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<tr>
<td>$W_n$</td>
<td>598.20</td>
<td>5.47</td>
<td>94.16</td>
<td>3.03</td>
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<tr>
<td>$W_p$</td>
<td>597.93</td>
<td>4.16</td>
<td>94.15</td>
<td>3.25</td>
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<tr>
<td>$V_{DD}$</td>
<td>602.37</td>
<td>17.83</td>
<td>94.59</td>
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<tr>
<td>$C_S$</td>
<td>597.93</td>
<td>4.15</td>
<td>94.18</td>
<td>3.02</td>
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<tr>
<td>$C_{BL}$</td>
<td>597.82</td>
<td>6.16</td>
<td>94.11</td>
<td>4.11</td>
</tr>
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<td>$V_{thn}$</td>
<td>598.69</td>
<td>5.93</td>
<td>94.42</td>
<td>3.12</td>
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<td>$t_{oxn}$</td>
<td>598.19</td>
<td>5.09</td>
<td>94.36</td>
<td>3.53</td>
</tr>
<tr>
<td>$t_{oxp}$</td>
<td>598.11</td>
<td>4.20</td>
<td>94.41</td>
<td>3.09</td>
</tr>
</tbody>
</table>
Algorithm 2 Heuristic algorithm for sense amplifier circuit optimization using Dual Threshold Based Technology

1. Create the netlist of the sense amplifier circuit.
2. Number each of the transistors in the netlist from 1 to N.
3. for Each of the transistors $i = 1$ to $N$ do
4. Rank the transistors for a figure of merit. For example, contributions to precharge.
5. Identify the significant transistors from the ranks, e.g. 30% or 50%, etc
6. end for
7. Start with the highest ranked transistor as $i = 0$
8. while Design constraint of the sense amplifier is met and the transistor $M_i$ is a significant transistor that contributes to the overall FoM value of the sense amplifier do
9. Increase threshold voltage of the transistor $M_i$.
10. Move to the next ranked transistor.
11. end while
Characterization of Optimized Design

- The FoM’s are improved on the final design.

<table>
<thead>
<tr>
<th>FoMs</th>
<th>Precharge</th>
<th>Power</th>
<th>Sense Delay</th>
<th>Sense Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>7.5 ns</td>
<td>153.1 μW</td>
<td>4.4 ns</td>
<td>43.4 mV</td>
</tr>
<tr>
<td>Dual-$V_{th}$-Optimal</td>
<td>1.2 ns</td>
<td>133.1 μW</td>
<td>0.87 ns</td>
<td>70.4 mV</td>
</tr>
<tr>
<td>Improvement</td>
<td>83.9%</td>
<td>13.1%</td>
<td>80.2%</td>
<td>61.9%</td>
</tr>
</tbody>
</table>
Conclusions

• The effects of process variation were analyzed through parametric and Monte Carlo analysis.
• A method of producing more tolerant and optimal designs was presented.
• FoM’s were improved
  – Precharge by 83.9%
  – Sense delay by 80.2%
  – Sense margin by 61.9%
  – Power dissipation by 13.1%
• Analysis will be extended to different sense amplifier topologies.