Lecture 11: Efficient Design of Flash ADC

CSCE 6933/5933
Advanced Topics in VLSI Systems

Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.
A 45nm Flash Analog to Digital Converter (ADC)
Outline

• Introduction and Motivation
• Specifications
• Related Research Works
• Design of flash ADC
• The TIQ principle
• TIQ Comparator
• Sizing of transistors
• Functional Simulation
• Ideal vs Actual Characteristics
• DNL
• INL
• SNDR
• Instantaneous Power Plot
• Conclusion and Future Works
Introduction and Motivation

• ADCs are interfaced with digital circuits in mixed signal chips, where digital signal processing is performed.
• Supply voltage decreasing rapidly for digital circuits as technology scales.
• Analog to digital converters required to be operating with these devices at the same voltages.
• The proposed design meets both criteria: Low supply voltage (0.7V) and technology (45nm).
Specifications

• Resolution : 6 bits.
• Technology  : 45nm.
• Speed       : 1Gs/sec.
• $V_{\text{LSB}}$ : 500µV.
• $V_{\text{DD}}$ : 0.7V.
• INL         : 0.46LSB.
• DNL         : 0.70LSB.
• SNDR        : 31.9dB.
### Related Research Works

<table>
<thead>
<tr>
<th>Reference</th>
<th>Resolution (bits)</th>
<th>Technology (nm)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
<th>SNDR (dB)</th>
<th>VDD (V)</th>
<th>Power (mW)</th>
<th>Samples/s</th>
<th>sec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Choi 2001</td>
<td>6</td>
<td>350</td>
<td>&lt;±0.3</td>
<td>&lt;±0.3</td>
<td>32</td>
<td>3.3</td>
<td>545</td>
<td>1.3G</td>
<td></td>
</tr>
<tr>
<td>Donovan 2002</td>
<td>6</td>
<td>250</td>
<td>-----</td>
<td>-----</td>
<td>33</td>
<td>2.2</td>
<td>150</td>
<td>400M</td>
<td></td>
</tr>
<tr>
<td>Geelen 2001</td>
<td>6</td>
<td>350</td>
<td>&lt;0.7</td>
<td>&lt;0.7</td>
<td>5.6 (ENOB)</td>
<td>3.3</td>
<td>300</td>
<td>1.1G</td>
<td></td>
</tr>
<tr>
<td>Lee 2002</td>
<td>6</td>
<td>250</td>
<td>1.04</td>
<td>0.81</td>
<td>-----</td>
<td>2.5</td>
<td>59.91</td>
<td>1.11G</td>
<td></td>
</tr>
<tr>
<td>Mehr 1999</td>
<td>6</td>
<td>350</td>
<td>&lt;0.32</td>
<td>&lt;0.2</td>
<td>&gt;5(ENOB)</td>
<td>3.3</td>
<td>225</td>
<td>500M</td>
<td></td>
</tr>
<tr>
<td>Sandner 2005</td>
<td>6</td>
<td>130</td>
<td>&lt;0.4</td>
<td>&lt;0.6</td>
<td>32.5</td>
<td>1.5</td>
<td>160</td>
<td>600M</td>
<td></td>
</tr>
<tr>
<td>Scholten 2002</td>
<td>6</td>
<td>180</td>
<td>-----</td>
<td>0.42</td>
<td>5.7(ENOB)</td>
<td>1.95</td>
<td>328</td>
<td>1.6G</td>
<td></td>
</tr>
</tbody>
</table>
## Related Research Works

<table>
<thead>
<tr>
<th>Reference</th>
<th>Resolution (bits)</th>
<th>Technology (nm)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
<th>SNDR (dB)</th>
<th>VDD (V)</th>
<th>Power (mW)</th>
<th>Samples/s ec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Song 2000</td>
<td>6</td>
<td>350</td>
<td>-0.6</td>
<td>0.7</td>
<td>33.5</td>
<td>1</td>
<td>10</td>
<td>50M</td>
</tr>
<tr>
<td>Srinivas 2006</td>
<td>6</td>
<td>350</td>
<td>0.3</td>
<td>0.3</td>
<td>33.6</td>
<td>3.3</td>
<td>50</td>
<td>160M</td>
</tr>
<tr>
<td>Tseng 2004</td>
<td>6</td>
<td>250</td>
<td>&lt;±0.1</td>
<td>&lt;±0.4</td>
<td>32.7</td>
<td>2.5</td>
<td>35</td>
<td>300M</td>
</tr>
<tr>
<td>Uyttenhove 2000</td>
<td>6</td>
<td>350</td>
<td>-----</td>
<td>-----</td>
<td>32</td>
<td>3.3</td>
<td>-----</td>
<td>1G</td>
</tr>
<tr>
<td>Uyttenhove 2002</td>
<td>6</td>
<td>250</td>
<td>0.42</td>
<td>0.8</td>
<td>32</td>
<td>1.8</td>
<td>600</td>
<td>1.3G</td>
</tr>
<tr>
<td>Yoo 2001</td>
<td>6</td>
<td>250</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>2.5</td>
<td>66.87</td>
<td>1G</td>
</tr>
<tr>
<td><strong>This Design</strong></td>
<td><strong>6</strong></td>
<td><strong>45</strong></td>
<td><strong>0.7</strong></td>
<td><strong>0.46</strong></td>
<td><strong>31.9</strong></td>
<td><strong>0.7</strong></td>
<td><strong>45.42μW</strong></td>
<td><strong>1G</strong></td>
</tr>
</tbody>
</table>
Design of flash ADC

- High level block diagram of ADC.
- Input is analog (generally ramp or sine wave).
- Output of Comparator Bank is thermometer code.
- Converted to 1-out of n code using 1-out of n code generators.
- NOR ROM converts the 1-out of n code to binary code.
Design of flash ADC

- For an n-bit ADC we need: $2^n - 1$ Comparators.
- 1-out of n code generators.
- NOR ROM : $2^n - 1 \times n$.
- For discussion purposes, 3-bit flash ADC is shown. 6-bit ADC has similar structure.
Threshold Inverter Quantization Principle

- TIQ comparator.
- Formed by cascading of digital inverters.
- Sizing of transistors determine switching point.

- Differential comparator.
- Require resistive ladder network.
- Area overhead increases.

Advanced Topics in VLSI Systems

UNT
UNIVERSITY OF NORTH TEXAS
Discover the power of ideas
TIQ Comparator

- Formed by four cascaded inverters.
- Provide a sharper switching for the comparator and full voltage swing.
- Sizes of PMOS and NMOS in a comparator are same, but different for different comparators.
Transistor sizing

DC parametric sweep is used to determine the transistor sizes.

- Input voltage varied from 0 to 0.7 V in steps of 500 µV.
- W/L for NMOS transistors kept as 90nm/90nm. L for PMOS transistors kept as 90nm. W for PMOS transistors was given a parametric sweep in steps of 1 nm. Minimum width=51 nm, maximum width=163 nm.
Functional Simulation

- Transient analysis carried out.
- Ramp generated from 296.3mV to 327.8mV. Digital codes going from 0 to 63 are obtained at the output.
Ideal vs Actual Characteristics

- Ideal vs actual transfer function
- Due to transistor implementation, actual transfer function never equal to ideal transfer function.
- Characterized using DNL and INL.
Max DNL of ADC = 0.7\textit{LSB}

- Differential Non-Linearity. Difference between actual step width and ideal value of 1\textit{LSB}.
- Modeled as Verilog-A block. Uses histogram method. DNL<1\textit{LSB} ensures monotonicity.
Max INL of ADC = 0.46 LSB

- Integral No-linearity. Deviation of actual transfer function from a straight line. expressed in LSB.
- Verilog-A block used. Slowly varying ramp given as input, covering full scale range in 4096 steps.
SNDR = 31.9 dB

\[ SNDR = 20 \times \log_{10} \left( \frac{A_{RMS, \text{Signal}}}{A_{RMS, \text{noise+harmonics}}} \right) dB \]

- Signal to noise and distortion ratio.
- ADC output fed to Ideal DAC. FFT of DAC output obtained. SNDR calculated from this.
Instantaneous Power Plot

- Peak Power = 45.42 µW.
- Avg. Power = 8.8 µW.
- Low power design.
Conclusions

• Successful ADC design at nano-scale (45nm)technology.
• DNL=0.7LSB, INL=0.46LSB.
• SNDR=31.9dB, Low power design (Avg. Power = 8.8µW).
• Layout using 90nm general process design kit.
• Scaling the layout rules to perform layout at 45nm.
A Process and Supply Variation Tolerant Low Voltage, High Speed ADC
Outline of the Talk

• Introduction and Motivation
• Contributions, Design issues and Solutions
• Related Prior Research Works
• Transistor level design of the proposed ADC
• Physical design and Characterization of ADC
• Process and Supply variation Characterization
• Conclusion and Future Works
Introduction: Why Nano-CMOS ADC

- A large number of SoCs manufactured at the 90nm process, 65nm, 45nm closely following.
- Challenge is to meet performance of analog circuit with that of digital portion.
- Systems that once worked at 3.3/2.5V need to work at 1.8V without performance degradation.
- New circuit design techniques required to accommodate lower supply voltages.
- Analog/Mixed signal circuits should be designed using standard CMOS digital process.
Introduction: Nano-CMOS ADC

- ADC is a true mixed signal circuit used to bridge the gap between analog circuits and digital logic world.
- ADC circuit designs often contain matched transistors. In analog circuits, threshold voltage mismatch needs to be considered.
- For SoC capability, supply voltage variation should also be accounted.
- The demand for emerging application-specific, nanoscale mixed-signal SoCs which need process (threshold voltage mismatch) and power supply voltage variation tolerant ADC interfacing has motivated this research.
Design Issues and Solutions

- Logical and physical design of a **process and supply variation tolerant ADC** using **90nm** technology, suitable for SoC integration.

- Post-layout simulation results presented.

- Low supply voltage ($V_{dd} = 1.2V$), low power (Power $\alpha V_{dd}^2$). Low $V_{dd}$ puts constraint on the choice of 63 quantization levels (for 6-bit ADC in this paper). $LSB = 1mV$ chosen for this design.

- **INL** degradation ($INL > 1LSB$) observed in the initial physical design, due to IR drop in the supply lines. $INL = 0.344LSB$, by using large number of contacts and widening the supply lines.

- Power analysis with $100fF$ reveals ADC consumes minimal power.
## Related Prior Research Works

<table>
<thead>
<tr>
<th>Works</th>
<th>Tech. (nm)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
<th>$V_{dd}$ (V)</th>
<th>Power (mW)</th>
<th>Rate (GS/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Geelen[9]</td>
<td>350</td>
<td>&lt; 0.7</td>
<td>&lt; 0.7</td>
<td>3.3</td>
<td>300</td>
<td>1.1</td>
</tr>
<tr>
<td>Uytttenhove [19]</td>
<td>350</td>
<td>---</td>
<td>---</td>
<td>3.3</td>
<td>---</td>
<td>1</td>
</tr>
<tr>
<td>Donovan [6]</td>
<td>250</td>
<td>---</td>
<td>---</td>
<td>2.2</td>
<td>150</td>
<td>0.4</td>
</tr>
<tr>
<td>Tseng [8]</td>
<td>250</td>
<td>&lt; 0.1</td>
<td>&lt; 0.4</td>
<td>2.5</td>
<td>35</td>
<td>0.3</td>
</tr>
<tr>
<td>Yoo [11]</td>
<td>250</td>
<td>---</td>
<td>---</td>
<td>2.5</td>
<td>66.87</td>
<td>1</td>
</tr>
<tr>
<td>Scholtens [16]</td>
<td>180</td>
<td>---</td>
<td>0.42</td>
<td>1.95</td>
<td>328</td>
<td>1.6</td>
</tr>
<tr>
<td>Sandner [7]</td>
<td>130</td>
<td>&lt; 0.4</td>
<td>&lt; 0.6</td>
<td>1.5</td>
<td>160</td>
<td>0.6</td>
</tr>
<tr>
<td>This Work</td>
<td>90</td>
<td>0.459</td>
<td>0.344</td>
<td>1.2</td>
<td>3.875</td>
<td>1</td>
</tr>
</tbody>
</table>

- Low Technology, low voltage, low power, high speed design with satisfactory DNL, INL performance.
Transistor Level Design of the Proposed ADC
- Output of Comparator Bank is thermometer code.
- Converted to 1-of n code using 1-of n code generators.
- NOR ROM converts the 1-of n code to binary code.
ADC : Circuit Diagram
Comparator Design: Technique

• Comparator designed using Threshold Inverting (TI) technique.

• Advantages of TI technique:

  1. High speed.
  2. Simplicity.
  3. Eliminates the need for inherently complex high-gain differential input voltage comparators and additional resistor ladder circuit.
Comparator Design : Circuit

- $V_{\text{switching}}$ set internally based on transistor sizes.
- Inverter 1 and 2 form the baseline comparator, while Inverter 3 and 4 provide increased gain and sharper switching.
Comparator Design: Equations

For short channel transistors:

\[ V_{\text{switching}} = V_{dd} \left( \frac{R_n}{R_n + R_p} \right) \]

\( R_n \) = NMOS effective switching resistance.
\( R_p \) = PMOS effective switching resistance.

\[ \text{InputVoltageRange} = V_{dd} - \left( V_{tn} + |V_{tp}| \right) \]

\( V_{dd} \) = supply voltage.
\( V_{tn} \) = NMOS threshold voltage.
\( V_{tp} \) = PMOS threshold voltage.

Values chosen 493mV to 557mV.

\[ V_{LSB} = \left( \frac{\text{InputVoltageRange}}{2^n} \right) \]

For our design,
\( V_{LSB} = 1mV \).
1 of n code generator Design

- Converts thermometer code into 1 of n code.
- Consists of AND gates as combination of an inverter followed by a NAND gate.
- Output from each of the AND gates is fed to the input of the NOR ROM.
- One of the two inputs to the AND gate is fed from the TI comparator output.
- The other input to the AND gate is the inverted output from the next level comparator.
NOR ROM Design

- Converts 1-of-n code to binary code.
- Consists of PMOS (135nm/180nm) pull-up and NMOS (180nm/180nm) pull-down devices.
- 63 word lines, 6 bit lines, 63 x 6 NOR ROM designed.
- $W_p < W_n$, to ensure PMOS is narrow enough for NMOS to pull down output safely.
- Buffers, consisting of two cascaded inverters (PMOS: 480nm/120nm, NMOS: 240nm/120nm) are applied at the outputs to obtain symmetrical waveforms, with equalized rise and fall times.
Physical Design and Characterization of ADC
ADC: Physical Design

• Physical design of the ADC carried out using 90nm Salicide “1.2V/2.5V 1 Poly 9 Metal” digital CMOS pdk, demonstrating SoC readiness.

• To ensure minimal IR drop, power and ground routing comprises of wide vertical bars and generous use of contacts has been made.
Post Layout Functional Simulation

• Transient analysis is carried out, where a linearly varying ramp covering full scale range of ADC, is given as input.

• Output digital codes from 0 to 63 obtained correctly, with no missing codes. Maximum sampling speed - 1GS/s.

![Transient Response Graph](image-url)
Characterization: Equations

- ADC characterized for static performance.
- Nominal characterization: Histogram test used to determine \( \text{INL} \) (Integral Non-Linearity), \( \text{DNL} \) (Differential Non-Linearity).
- Equations for \( \text{INL}, \text{DNL} \):

  \[
  \text{INL}[i] = \text{width}[i] + \text{INL}[i-1] - 1 \]
  \[
  \text{DNL}[i] = \text{width}[i] - 1 \]
  \[
  \text{width}[i] = \frac{1 \times \text{bucket}[i]}{\text{hits} \times (\text{NUM}_{\text{CODES}} - 2)}
  \]

  - where \( \text{bucket} \) holds the number of code hits for each code.
  - \( \text{width} \) holds the code width calculations.
  - Total hits between codes 1 and 62 is denoted as \( \text{hits} \).
  - \( \text{NUM}_{\text{CODES}} \) is the number of codes, 64 for a 6-bit ADC.
Characterization: \textit{INL} and \textit{DNL} Plots

- Maximum \textit{INL}=0.344\textit{LSB}.
- Maximum \textit{DNL}=0.459\textit{LSB}.
Power Analysis

- Power analysis of the ADC performed with a capacitive load of 100fF.
- Peak Power = 5.794mW.
- Average Power = 3.875mW.

**Instantaneous Power Plot.**

<table>
<thead>
<tr>
<th>ADC Components</th>
<th>Average Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator Bank</td>
<td>3.68125 (95%)</td>
</tr>
<tr>
<td>1 of n code Generators</td>
<td>0.03875 (1%)</td>
</tr>
<tr>
<td>NOR ROM</td>
<td>0.155 (4%)</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>3.875</strong></td>
</tr>
</tbody>
</table>
## ADC Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90nm CMOS 1P 9M</td>
</tr>
<tr>
<td>Resolution</td>
<td>6 bit</td>
</tr>
<tr>
<td>Supply voltage ($V_{dd}$)</td>
<td>1.2V</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>1GS/s</td>
</tr>
<tr>
<td><strong>INL</strong></td>
<td>0.344LSB</td>
</tr>
<tr>
<td><strong>DNL</strong></td>
<td>0.459LSB</td>
</tr>
<tr>
<td>Peak Power</td>
<td><a href="mailto:5.794mW@1.2V">5.794mW@1.2V</a></td>
</tr>
<tr>
<td>Average Power</td>
<td><a href="mailto:3.875mW@1.2V">3.875mW@1.2V</a></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>493mV to 557mV</td>
</tr>
<tr>
<td>$V_{LSB}$</td>
<td>1mV</td>
</tr>
</tbody>
</table>
Process and Supply variation
Characterization
Process Variation

• Corner-based methodology is used.
• NMOS threshold voltage \( (V_{tn}) \) and PMOS threshold voltage \( (V_{tp}) \) varied by ±5% from nominal value in the pdk.
• Shift in \( INL \), \( DNL \), input voltage range recorded.
• \( INL \) shows maximum variation of 10.5%.
• \( DNL \) shows maximum variation of 5.7%.
Process Variation: Corner Method

Diagram showing variations in Vtp and Vtn with nominal values and variations of +5% and -5%.
### Process Variation: INL and DNL

<table>
<thead>
<tr>
<th>$V_{tp}, V_{tn}$</th>
<th>Input Range (mV)</th>
<th>$V_{LSB}$ (mV)</th>
<th>INL (LSB)</th>
<th>DNL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>nominal</td>
<td>493-557</td>
<td>1</td>
<td>0.344</td>
<td>0.459</td>
</tr>
<tr>
<td>+5%, +5%</td>
<td>495-557</td>
<td>0.96875</td>
<td>0.333</td>
<td>0.46</td>
</tr>
<tr>
<td>-5%, -5%</td>
<td>491-556</td>
<td>1.015625</td>
<td>0.345</td>
<td>0.477</td>
</tr>
<tr>
<td>-5%, +5%</td>
<td>500-564</td>
<td>1</td>
<td>0.36</td>
<td>0.485</td>
</tr>
<tr>
<td>+5%, -5%</td>
<td>501-566</td>
<td>1.015625</td>
<td>0.38</td>
<td>0.479</td>
</tr>
</tbody>
</table>
Supply Variation: INL and DNL

- Nominal supply voltage (1.2V) varied by \( \pm 10\% \).
- INL, DNL, and input voltage range values are recorded.
- INL shows maximum variation of 4%.
- DNL shows maximum variation of 4.8%.

<table>
<thead>
<tr>
<th>Vdd(V)</th>
<th>Input Range (mV)</th>
<th>V_{LSB} (mV)</th>
<th>INL (LSB)</th>
<th>DNL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.08V (-10%)</td>
<td>448-500</td>
<td>0.8125</td>
<td>0.359</td>
<td>0.467</td>
</tr>
<tr>
<td>1.2V (nominal)</td>
<td>493-557</td>
<td>1</td>
<td>0.344</td>
<td>0.459</td>
</tr>
<tr>
<td>1.32V (+10%)</td>
<td>537-614</td>
<td>1.203</td>
<td>0.339</td>
<td>0.481</td>
</tr>
</tbody>
</table>
Conclusion and Future Works

• Design of a process and supply variation aware low voltage, high speed flash ADC presented.
• Comparators designed using threshold inverting (TI) technique.
• ADC subjected to ±10% supply variation, ±5% threshold voltage mismatch.
• Nominal $INL=0.344\text{LSB}$, maximum variation of 10.5%.
• Nominal $DNL=0.459\text{LSB}$, maximum variation of 5.7%.
• It is demonstrated that the design of low voltage, high speed and SoC ready ADCs is possible at 90nm technology and below.
• We plan to carry out the complete design cycle for this ADC at 45nm.
• Alternative encoder architectures will be explored to achieve higher sampling speeds.