An Energy Efficient Epileptic Seizure Detector

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Abstract-Epilepsy is one of the most common neurological disorders affecting up to 1% of the world's population and approximately 2.5 million people in the United States. Seizures in more than 30% of epilepsy patients are resistant to antiepileptic drugs. A significant biomedical research is focused on the development of an energy efficient implantable integrated circuit for real-time detection of seizures. In this paper we propose an architecture for an implantable seizure detector using a hyper-synchronous signal detection circuit and signal rejection algorithm (SRA). The proposed seizure detector (SD) continuously monitors neural signals for hyper-synchronous pulses and extracts the seizure onset signal. If the pulses in an epoch exceed a threshold value, a seizure is declared. The design was validated using Simulink[®]. The signal rejection algorithm (SRA) reduces false detection and minimal circuitry leads to a 12% reduction of power consumption.

Index Term— Energy Efficient Design, Epilepsy, Seizure, Hypersynchronous

I. INTRODUCTION

Smart health care is increasingly important due to the twin pressures of increasing population and limited resources. A specific example of smart health care is the automated realtime detection of epileptic seizures [1]. A seizure is the manifestation of an abnormal hyper-synchronous disturbance of a population of cortical neurons [2], which may manifest as sensory disturbance, loss of awareness, or convulsions. Epilepsy is a neurological disorder marked by spontaneous recurrent seizures.

Anti-epileptic drugs are used to control seizures, but more than 30% of epilepsy patients remain refractory to medication. Epilepsy surgery is not a good choice for some refractory patients if the seizure focus is located in the eloquent cortex. Surgery leads to the damage of the eloquent area and creates significant neurological deficit [3], [4]. Consequently, in patients who are refractory, uncontrolled seizures result in a devastating impact on the patient's quality of life. There has been a trend to develop a fully implantable device for automated monitoring, warning and suppression of seizures. Early warning can enable a patient to take protective action when necessary. Automated, closed loop therapy for seizure detection can manage epilepsy successfully. It offers a significant reduction of the intensity of the seizure. Responsive Saraju P. Mohanty Dept. of Computer Science and Engineering University of North Texas, USA. Email: saraju.mohanty@unt.edu

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neural stimulation (RNS) which is approved by the Food and Drug Administration (FDA) suppresses seizure at their onset.

We propose in this paper a seizure detector for an implantable medical device. The proposed seizure detector offers reduced design complexity, power consumption, and sensitivity to noise. In this approach, neural signals are monitored continuously. A detection circuit analyzes the input signal and detects candidate seizure activity (hyper-synchronization). A separate algorithm is used to analyze the hyper-synchronous pulses. If the pulses exceed a threshold, then a seizure is declared. MATLAB[®] software analyzes the electrophysiological signals and the implementation of the proposed model is performed in Simulink[®]. The proposed seizure detector considerably enhances detection accuracy and power gain.

The remainder of the paper is organized as follows: Section II highlights the novel contributions. Existing research on seizure detection is presented in Section III. Section IV illustrates the architectural overview and design of the proposed detector. The implementation of the design block is discussed in Section V. Simulation results are shown in Section VI and conclusions are presented in Section VII.

II. NOVEL CONTRIBUTIONS OF THIS PAPER

The proposed approach detects seizure onset based on the number of hyper-synchronous pulses. The signal detection circuit provides the data for the hyper-synchronous pulses. The proposed signal rejection algorithm (SRA) analyzes the data and then accurately removes unwanted bursts of pulse and high frequency samples. The algorithm continues until the hyper-synchronous pulses cross a threshold point, which helps reduce false detections. This algorithm is tested with different data and is proven to be accurate and useful. The use of limited circuitry in the proposed method leads to reduced power consumption and consequently makes this method more energy efficient.

III. RELATED PRIOR RESEARCH

Several seizure detection algorithms like wavelet decomposition [5], phase coherence [6], and signal synchronization have been proposed. The implementations of those algorithms are only confined to powerful desktop computers and are not applicable to an implanted device. Over the last few years, a significant research is focused on developing implantable devices [7], [8], [4]. The event based algorithm [7] is relied on distributing EEG datasets into identical sized events. The threshold voltage associated with EEG abnormalities defines a seizure state. The detector depends on both positive and negative threshold voltages, but can lead to false detection. The detection method based on support vectors [9] has improved the detection accuracy considerably but requires numerous support vectors to define a seizure and normal state. The drawback is high cost and high power consumption. The detector in [10] needs complex digital circuitry and an application specific chip to achieve the required sensitivity. The preamplifier based detection technique in [4], which is implemented with CMOS technology, is very useful for epileptic seizure detection. But the power consumption is relatively high. There are also some noise related issues due to poor noise performance of CMOS technology. Here, we present a detection method which is energy efficient and less vulnerable to noise [11].

IV. THE PROPOSED NOVEL SEIZURE DETECTOR: AN ARCHITECTURE PERSPECTIVE

The proposed implantable seizure onset detector monitors the brain activity in the seizure onset area. Low-voltage fast activity discharge (Fig. 1) is generally used to characterize seizure onset. Some of the epileptic discharge is very short period which is referred as brief seizure. Brief seizure does not spread to the Epileptogenic Zone (EZ) and can be ignored.



Fig. 1. Seizure activity characterization in time domain (a) Invasive Electroencephalography (EEG) of an epileptic seizure (b) zoom inset 6-10 seconds.

A. Overall Proposed Architecture

Fig. 2 shows the architecture of the proposed detector. The input signal is modulated with a high frequency carrier signal.

The conversion of positive signal amplitudes from negative is done using eq. (1) [2]. The voltage level detector detects the hyper-synchronous pulses based on eq. (2). The discrete modulated signal V_{mod} is:

$$V_{mod}(n) = \sum_{n=1}^{T_f/T} x(nT_S)(-1)^n$$
(1)

where, n = 1, 2, 3...N.

The detected over-excited signal is:

$$V_{vld}(n) = \begin{cases} 1, & \text{for } V_{upper} > V_{mod}(n) > V_{lower} \\ 0, & \text{otherwise} \end{cases}$$
(2)

where V_{lower} and V_{upper} are the lower and upper boundaries of the voltage level detector. Unwanted signals are eliminated by eq. (3). The elimination of the unwanted signals continues till the hyper-synchronous pulses exceed the threshold. The seizure detection is:

$$V_{SE}(n) = \begin{cases} 1, & \text{seizure, for } V(n-i) = 1 \cdots \text{ and } V(n) = 0\\ 0, & \text{no seizure, otherwise} \end{cases}$$
(3)



Fig. 2. Proposed architecture of the seizure detector.

The proposed system comprises of two main functional blocks, the details of which are given below.

B. Hyper-synchronous Signal Detection Circuit

The proposed circuit (Fig. 3) consists of a modulator, amplifier, high-pass filter and Voltage Level Detector (VLD). The low amplitude neural signal is modulated to a high frequency (F_s) to make the signal invulnerable to low frequency instrumentation noise.



Fig. 3. Proposed hypersynchronous signal detection circuit.

Due to very low amplitude range of neural signals, they need to be amplified prior to analysis. The adjustable gain of the amplifier enables amplification to the desired level. A high pass filter attenuates unwanted low frequency signal and various noise including DC-offset voltage noise associated with the amplifier. Hyper-synchronous signals are detected by the VLD, as indicated in eq. 2. The threshold voltages of the VLD are determined by time domain analysis of the filtered signal.

C. Signal Rejection Algorithm (SRA): Detection of seizure onset from hypersynchronous signals

The rejection algorithm analyzes the hyper-synchronous signal from the VLD and eliminates spurious pulses using the following algorithm: The removal of false detections is carried out by:

$$V_{SE1}(n) = \begin{cases} 0, & V(n-2) = 0 \text{ or } V(n-1) = 0\\ V(n), & \text{otherwise} \end{cases}$$
(4)

The spurious pulse is further eliminated using:

$$V_{SE2}(n) = \begin{cases} 0, & V(n-1) = 0, \text{ if } V(n) = 1\\ V(n), & \text{otherwise} \end{cases}$$
(5)

The seizure onset is defined by:

$$V_{SE}(n) = \begin{cases} \text{Seizure,} & V(n-2) = 1, \text{ if } V(n-1) = 0\\ 0, & \text{otherwise} \end{cases}$$
(6)

The seizure detector (SD) monitors neural signals continuously. The proposed algorithm detects seizure onset from hyper-synchronous pulses (V_{vld}). In a time frame, this algorithm eliminates spurious pulses if they fall below the defined threshold. The SRA completes the *n*-th iteration to define a seizure onset. If the number of hyper-synchronous pulses exceeds the threshold number, SD locks its V_{SE} to 1 followed by eqs (4),(5) and (6), thus indicating a seizure. The decision is locked until time period ends.

V. MODELING AND IMPLEMENTATION OF THE PROPOSED EPILEPTIC SEIZURE DETECTOR

The EEG signal is initially modulated with a high frequency carrier signal. Modulation separates the original signal from low frequency noise. The low amplitude neural signal is then amplified using an adjustable gain amplifier. The high pass filter eliminates various low frequency noise components associated with the amplifier and the channel. The upper and lower voltages associated with the voltage level detector define the hyper-synchronous signal. The proposed detector extracts the seizure onset using SRA.

The power estimation of the proposed detector is performed in Simulink[®]. An input pattern independent method is employed for the accurate estimation of power dissipation. In this method, the proposed design is simulated with different EEG datasets of identical size. The average of the simulation results is considered as a estimation for power dissipation. The sensors and measurement blocks of Simulink[®] extracts the voltage and current value from the design, which is viewed as a black box, and gives power dissipation. Brain signals are fed into the system. The modulation of the EEG signals with a high frequency carrier lead to the prevention of various low frequency noise. Neural signal analysis is a critical issue, as the amplitude is in the tiny micro-volt level range.

The adjustable gain amplifier enables signals to be amplified to the desired level. A high pass filter eliminates low frequency signals and extracts all seizure onset information. Hypersynchronous signals are detected by the VLD. The VLD uses a Simulink[®] user defined function, with a maximum and minimum value. If the voltage is within the range, the function outputs a 1, otherwise it is zero. The maximum and the minimum voltage of the VLD is determined by time domain analysis of the filtered signal. The hyper-synchronous signal is processed with the Signal Rejection Algorithm (SRA). Initially, if a signal is 0 and neighboring values are 0, the algorithm outputs a 0; if the signal is 1 and neighboring values are 0, the algorithm outputs a 0. '1' denotes an overexcited pulse. A threshold number of hyper-synchronous pulses defines seizure onset. The threshold value of the overexcited pulses can be calculated from time frame and samples. If the number of hyper-synchronous pulses in a time frame exceeds the threshold, the algorithm indicates a 1, signaling a seizure.

VI. EXPERIMENTAL RESULTS

The EEG recordings were the from Bern-Barcelona EEG Database [12], [13]. Input data are analyzed in MATLAB[®] then Simulink[®] is invoked. The input EEG signal is modulated into a high frequency (6 KHz) signal as shown in Fig. 4. The modulated signals (V_{mod}) are amplified to the desired level. The VLD extracts the seizure onset information using upper and lower voltages (Fig. 5). The voltages V_{upper} , V_{lower} can be determined by time domain or frequency domain analysis of the filtered signal (V_{hpf}) . VLD detects a number of unwanted pulses of varied amplitude, as a result of modulation. The detected hyper-synchronous pulses (V_{vld}) are fed into the SRA which removes portion of the pulses during the first iteration. A threshold number of over-excited pulses within a time frame (T_f) defines a seizure onset. The iteration continues until the number of hyper-synchronous pulses surpass the threshold number. The threshold number can be calculated from time frame, samples and time domain analysis of hypersynchronous signal (V_{vld}) . SRA completes the *n*-th iteration to remove all unwanted pulses. Overall, the system has detected 1 pulse during 1 second simulation. The rejection of unwanted signal and detection of seizure onset using SRA during 1st and n-th iteration is shown in Fig. 6). The calculated time frame is 80 ms. The detection time varies with the patient but is typically in the order of a few seconds.

Based on the patient, T_f , V_{upper} , V_{lower} can be varied. Some unwanted filtered signals with an amplitude identical with VLD range could cause false pulses. The incorporated SRA is highly effective in removing unwanted false signals. Simulation data are shown in Table I. The frequency range for epileptic discharge is between 5 and 25 HZ. The amplitude of the seizure pattern at onset is between 200mv to 400mv. The



Fig. 4. Transient analysis (a) Zoom inset 6-9 seconds of input EEG signal (b) Modulated signals.



Fig. 5. Transient analysis (a) Zoom inset 8-9 seconds of input EEG signal (b) Output of VLD.

total power consumption is 6.18μ , which is 12% less compared to [2], and 18% less compared to [9].



Fig. 6. Transient analysis (a) Zoom inset 8-9 seconds of input EEG signal (b) Output of SRA after first iteration (b) Output of SRA after nth iteration and detection of seizure onset.

VII. CONCLUSION AND FUTURE RESEARCH

We propose an energy-efficient epileptic seizure detector. The implementation of the proposed algorithm is performed

 TABLE I

 SIMULATION DATA OF THE PROPOSED DETECTOR

Parameter	Value
Seizure Frequency (Minimum)	5 Hz
Seizure Frequency (Maximum)	25 Hz
VLD (Average Lower Threshold)	210 mV
VLD (Average Upper Threshold)	380 mV
Total Power Consumption	6.18 uw

using Simulink[®]. The system level simulation demonstrates the detection of seizure onset marked by hyper-synchronous activity. The rejection algorithm employed by the seizure detector is highly efficient in minimizing false detection by removing unwanted signals. It is evident from the simulation results that there is a considerable reduction in power consumption (12%-18%) compared to existing methods and may be useful for epilepsy treatment. Future research involves generating a probabilistic pattern of EEG abnormalities and combining it with the proposed architecture for the seizure onset detector.

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