Overview
In this section of the lab, we will be simulating the VHDL circuit we created in part 1 using Modelsim.

Procedure
1. **Mount CSEE account**

   Open the Modelsim tool...
2. **Start->Applications->Modelsim XE II v5.6e->Modelsim**

   Open new project
3. **File->New Project**
4. Enter a name for the project in the *Project Name* box.
5. Leave the default library name as *work*

   Add VHDL Source
6. In the "Add items to project" window, select **Add Existing File**
7. Enter the path and file name for the VHDL source file created in the first part of the lab, click **OK**.

   Compile VHDL Source File
8. In the project window, select file just added. Click **Compile->Compile ALL**

   Start Simulation
9. There are multiple ways to complete tasks within Modelsim. Use of the commands at the command prompt window is encouraged as most of the technical parts of the simulations will be done in this form. To start the simulation, either...

   type **vsim** *entity_name* into the command prompt window, where entity_name is the name of the entity for your circuit

   OR

   Simulate->Simulate..., expand **work** and select your entity. Then click **Load**.

10. Open wave form window and signal list...

    type: **view wave signals** into the command prompt window

    OR

    View->Wave and **View->Signals**

11. Add signals to wave: in signals window, click **Add->Wave->Signals in Design**

Set initial values
12. Simulations require input stimuli in order to simulate the design. Testbenches are the standard way to test VHDL designs, but writing testbenches is beyond the scope of the purpose for this lab. Modelsim provides a convenient way to set input values with the **force** command. Here is the syntax:

> **force [-repeat** *after_period* **]** *signal_name logic_value after _delay, logic_value after_delay, ...*

signal_name is the name of the signal we want to force,
logic_value after_delay indicates what logic value to assign and after what delay to wait from the current simulation time before assigning it. Multiple transitions can be specified in this manner with a single force statement by separating them (*logic_value after_delay)* with commas.
-repeat *after_period* indicates that the value assignments are periodic and what the period is (like a repeating clock, where the *after_period* is the clock period).

> *ex:* force input signal *input1* to a value '0' now (0 ns delay) and then to a '1' after a 40 ns delay. The force command would look like this:

> force input1 0 0ns, 1 40ns

> If the signal transition needs to be repeated every 80 ns (like a clock with a period of 80 ns) then it could be specified like this:

> force -repeat 80ns input1 0 0ns, 1 40ns

For this lab, the circuit will need to be tested exhaustively by giving all possible combinations of the two inputs. To do this, give one input twice the period of the other and make them repeat.
> *ex:*

> force -repeat 80ns input1 0 0ns, 1 40ns
> force -repeat 160ns input2 0 0ns, 1 80ns

To undo the forced values (or if an output accidentally gets forced!), use:
> **noforce** *signal_name*

Run Simulation
13. In the command prompt window, type **run 200ns**. This will run the simulation for 200 ns.
14. Verify that the circuit is functionally correct.

Print Waveform

15.Click **View->Zoom->Zoom Full**, which will expand the waveform to fill the entire viewable window.

16.Click **File->Print...** and select the following

   Signal Selection: All Signals

   Click **Setup** and indicate the following:

   Scaling: fit to 1 page
   Orientation: Landscape
   Color: B&W
   Grid: On

   Click **OK** and **Print**.

Lab Report

For the Lab report, create a cover sheet with your Name, the Lab Number, Course Name, and what Day and Time you attend lab (ex. MW 3:30 – 4:45). This format for cover sheet will be used for all following labs. Print a copy of your VHDL source file and your synthesis report from part 1. Submit the cover sheet, VHDL source file, Synthesis Report, and the waveform from Modelsim by the end of lab.