Memory and Programmable Logic Devices

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Part 2

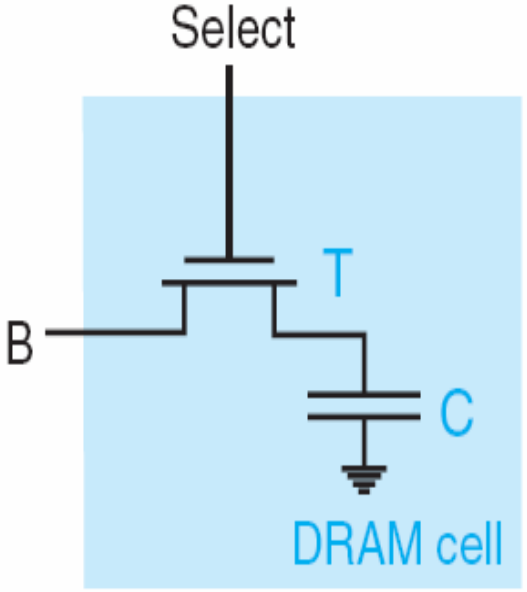
- Dynamic RAM ICs
- Array of RAM ICs
- Programmable Logic Technologies
- Read-Only Memory

Sources

–Logic and Computer Design Fundamentals by M. M. Mano and C. R. Kime.

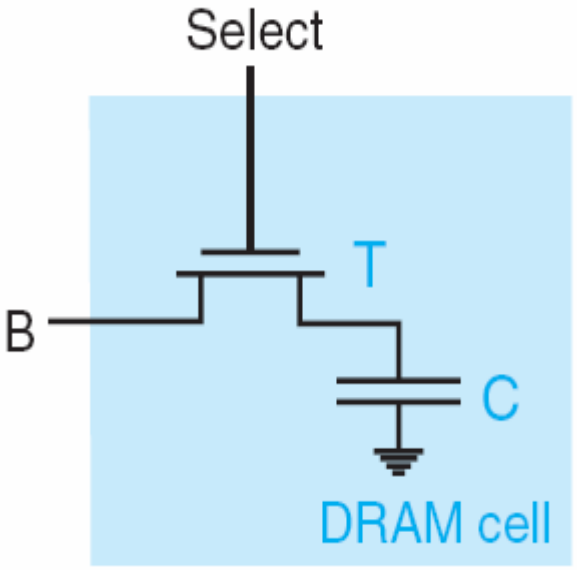
Dynamic RAM ICs

- Due to high storage capacity at low cost, DRAM dominates the high-capacity memory applications.
- Storage of information only temporary, the information must be periodically refreshed to mimic behavior of static RAM. Hence the name dynamic.

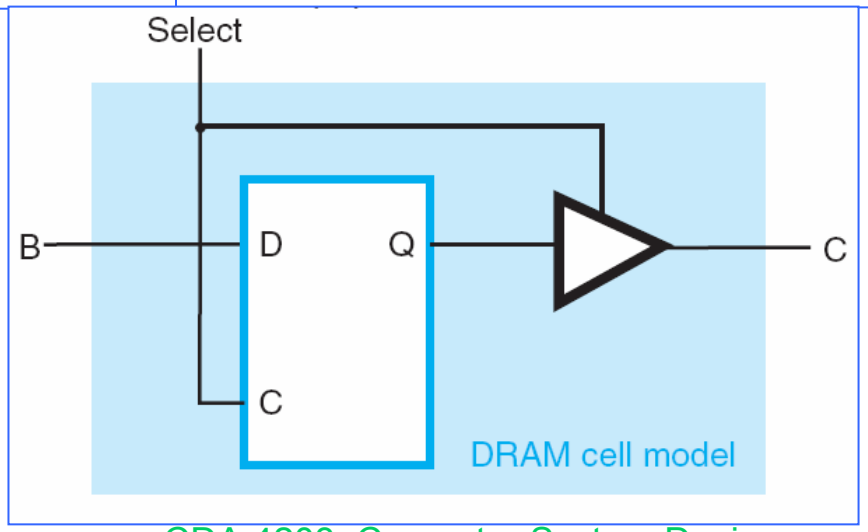


- Consists of a capacitor and a transistor
- Capacitor is used to store electric charge.
- Transistor acts a switch.
- If there is a sufficient charge stored in a capacitor, then it is viewed as storing logic 1.
- On the other hand, if there is insufficient charge stored in the capacitor, then it is viewed as logic 0.

Dynamic RAM ICs ….



- When the switch is open, the charge on the capacitor roughly remains fixed, i.e. stored.
- When the switch is closed, charge can flow into and out of the capacitor from the external Bit (B) line.
- This charge flow allows the cell to be written with a 1 or 0 and also to be read.



Dynamic RAM ICs: Refreshing

- The problem with capacitors is that they only hold a charge for a short period of time, and then it fades away (being leaky in nature).
- These capacitors are very small, so their charges fade particularly quickly.
- This is why the refresh circuitry is needed to read the contents of every cell and refresh them with a fresh "charge" before the contents fade away and are lost.
- Refreshing is done by reading every "row" in the memory chip one row at a time; the process of reading the contents of each capacitor re-establishes the charge.

Dynamic RAM ICs: Refreshing …

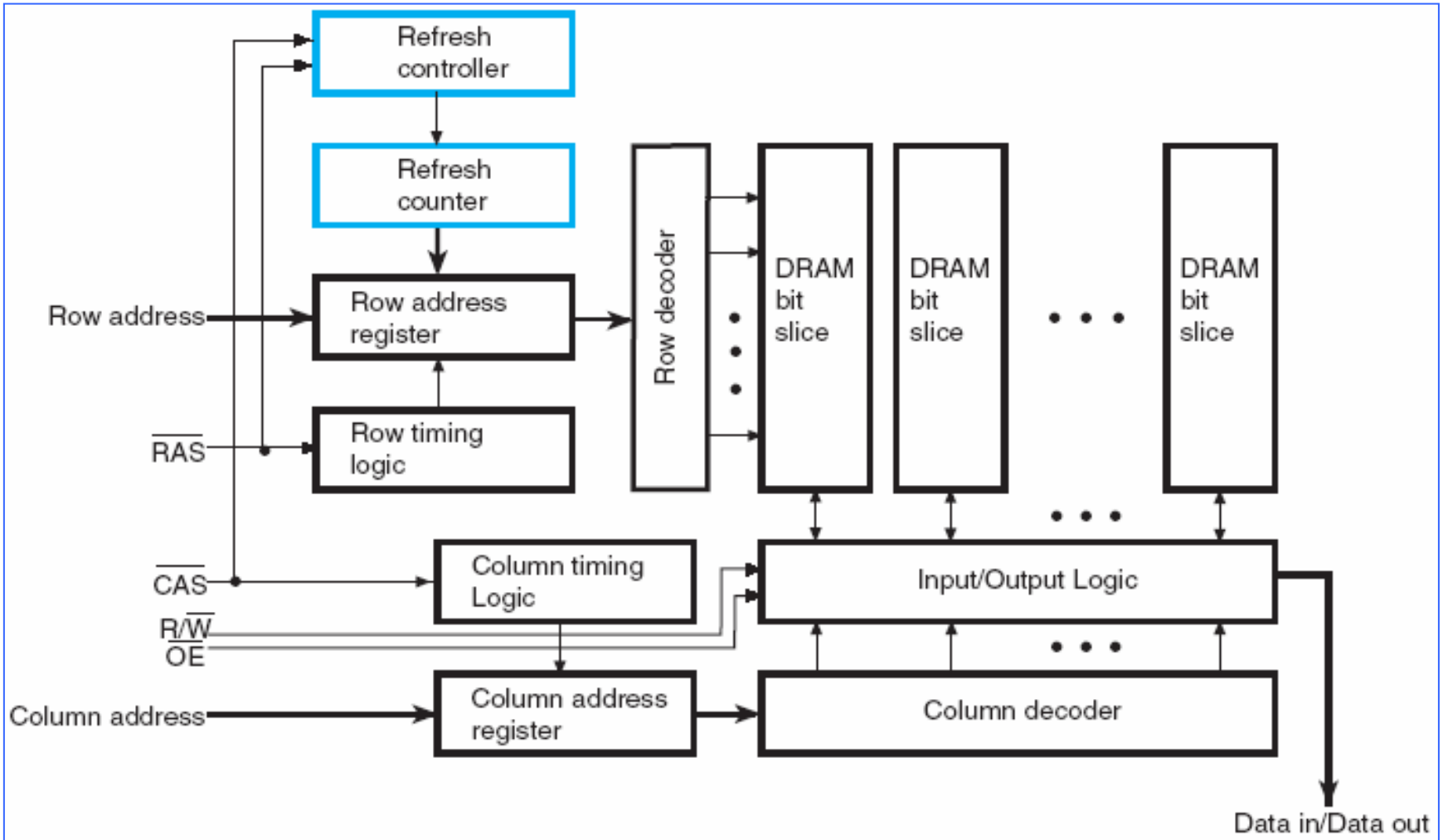
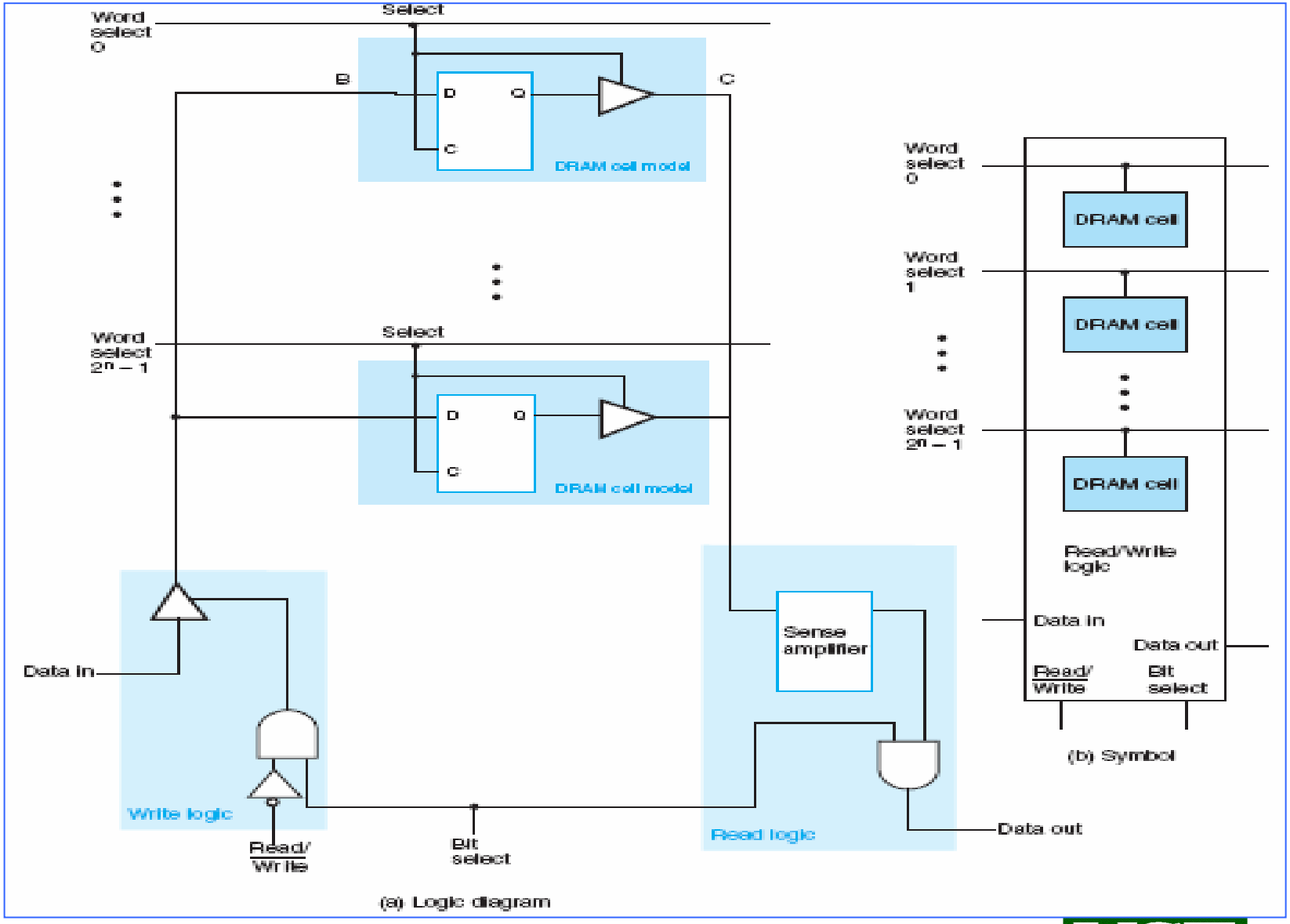


Fig. 6-13 Block Diagram of a DRAM Including Refresh Logic

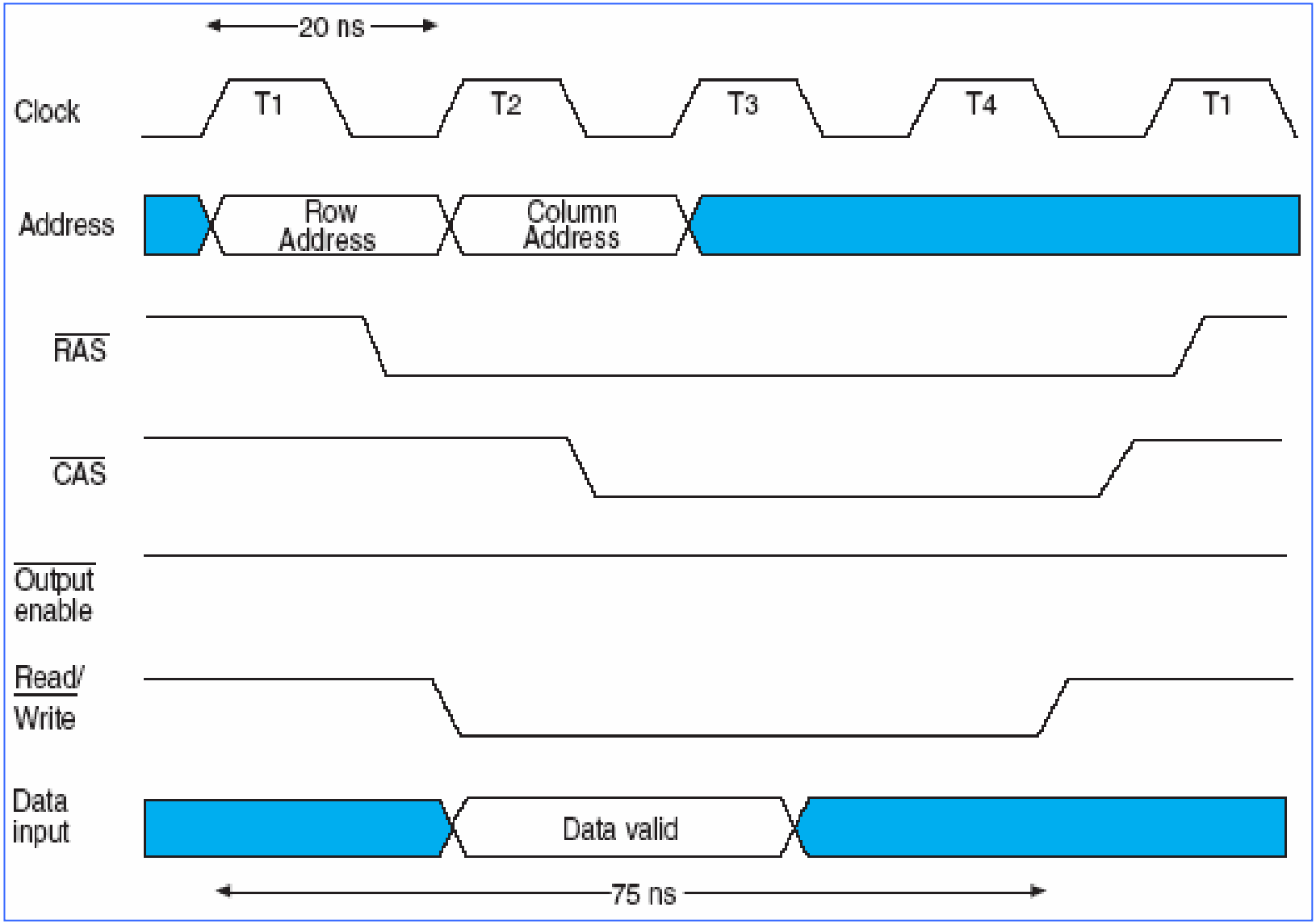
Dynamic RAM ICs: Refreshing …

- To reduce the number of pins, the DRAM address is applied in two parts with row address, first and then column address.
- Row address register is used to store the row address.
- The column address is also stored in a register.
- The load signal for the row address register is RAS' (Row Address Strobe).
- Similarly, the load signal for the column address register is CAS' (Column Address Strobe).
- Additional signals are, R/W' (Read/Write') and OE' (Output Enable)'.

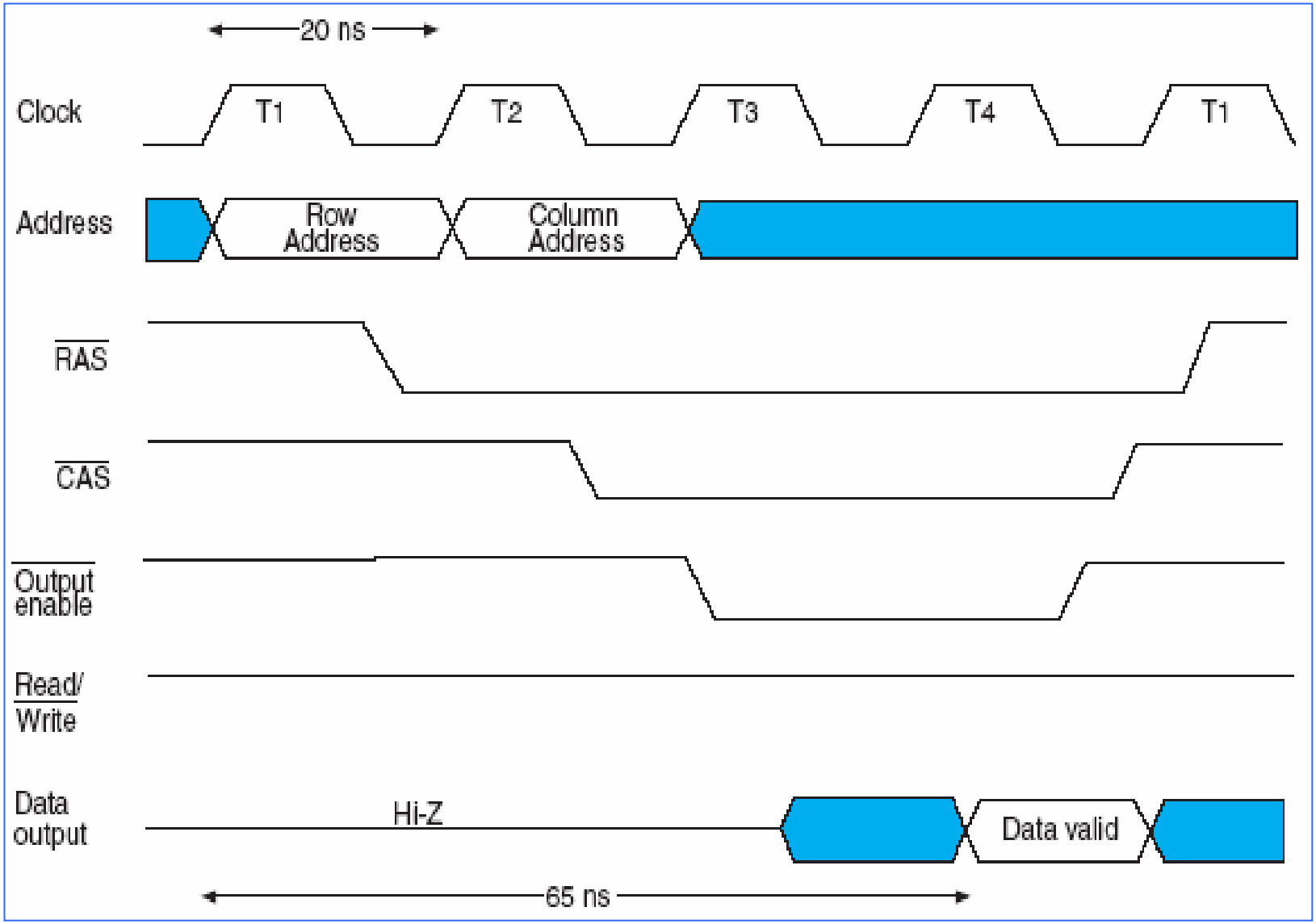
Dynamic RAM ICs: bit-slice model



DRAM Timing Diagram: Write cycle



DRAM Timing Diagram: Read cycle



Dynamic RAM ICs: Refreshing …

- There is a Refresh counter and a Refresh controller to support DRAM refreshing.
- Refresh counter is used to provide the address of the row of the DRAM cells to be refreshed. The Refresh counter advances one for each refresh cycle.
- The initiation of refresh is controlled externally by using the RAS' and CAS'.
- Each row is refreshed within a specified refresh time, typically in the range 16-64 ms.

NOTE: More on DRAM Refer http://www.pcguide.com/ref/ram/typesDRAM-c.html

Dynamic RAM ICs: Refreshing …

- Distribution refresh: refreshing at evenly spaced points
- Burst refresh: refreshing all rows one after another
- During any refresh cycle, no DRAM reads or writes can occur.
- Since use of burst refresh would halt the computer for a fairly long period, distribution refresh is more commonly used.
- SDRAM (Synchronous DRAM) operated with an external clock and does multiple reads from successive DRAM addresses corresponding to the same row in rapid succession, thus giving better performance.

Dynamic RAM ICs: Refreshing …

- There are three ways in which a refresh cycle can be triggered and hence, giving rise to three different refresh types.
- RAS only refresh: External DRAM controller supplies the refresh addresses, RAS is changed to 0.
- CAS before RAS refresh: The CAS is changed from 1 to 0 followed by a change from 1 to 0 on RAS. The refresh addresses come from the refresh counter, which is incremented after refresh for each cycle.
- Hidden refresh: Effectively, CAS before RAS refresh. The output data from prior read remains valid, hence the name. The time taken by hidden refresh is visible.

Array of RAM ICs

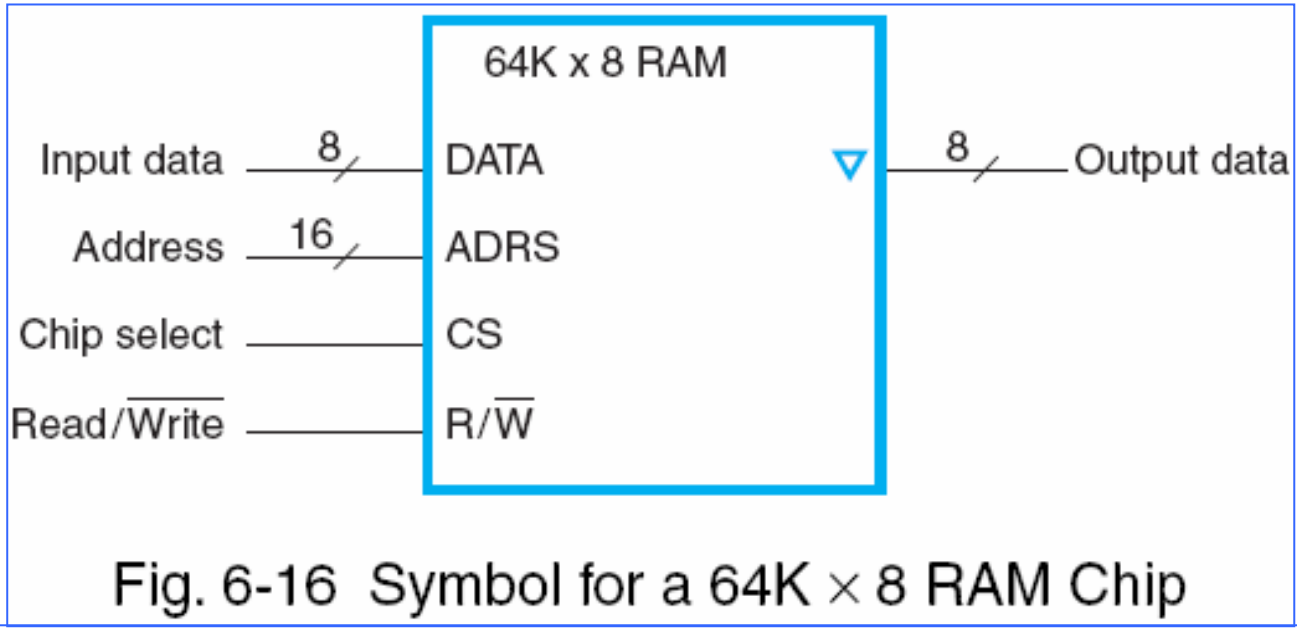
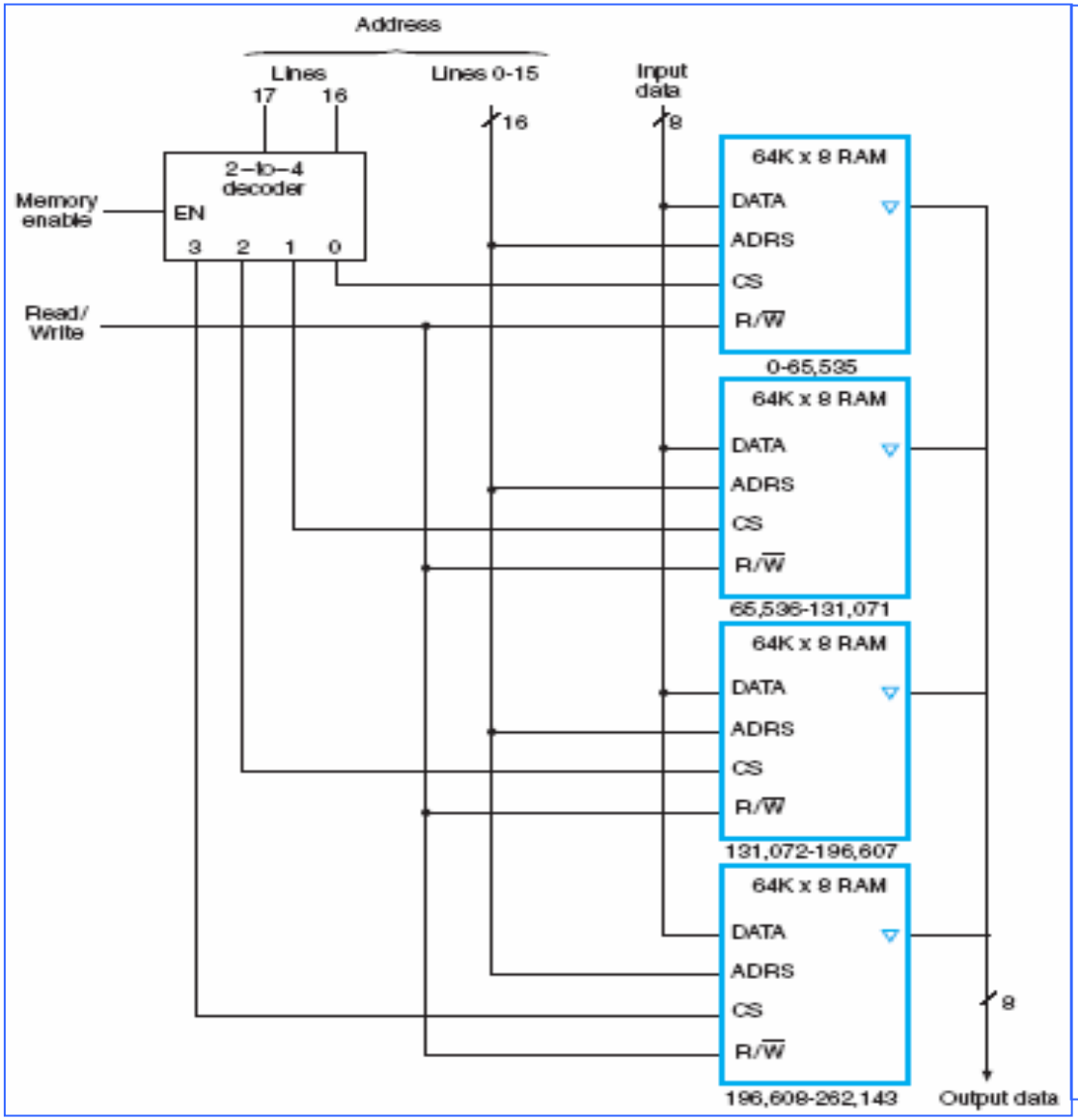


Fig. 6-16 Symbol for a 64K × 8 RAM Chip

- A RAM chip is shown with capacity of 64K words, 8 bits each.
- The chip select CS input selects the particular RAM chip and the Read/(Write)' specifies the operation when the chip is selected.
- When CS=0, chip is not selected, all data outputs are in the Hi-Z state. When CS=1, data output lines carry the eight bits of the selected word.
- Number of words in memory can be increased by using more RAM chips.

Array of RAM ICs …



16 and 17 needed as decoder inputs.

Decoder outputs are fed to the CS inputs of the four chips.

The memory is disabled when the decoder EN=0. All four outputs are zero, none of the chips is selected.

When decoder is enabled, lines 16 and 17 determine selected chip.

Array of RAM ICs …

It is possible to combine two chips to form a composite memory containing the same number of words, but with twice as many bits per word.

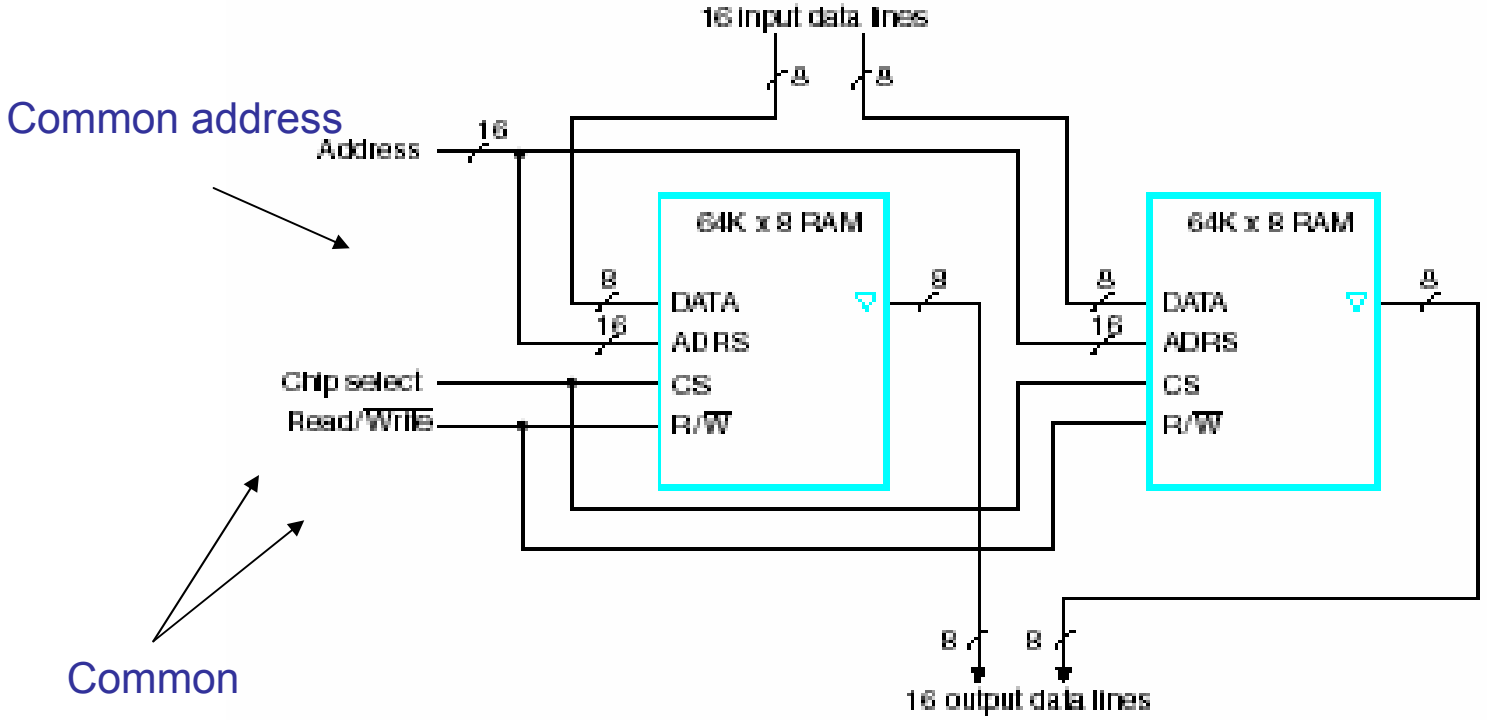


Fig. 6-18 Block Diagram of a 64K × 16 RAM

Arrays of RAM ICs: DRAM Controller

- DRAM controller is a complex synchronous sequential circuit with the external CPU clock providing synchronization of its operation.

- Following functions are performed by a DRAM controller:
  - Controlling separation of the address into a row address and a column address and providing these addresses at the required times.
  - Providing (RAS)' and (CAS)' signals (row, column access signals) at the required times for read, write and refresh operations.
  - Performing refresh operations at the necessary intervals.
  - Providing status signals to the rest of the system, for example, indicating whether the memory is busy performing refresh.

Programmable Logic Technologies

- Five types of PLDs, programmable logic devices:
  - ROM
  - PLA, programmable logic array
  - PAL, programmable array logic
  - CPLD, complex PLD
  - FPGA, field programmable gate array
- Programming technologies to control connections. First three are permanent.
- Use of fuse in each of the programmable points of the PLD having two states CLOSED and OPEN. Oldest programming technology. The fuse is blow by passing high current through application of high voltage.

Programmable Logic Technologies

- Mask programming, done at the last steps of chip fabrication process, where connections are made or not made in the metal layers serving as chip conductors.
- Antifuse, the opposite of a fuse, two conductors are separated by a material having a high resistance. This acts as an open circuit. By applying high voltage the antifuse is melted to provide low resistance, thus a closed path.
- Connection control using SRAM: A SRAM bit driving the gate of an MOS n-channel transistor at the programming point. If SRAM bit stores 1, then transistor is on / connection CLOSED. Otherwise, it is off / connection OPEN. This is volatile technology.

Programmable Logic Technologies

Programming technologies to build look-up tables:

Logic inputs are address inputs for reading the SRAM, logic outputs are the stored values for the addressed word that appears on the SRAM data outputs, store truth table in the SRAM, hence lookup table.

Programming technologies to control transistor switching:

Based on storing charge on a floating gate. Negative charge makes the transistor impossible to turn ON. Absence of that makes it possible to turn ON if a HIGH is applied to its regular gate. These technologies allow for reprogramming, thus ***erasable*** and ***electrically erasable*** technologies.

NOTE: Floating gate is located below the regular gate within an MOS transistor and is completely isolated by an insulating dielectric.

Read Only Memory: ROM

- ROM is a device where permanent binary information is stored.
- The information is specified by the designer and is then embedded into the ROM to form required interconnection or electronic device pattern.
- ROM is non volatile and hence information stays even if power supply is off.
- Inputs provide the memory address and the outputs give the data bits of the stored word that is selected by the address. **k** address input lines can specify 2^k words. ROM does not have data inputs.

ROM Block Diagram

Read Only Memory: Example

32x8 ROM, 32 words, 8 bits each. Five inputs to form binary numbers from 0– 31.

Each decoder output represents a memory address. The 32 outputs are connected through programmable connections to each of the 8 OR gates. Each OR gate must be considered as having 32 inputs. The ROM contains 32x8 = 256 programmable connections.

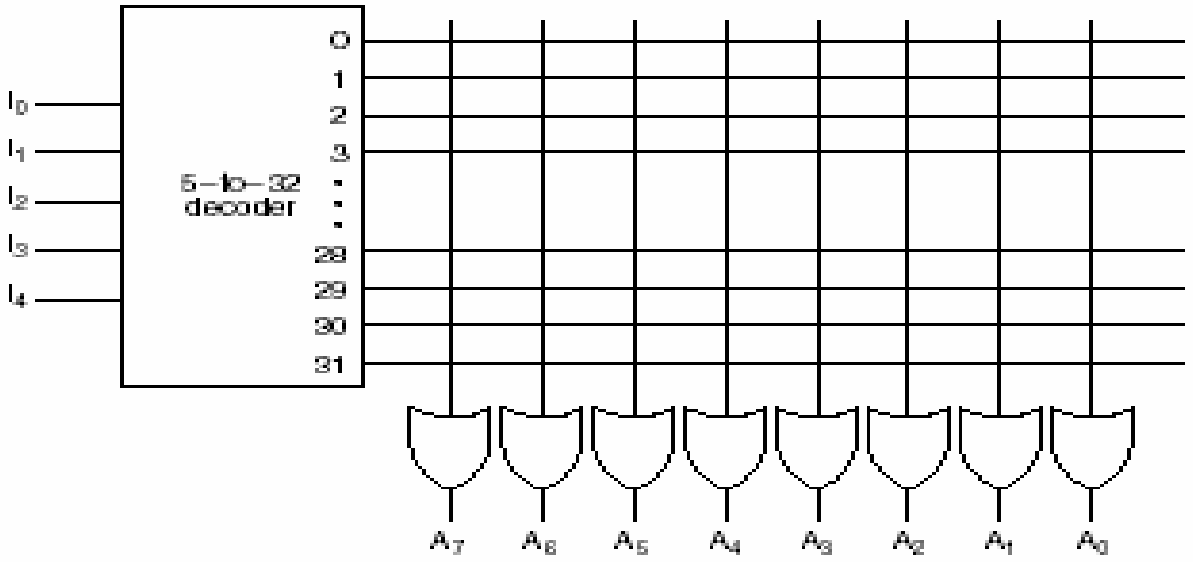


Fig. 6-20 Internal Logic of a 32 × 8 ROM

In general, a **2^kxn** ROM will have an internal **k-to-2^k** line decoder and **n** OR gates, each having **2^k** inputs.

Read Only Memory: Truth Table

- The internal storage of a ROM is specified by a truth table.
- The truth table shows the contents of a word in each address.

ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
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1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Table 6-2 ROM Truth Table (Partial)

Read Only Memory: Programming

- Hardware procedure programs the ROM with connections that follow the truth table.
- Every 0 specifies an OPEN circuit and every 1 specifies a CLOSED circuit.
- Example: the 8-bit word 10110010 for permanent storage at input address 00011. (1's are marked with x in diagram)

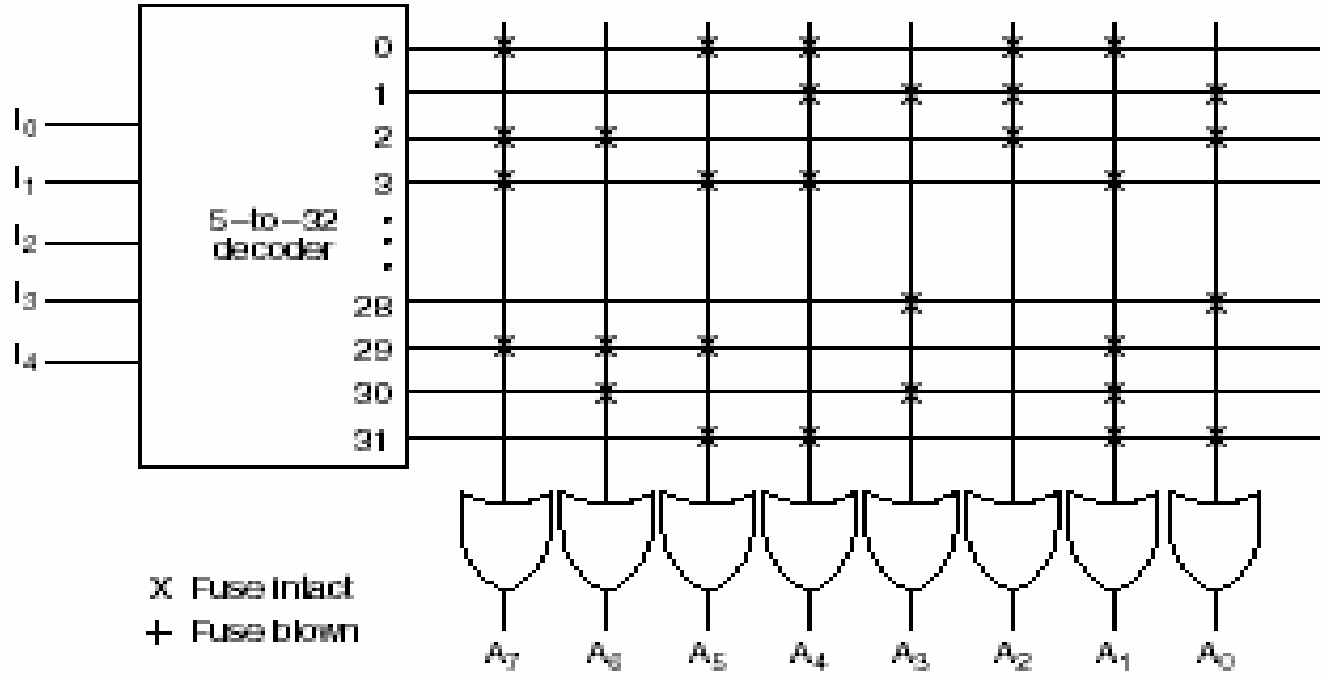

Fig. 6-21 Programming the ROM According to Table 6-2

Read Only Memory: Example

Design a combinatorial circuit using a ROM that accepts a 3-bit number and generates an output equal to the square of the input number.

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Table 6-3 Truth Table for Circuit of Example 6-1

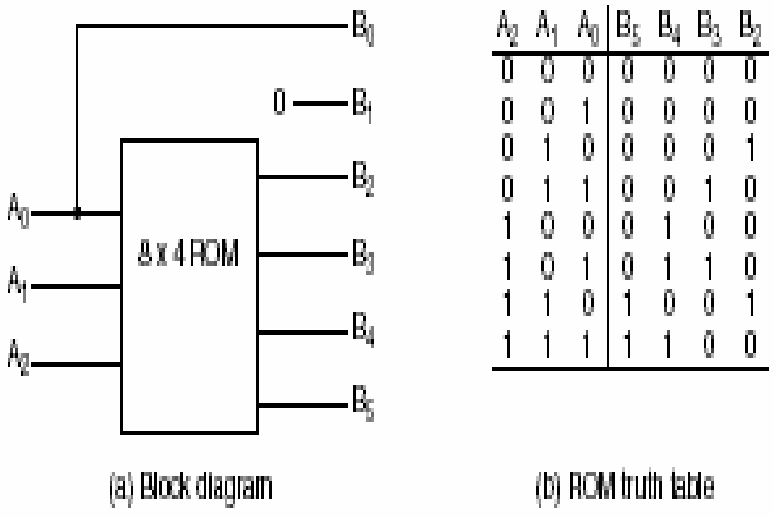

Fig. 6-22 ROM Implementation of Example 6-1

ROM that can be programmed using fuse is called programmable ROM (PROM): EPROM and EEPROM.