Registers and Counters

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- Registers and Counters Basics
- Registers
- Shift Registers
- Ripple Counter
- Synchronous Binary Counter
- Other Counters

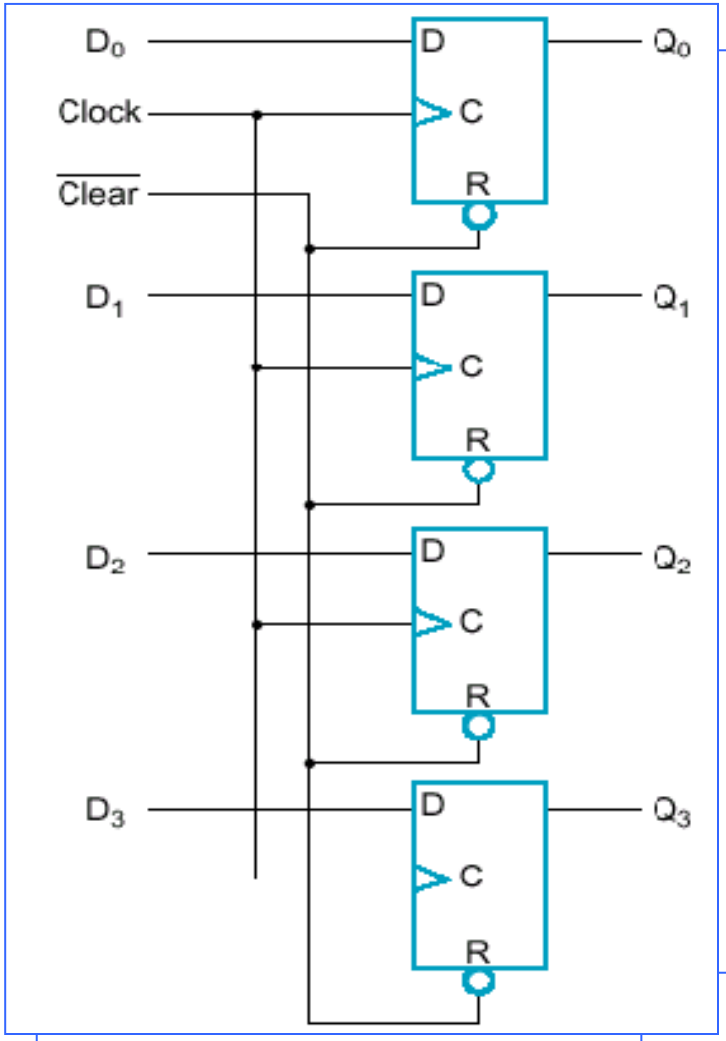
Sources

- Logic and Computer Design Fundamentals (2nd edition) by M. M. Mano and C. R. Kime.
- Lecture notes of Dr. John Y. Cheung, School of Electrical and Computer Engineering, University of Oklahoma.
- Dr. Valavanis lectures

Registers and Counters: Basics

- Combinatorial and sequential circuits are brought together to result in sequential functional blocks, referred to as registers and counters.
- Registers are useful for storing and manipulating information.
- Counters are employed in circuits that sequence and control operations in a digital system.
- Register consists of a set of flip-flops, together with gates that implement their state transitions. Since each FF is capable of storing one bit information, an n-bit register constructed using n FFs can store n bits of binary information.
- Counter – A register that goes through a predetermined sequence of states upon the application of clock pulses.

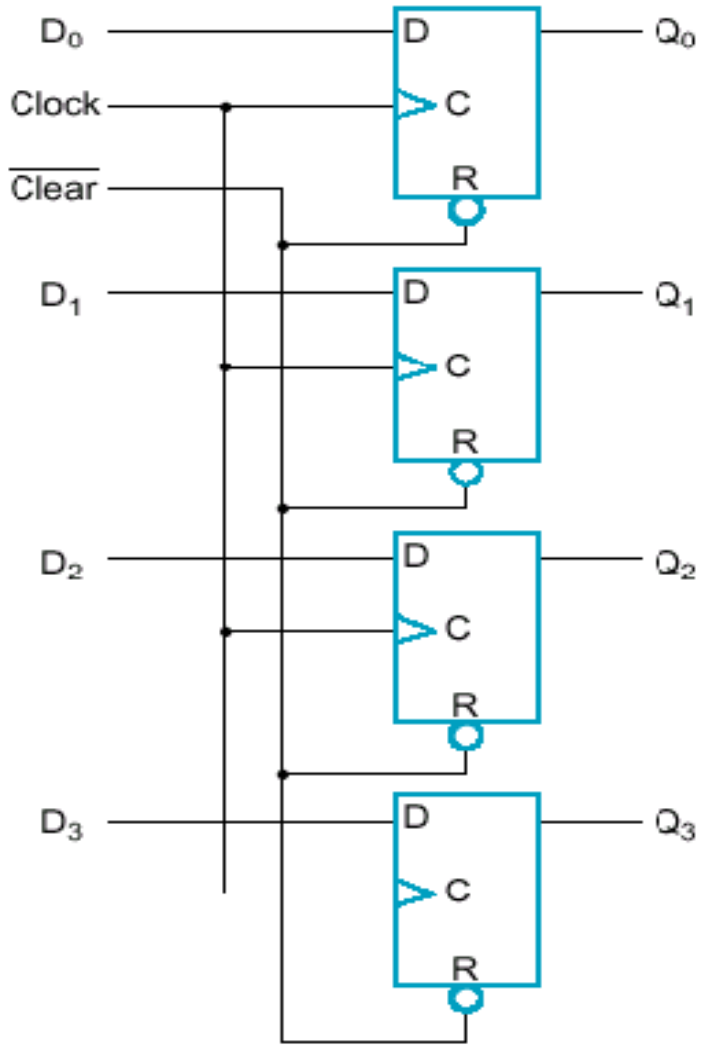
Registers: in Simplest form



Register with 4 D-type FF

- Simplest register– A register that consists of only flip-flops without external gates.
- Common **Clock** input triggers all FFs on the rising edge of each pulse, and the binary data available at the four **D** inputs are transferred into the 4-bit register.
- The four **Q** outputs can be sampled to obtain the binary information stored in the register.

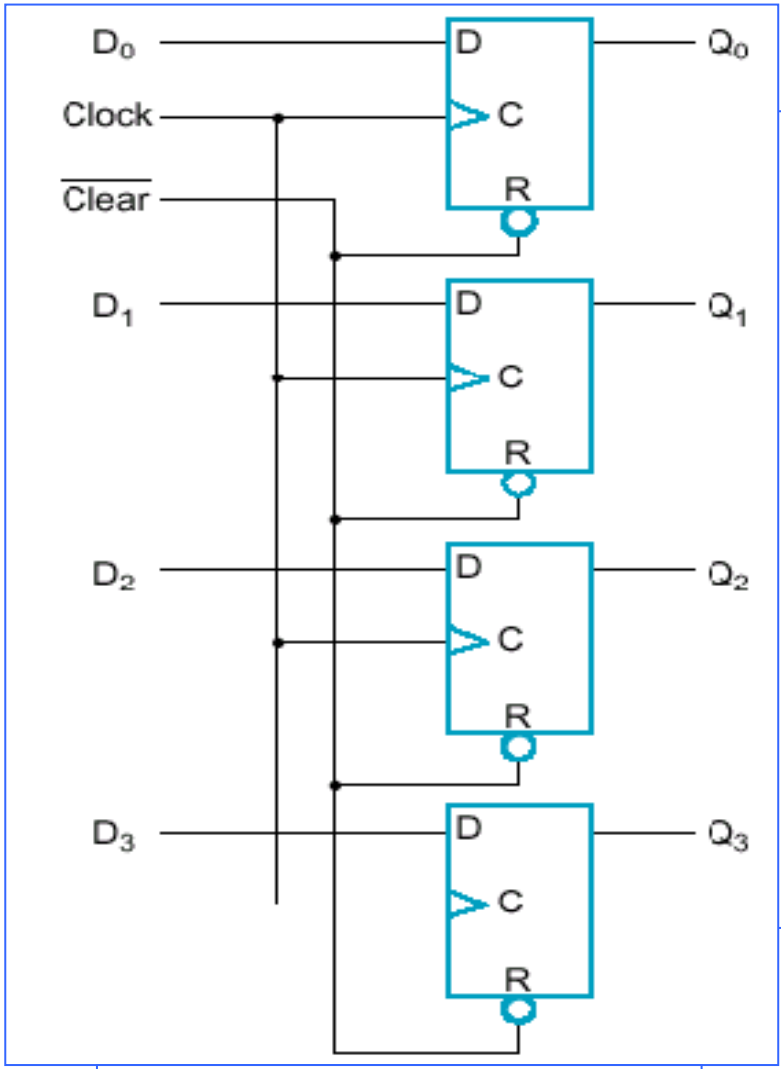
Registers: in Simplest form ….



Register with 4 D-type FF

- The **(Clear)'** is useful for clearing the register to all 0's prior to its clocked operation. A 0 must be applied to it to cause all FF to reset asynchronously.
- Activation of the asynchronous **R'** inputs to FF during normal clocked operation can lead to circuit designs that are highly delay dependent, and thus malfunctioning. So, we maintain **(Clear)'** at logic 1 during normal clocked operation, allowing this to be 0 for system reset.

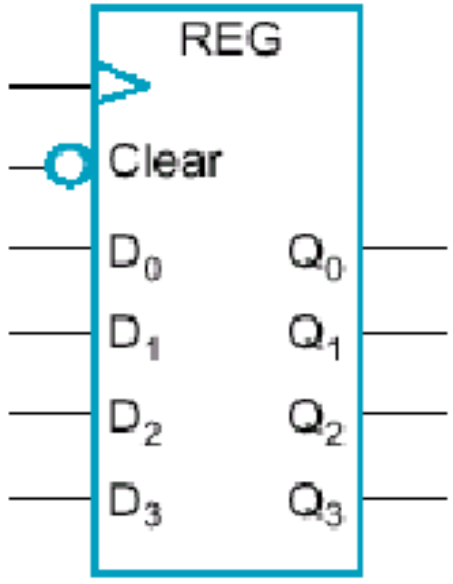
Registers: in Simplest form ….



Register with 4 D-type FF

- **Loading** the register: Transfer of new information into a register.
- **Parallel loading**: Loading all the bits of the register simultaneously with a common clock pulse.
- Most digital systems have a master clock generator that supplies a continuous train of clock pulses, applied to all FF and registers.

Registers: Symbol

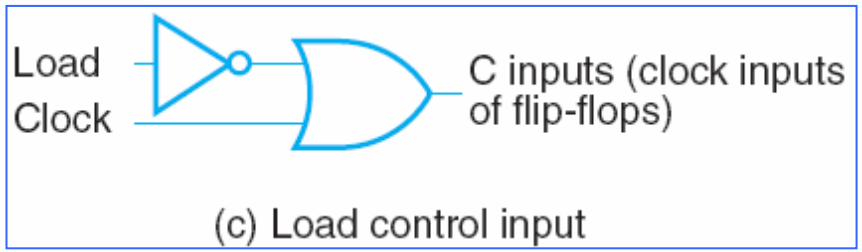


Register Symbol

- Symbol permits the use of register in a design hierarchy.
- Inputs are at the left and outputs are at the right.
- The clock input with a dynamic indicator represents positive edge-triggering.
- The clear symbol with a bubble indicate that logic 0 clears the FFs.
- If clear has to be written outside the symbol, then it should be written as **(Clear)'**.

Registers: Load and Clock

- The systems masters clock acts like a heart that supplies constant beat to all parts of the system.
- In order to preserve the contents of the registers this masters clock should not be given directly as the FF clock inputs.
- So, implementation with a load control input **Load (L)** combined with the clock as shown:



(c) Load control input

- The output of the OR gate is applied to the **C** inputs of the register FF.

C inputs = (Load)' + Clock

When **Load = 1**, **C inputs = Clock**, register is clocked normally, new info can be transferred into the register on the positive transitions of the clock. When **Load = 0, C inputs = 1**, no positive transitions so register contents remain unchanged.

Registers: Load and Clock ….

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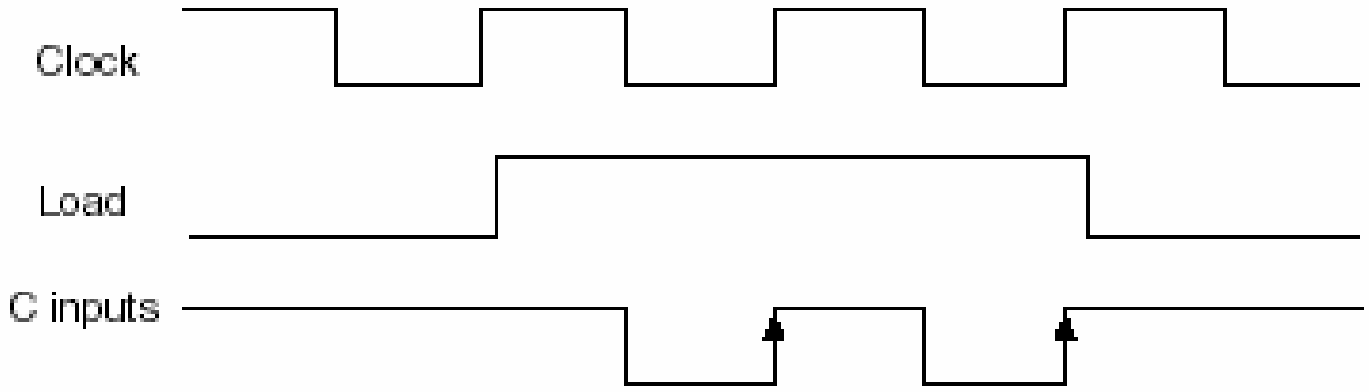
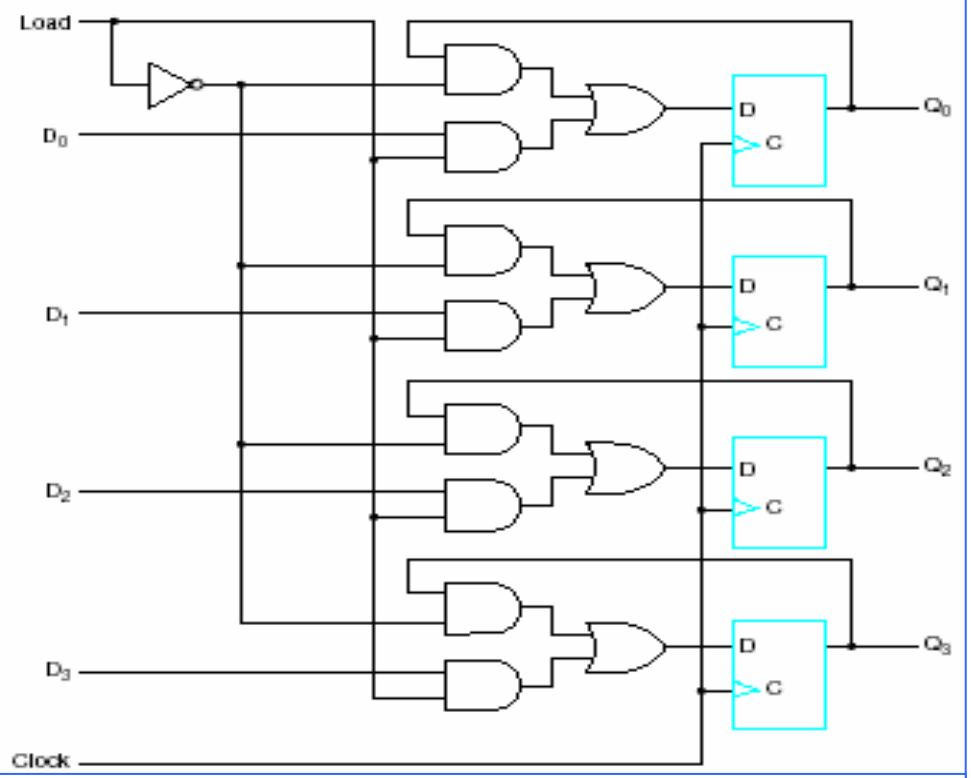


(d) Timing diagram

Register: with parallel load



With each clock pulse, the D input determines the next state of the output. To leave the output unchanged, it is necessary to make the D input equal to the present value of the output.

A 4-bit register with a control input **Load** directed through gates into the **D** inputs of the FF, instead of through clock gating on the **C** inputs. **Load** input determines the action to be taken.

When **Load =1**, data on the four inputs is transferred into the register with the next positive transition of the clock pulse.

When **Load =0**, data inputs are blocked.

Feedback is necessary because the D FF does not have a "no change" input condition.

Shift Registers

- A register capable of shifting its stored bits laterally in one or both directions.
- Logical configuration consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive a common clock pulse, which activates the shift from each stage to the next.
- Simplest possible shift register is the one that uses only FF.

Shift Registers …

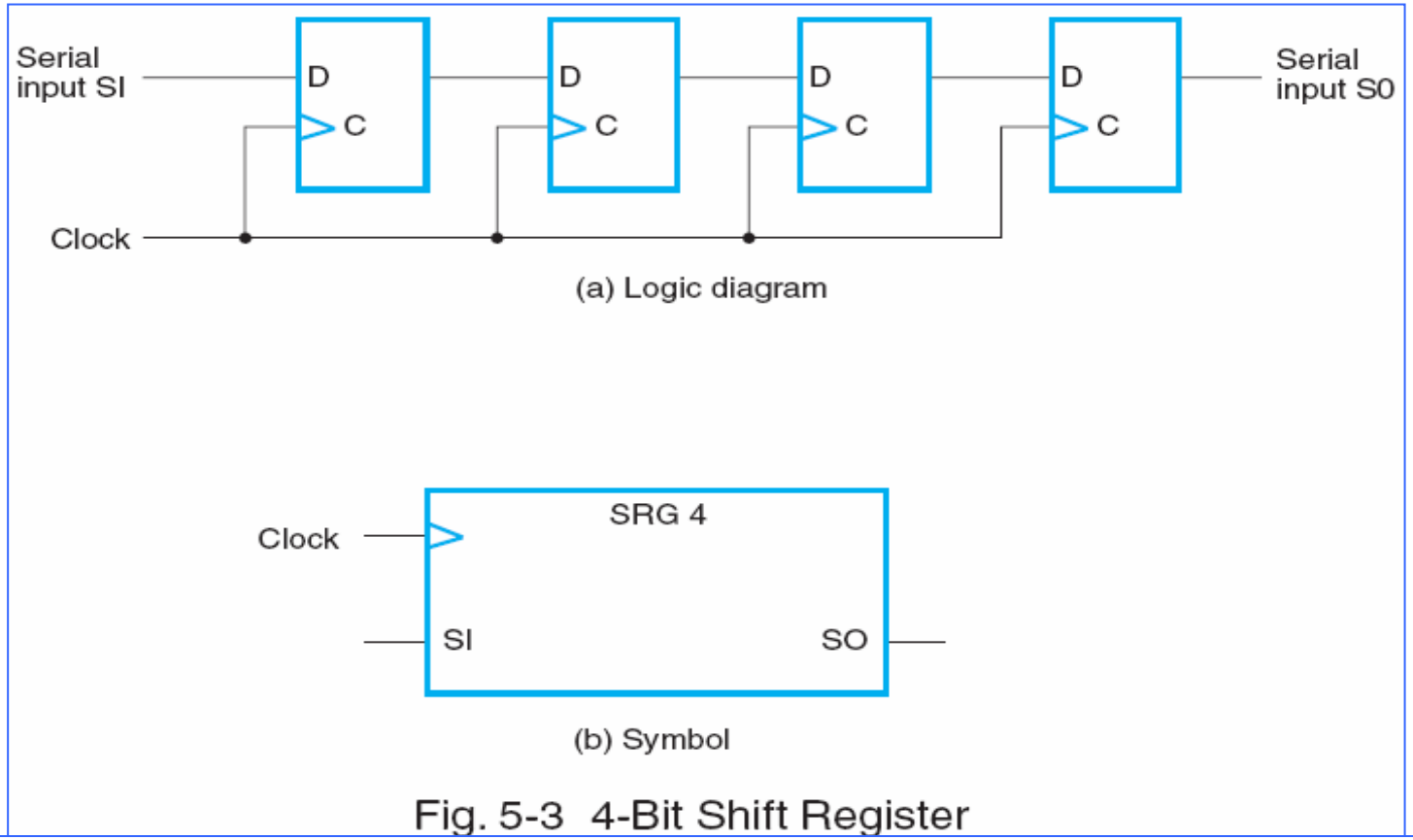
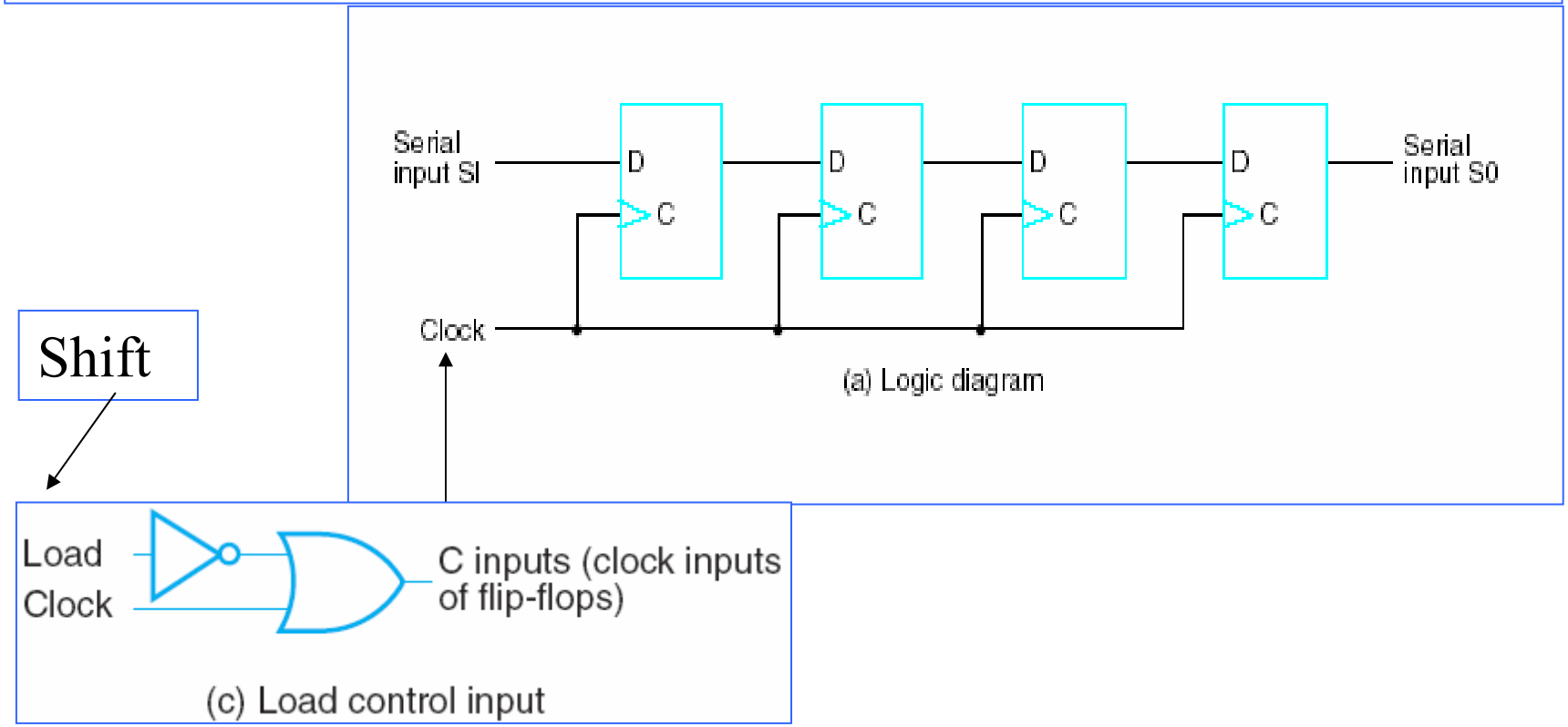


Fig. 5-3 4-Bit Shift Register

- Output of a given FF is connected to the D input of the FF at its right. Common clock to all FF.
- Serial input SI is the input to the leftmost flip-flop during the shift.
- Serial output SO is taken from the output of the rightmost flip-flop.

Shift Registers …

Sometimes it is necessary to control the shift so that it occurs only with certain pulses, but not with others. In this case, shift can be controlled by connecting the clock through the logic shown, with **Shift** replacing **Load**.



Shift Registers: Serial Transfer

- A digital system is said to operate in a serial mode when information in the system is transferred or manipulated one bit at a time.
- Transfer one bit at a time– Shift the bits out of one register and into a second register.
- Contrast with Parallel: Transfer all bits at the same time.

Parallel Vs Serial

- Operations in digital computers are generally parallel, due to faster speed attainable.
- Serial operations are slower and require lesser hardware.

Shift Registers: Serial Transfer …

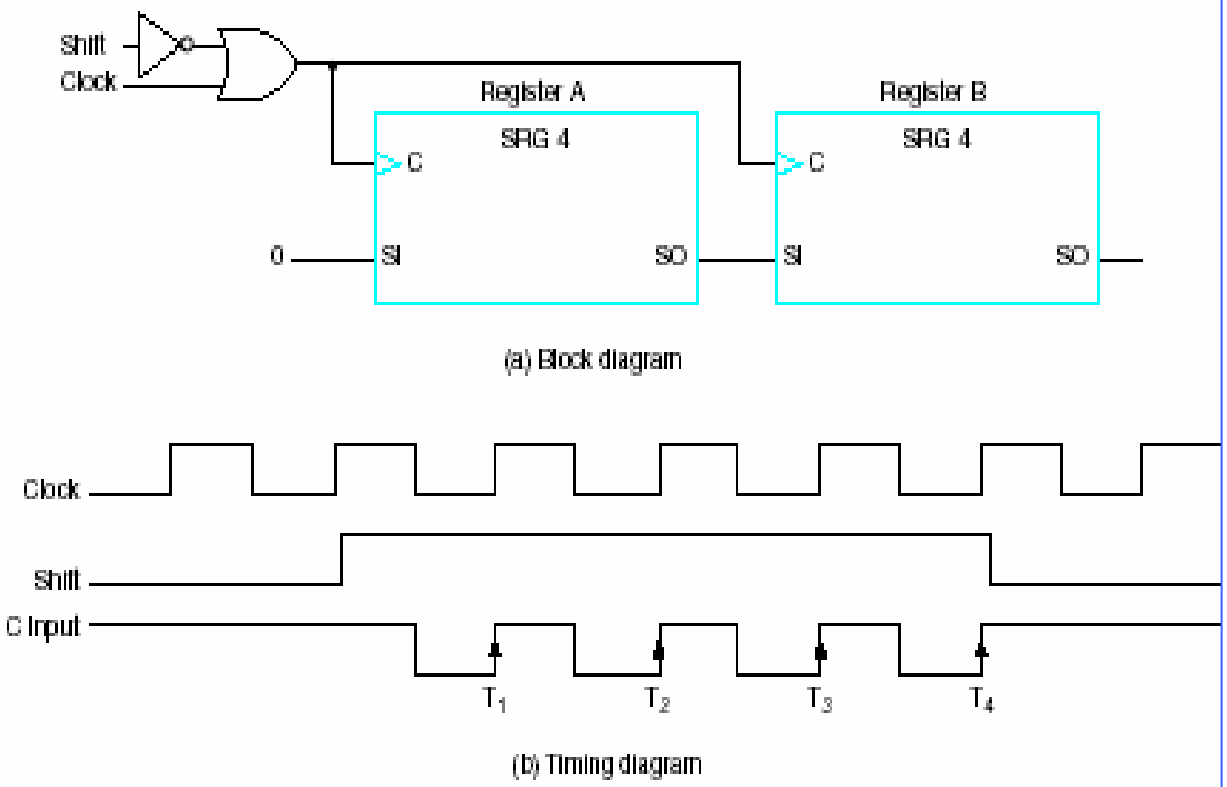


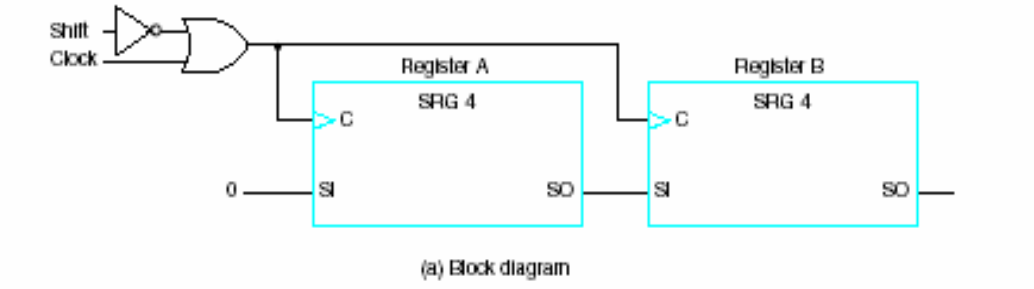
Fig. 5-4 Serial Transfer

- Serial output of A connected to serial input of B.
- SI of A receives 0's while its data are transferred to B.
- Also possible for A to receive other binary information.
- Initial content of B is shifted out through its SO and it is lost, unless transferred back to A.
- By connecting A's serial output to its serial input, info can be circulated back into the register.

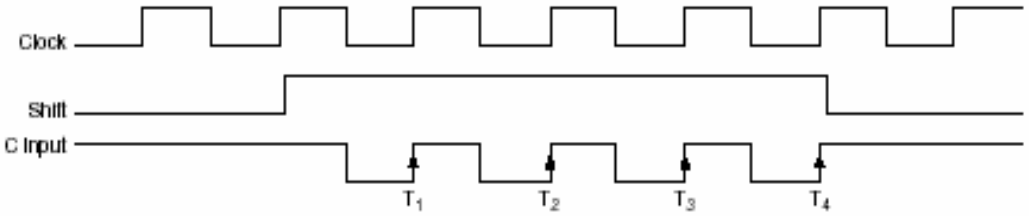
Shift determines when and how many times registers are shifted.

Clock pulses pass to the shift register clock inputs only when **Shift = 1**.

Shift Registers: Serial Transfer Example



(a) Block diagram



(b) Timing diagram

Timing pulse	Shift Register A				Shift Register B			
Initial value	1	0	1	1	0	0	1	0
After T_1	0	1	0	1	1	0	0	1
After T_2	0	0	1	0	1	1	0	0
After T_3	0	0	0	1	0	1	1	0
After T_4	0	0	0	0	1	0	1	1

Table 5-1 Example of Serial Transfer

Each shift register has four stages.

Logic that supervises the transfer must be designed to enable shift registers through **Shift** for a fixed time of 4 clock pulses. 4 pulses find **Shift** in the active state, so that output of the logic connected to the clock inputs of the registers produces 4 pulses $T_1 - T_4$.

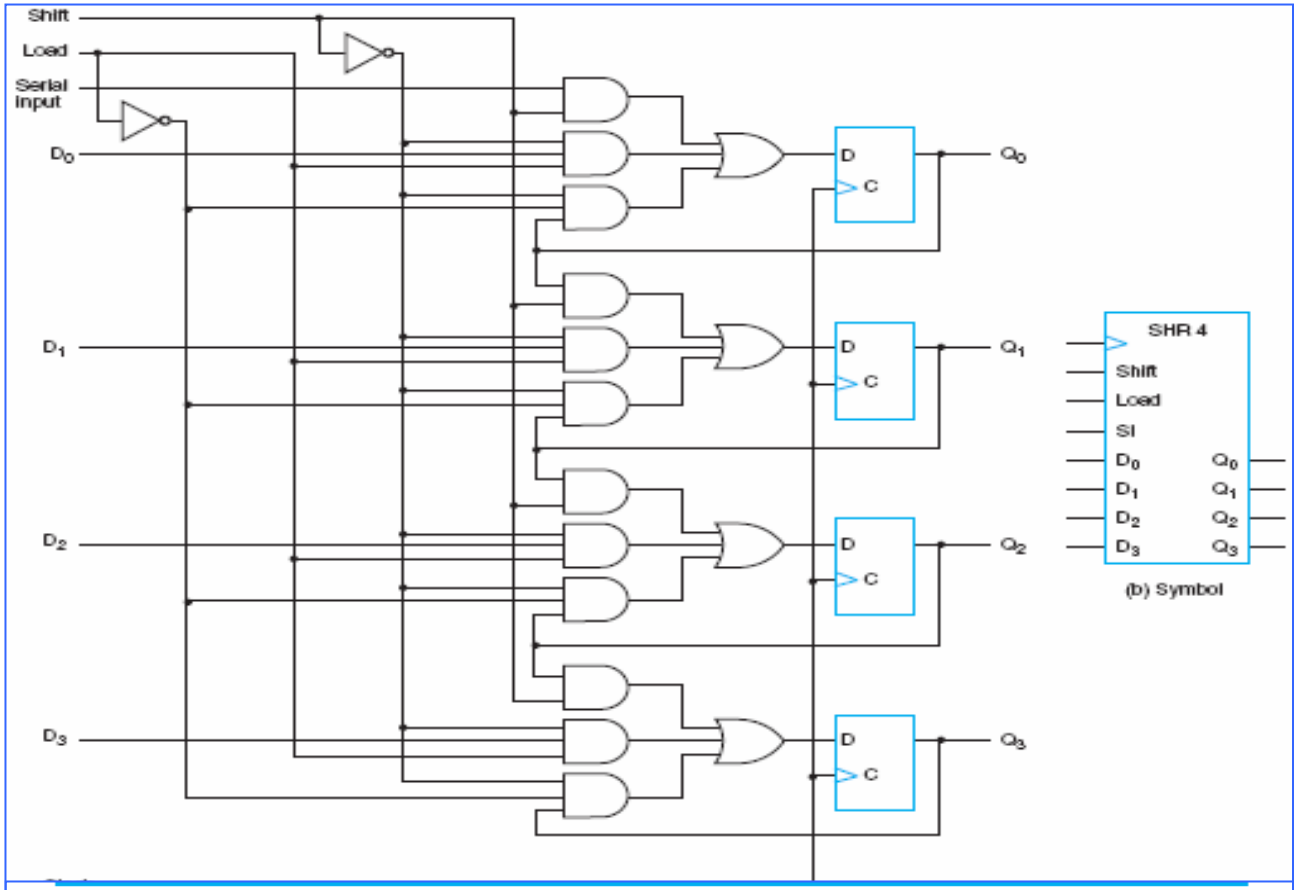
Each positive transition of these pulses causes a shift in both registers. After that **Shift** changes back to 0 and shift registers are disabled.

Example: A (1011), B(0010), SI of A is logic 0.

Shift Register: with Parallel Load

- If a parallel load capability is also added to shift register, then data entered in parallel can be taken out in serial fashion by shifting out the data in the register.
- Shift register with accessible flip-flop outputs and parallel load can be used for converting incoming parallel data to outgoing serial data and vice versa.
- Shift registers are often used to interface digital systems that are situated remotely from each other.

Shift Register: with Parallel Load …



Shift	Load	Operation
0	0	No change
0	1	Load parallel data
1	×	Shift down from Q_0 to Q_3

Table 5-2 Function Table for the Register of Figure 5-6

Shift Register: Bi-directional

- Unidirectional shift register – A register capable of shifting in one direction.
- Bi-directional shift register – A register capable of shifting in both directions.

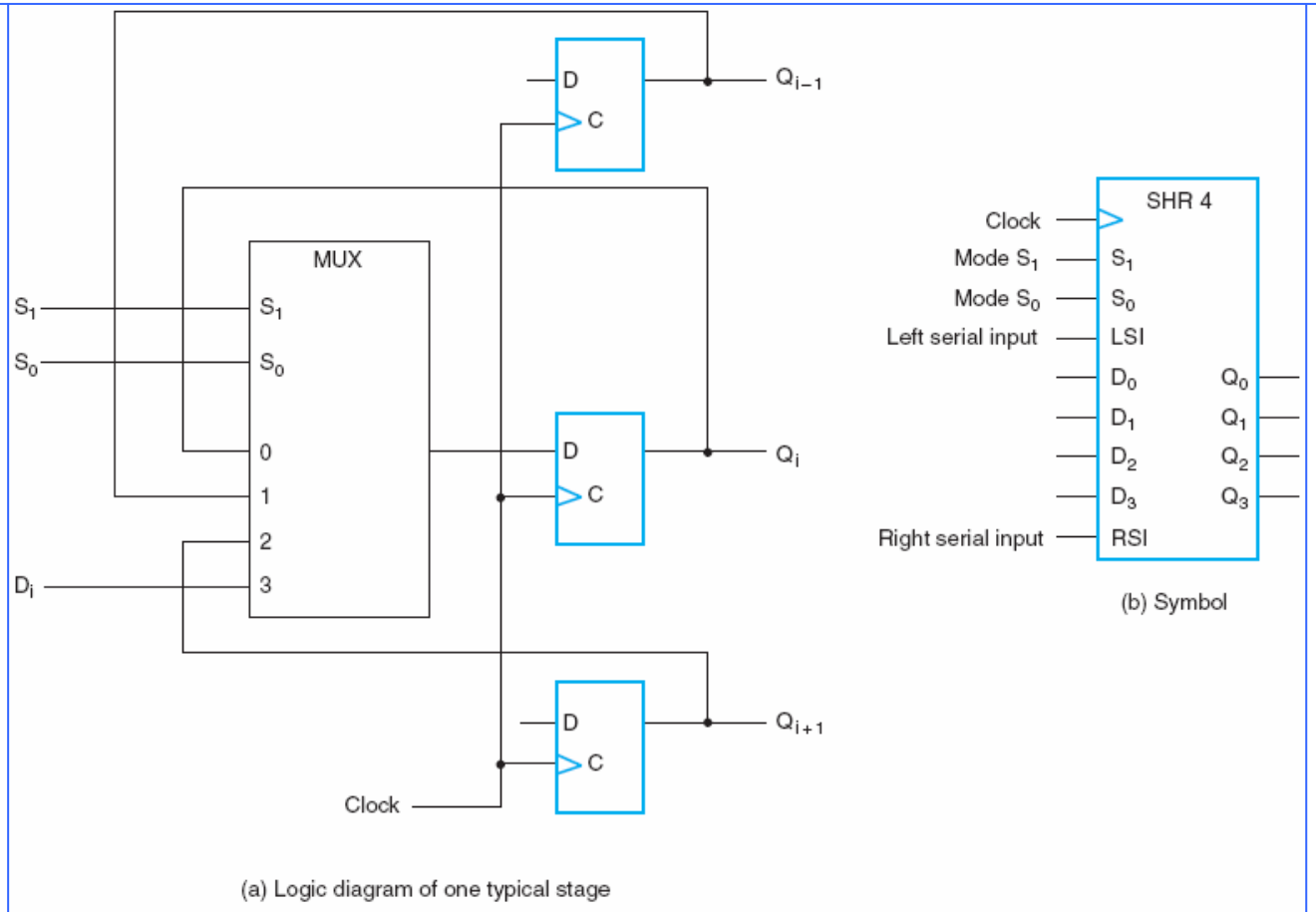
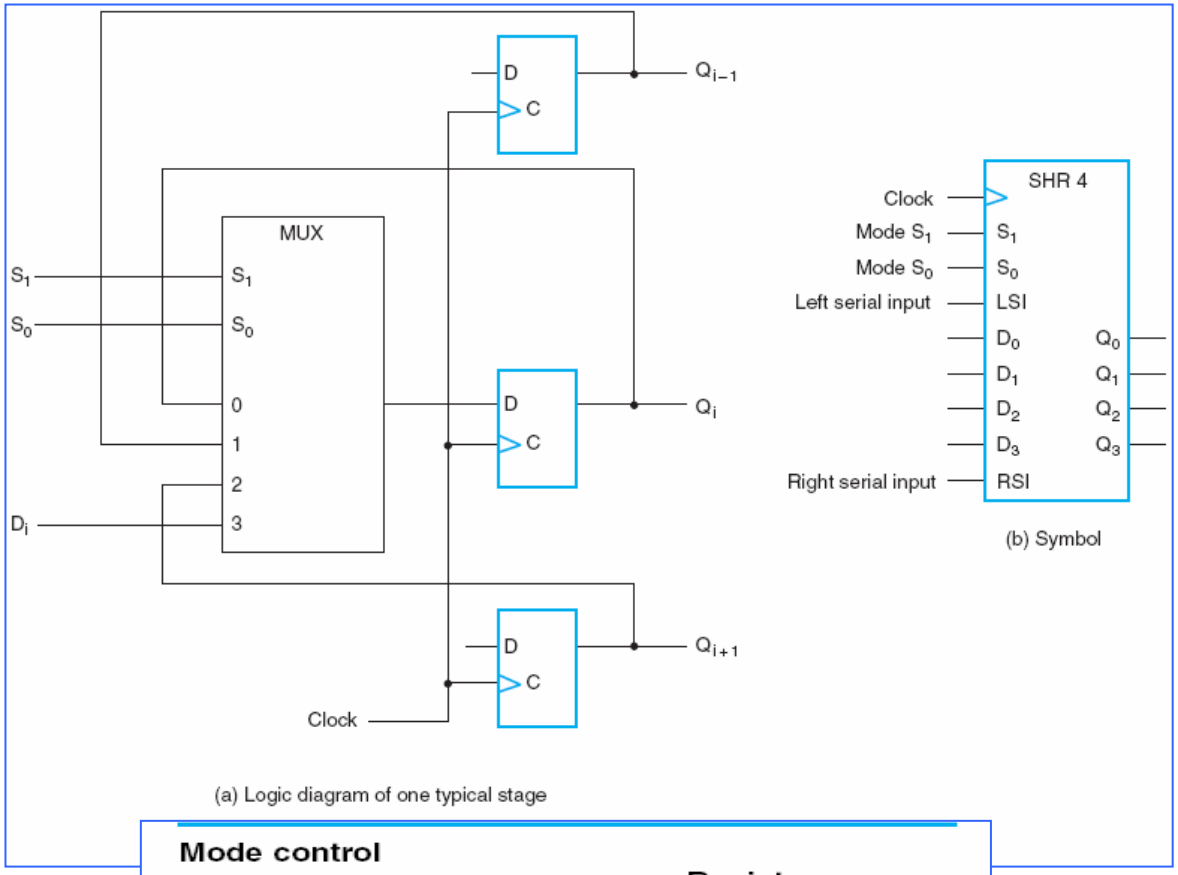


Fig. 5-7 Bidirectional Shift Register with Parallel Load

Shift Register: Bi-directional …



(a) Logic diagram of one typical stage

Mode control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift down
1	0	Shift up
1	1	Parallel load

Table 5-3 Function Table for the Register of Figure 5-7

Applications of Shift Registers

- Use of shift registers are common in digital systems.
- Typical uses include, Registering and Shifting.
- Registering: The most common application for a shift register is to hold a series of bits or an operand for later processing.
- Shifting operations are frequently used for many type of operations including:
  - Shifting
  - Multiplication
  - Division
  - Scaling
  - Serial to Parallel Conversion
  - Parallel to Serial Conversion

Shift Registers: Serial Addition

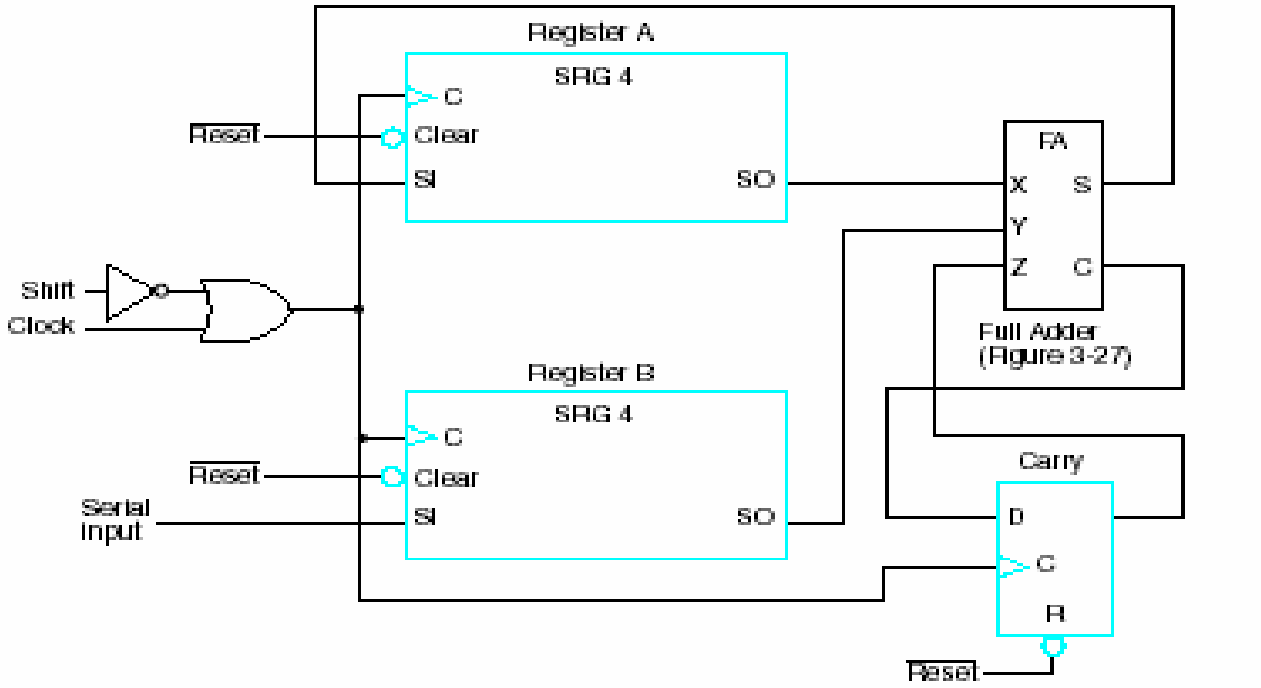


Fig. 5-5 Serial Addition

- Register A holds the augend, register B holds the addend.
- The carry flip-flop is reset to 0.
- Serial outputs of A and B provide a pair of significant bits for the full adder at X and Y.
- Output of the carry flip-flop provides the carry input at Z.

Counters: Basics

- A counter is a sequential machine that produces a specified count sequence. The count changes whenever the input clock is asserted.
- There is a great variety of counters based on its construction.
  - Clock: Synchronous or Asynchronous
  - Clock Trigger: Positive edged or Negative edged
  - Carry: Ripple or Parallel
  - Counts: Binary, Decade, Arbitrary
  - Count Direction: Up, Down, or Up/Down
  - Flip-flops: JK or T or D
- A Binary follows the binary number sequence. An n-bit binary counter consists of n flip-flops and can count in binary from 0 through $2^n - 1$.

Ripple Counter

- Ripple Counter: Flip-flop output transition serves as a source for triggering other flip-flops, i.e. C input of some or all of the FFs is triggered not by common clock pulse, but by transition of other FFs, leading to Asynchronous behavior.
- Advantage: Simple hardware.
- Disadvantage: Asynchronous circuits,

Ripple Counter …

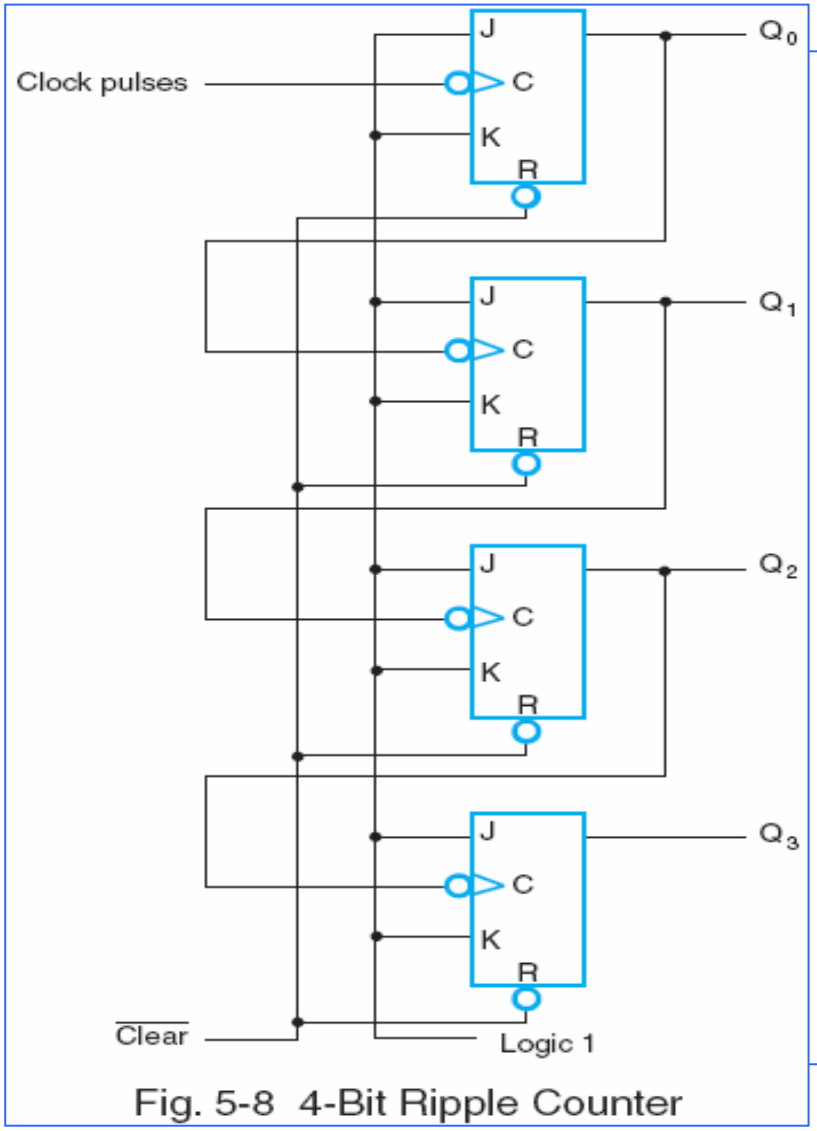


Fig. 5-8 4-Bit Ripple Counter

J and K's being connected to logic 1 and negative-edge triggering make each FF complement its value if the signal on its C input goes through a negative transition. Negative transition occurs when the output of the previous ff to which C is connected goes from 1 to 0. A 0-level signal on (Clear)' driving the R' inputs clears the register to 0 asynchronously.

Ripple Counter …

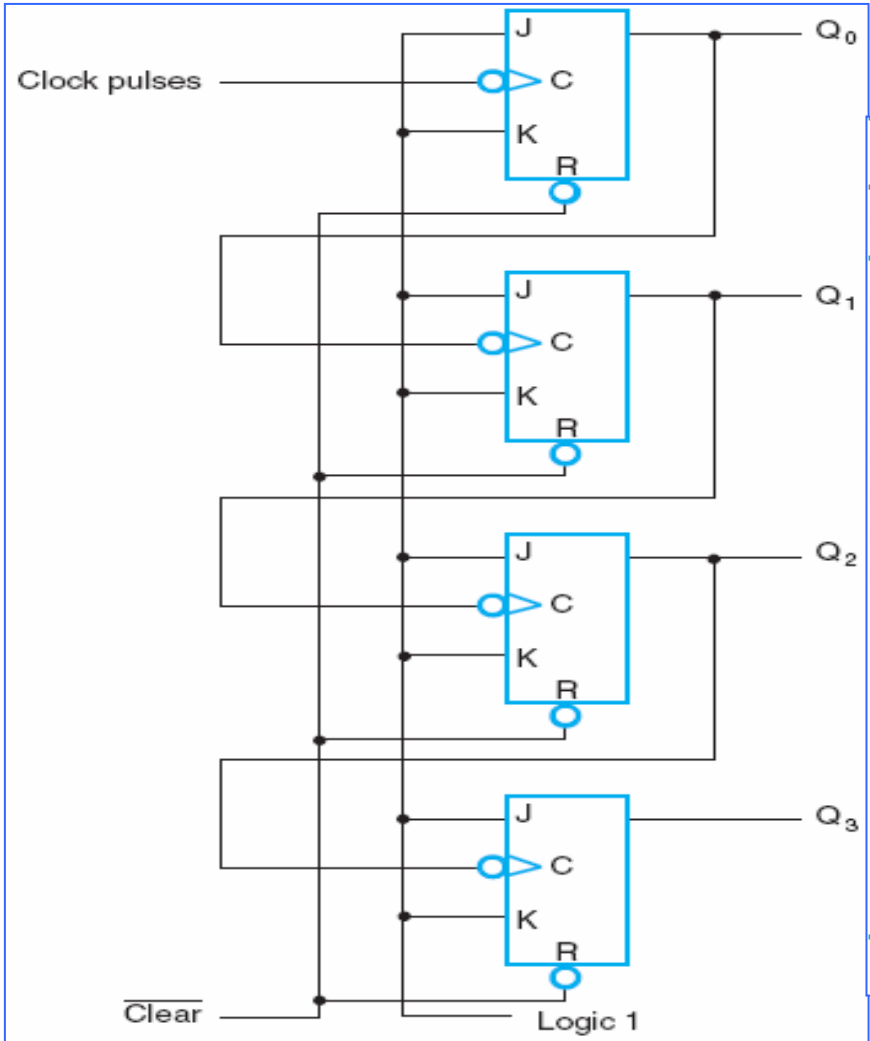


Fig. 5-8 4-Bit Ripple Counter

Upward Counting Sequence				Downward Counting Sequence			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	0
0	0	1	0	1	1	0	1
0	0	1	1	1	1	0	0
0	1	0	0	1	0	1	1
0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	0	0	0	0	1	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

Table 5-4 Counting Sequence of Binary Counter

Design of Synchronous binary Counters

Design procedure for a synchronous counter is the same as with any other synchronous sequential circuit. Counter may operate without external input, except for the clock pulses. Counter output taken from FF outputs without any additional outputs from gates. In the absence of inputs, counter state table will consist of columns for the present state and next state only.

Outputs implicitly represented by the present state column.

Present state				Next state				Flip-flop inputs							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_{Q3}	K_{Q3}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
0	0	0	0	0	0	0	1	0	×	0	×	0	×	1	×
0	0	0	1	0	0	1	0	0	×	0	×	1	×	×	1
0	0	1	0	0	0	1	1	0	×	0	×	×	0	1	×
0	0	1	1	0	1	0	0	0	×	1	×	×	1	×	1
0	1	0	0	0	1	0	1	0	×	×	0	0	×	1	×
0	1	0	1	0	1	1	0	0	×	×	0	1	×	×	1
0	1	1	0	0	1	1	1	0	×	×	0	×	0	1	×
0	1	1	1	1	0	0	0	1	×	×	1	×	1	×	1
1	0	0	0	1	0	0	1	×	0	0	×	0	×	1	×
1	0	0	1	1	0	1	0	×	0	0	×	1	×	×	1
1	0	1	0	1	0	1	1	×	0	0	×	×	0	1	×
1	0	1	1	1	1	0	0	×	0	1	×	×	1	×	1
1	1	0	0	1	1	0	1	×	0	×	0	0	×	1	×
1	1	0	1	1	1	1	0	×	0	×	0	1	×	×	1
1	1	1	0	1	1	1	1	×	0	×	0	×	0	1	×
1	1	1	1	0	0	0	0	×	1	×	1	×	1	×	1

Table 5-5 State Table and Flip-Flop Inputs for Binary Counter

Next state = present state + one

Design of Synchronous binary Counters …

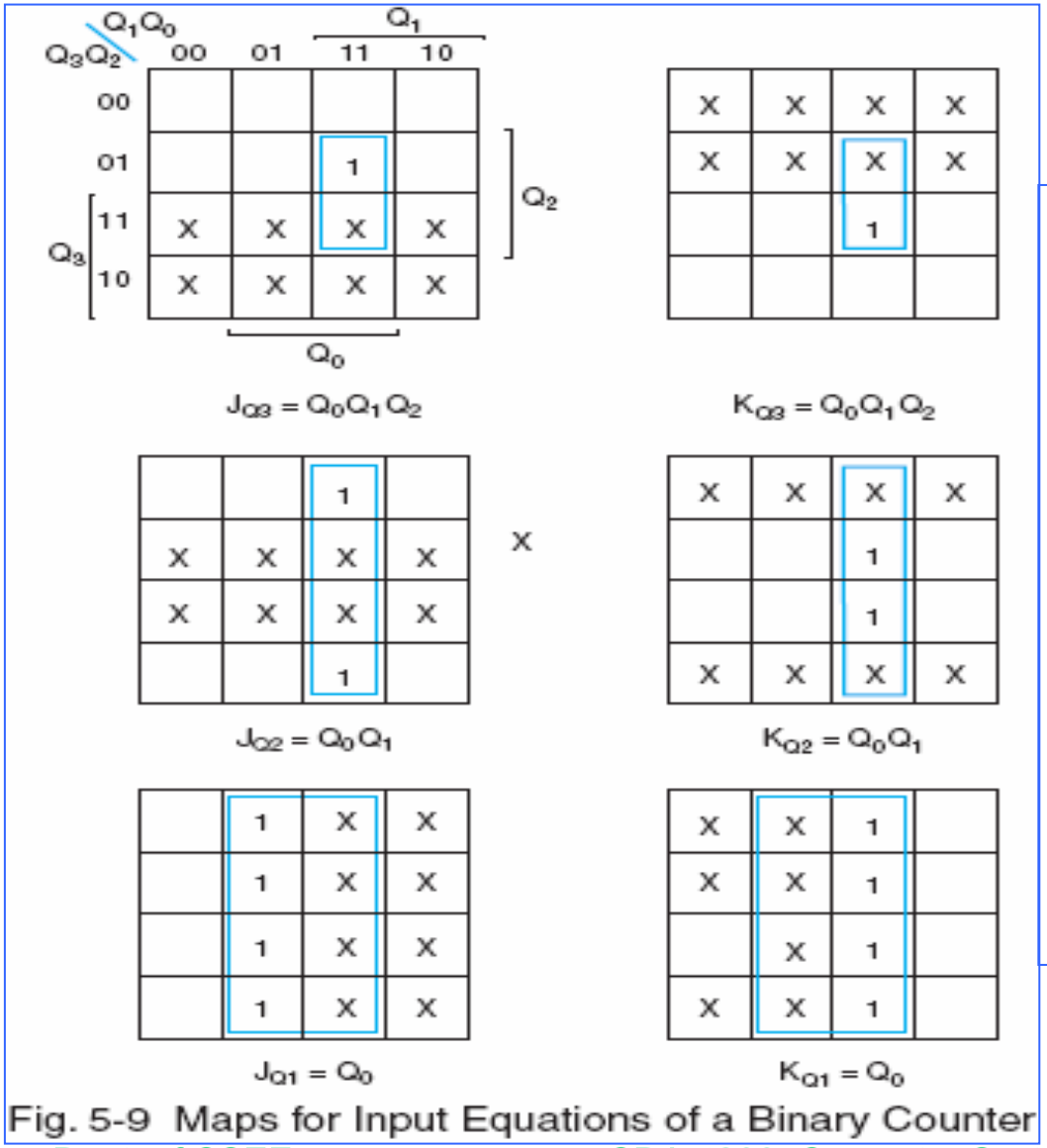


Fig. 5-9 Maps for Input Equations of a Binary Counter

Introducing a enable variable EN the FF input equations can be written as:

$$J_{Q0} = K_{Q0} = EN$$

$$J_{Q1} = K_{Q1} = Q_0.EN$$

$$J_{Q2} = K_{Q2} = Q_0.Q_1.EN$$

$$J_{Q3} = K_{Q3} = Q_0.Q_1.Q_2.EN$$

Design of Synchronous binary Counters …

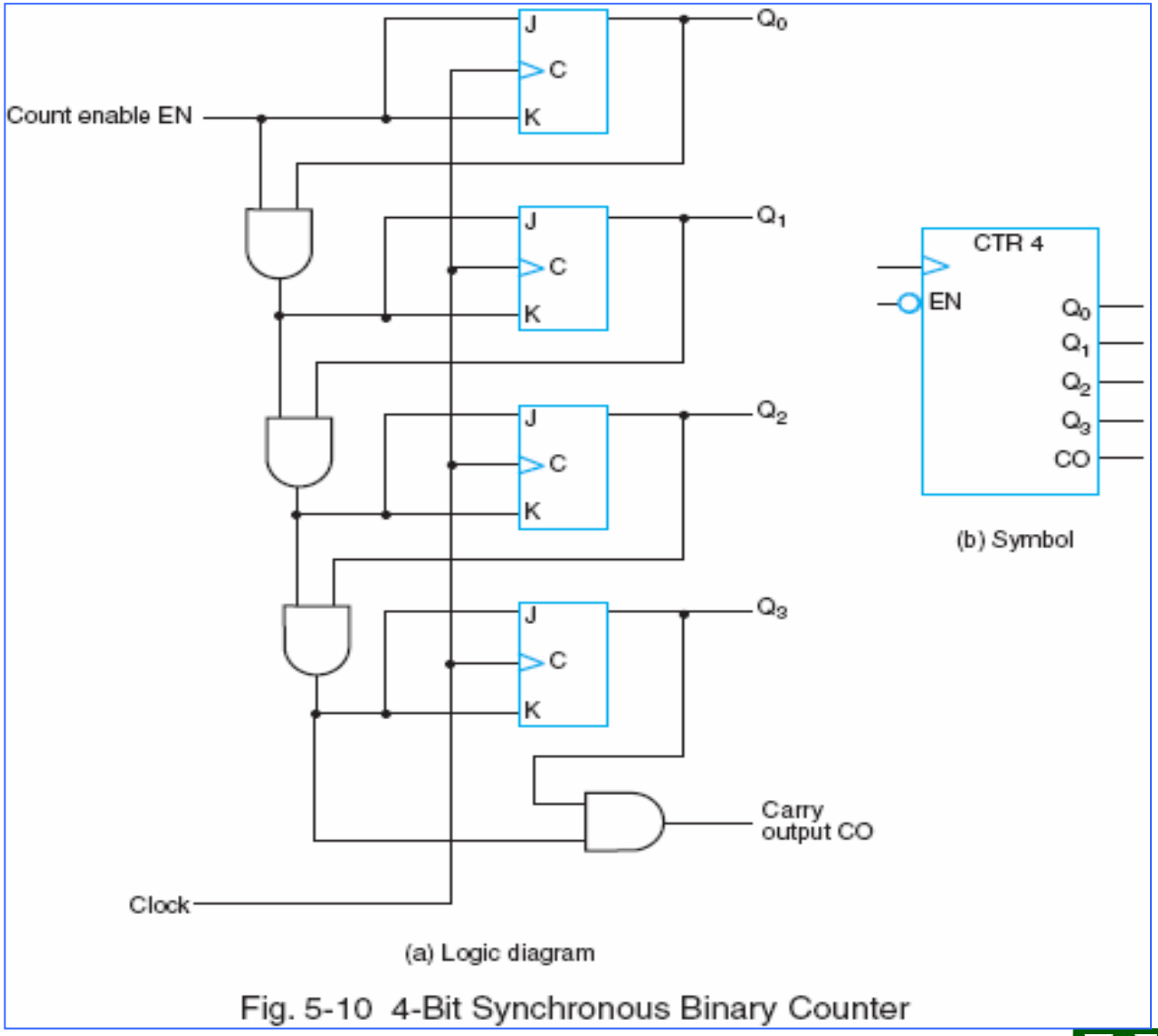


Fig. 5-10 4-Bit Synchronous Binary Counter

Design of binary Counters (Similarly with D FF)

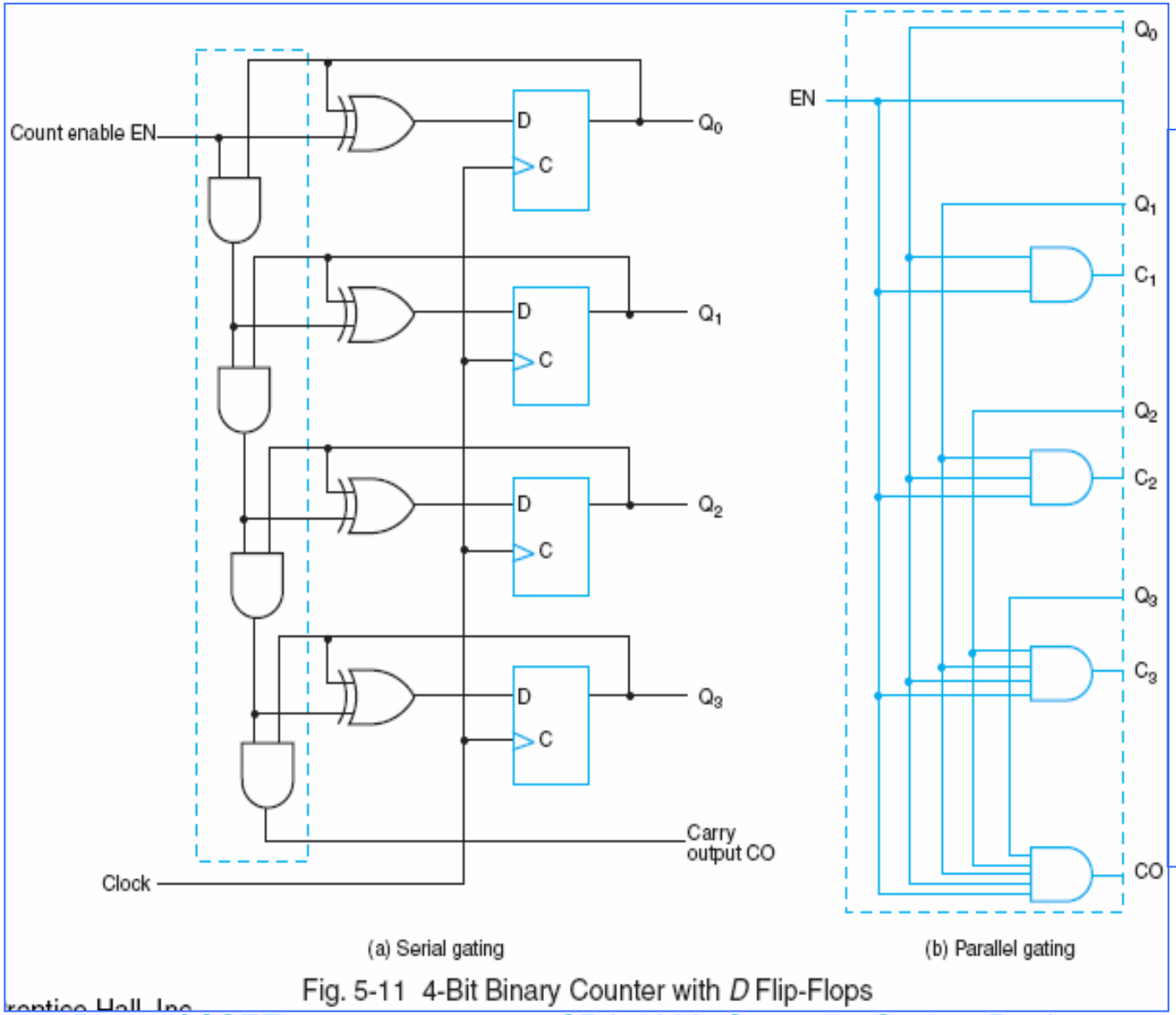


Fig. 5-11 4-Bit Binary Counter with *D* Flip-Flops

Serial gating: A chain of 2-input AND gates used to provide information to a FF from a prior stage. (Analogous to ripple carry adder)

Parallel gating: (Analogous to carry lookahead adder)

Advantage: Delay reduction

Synchronous Binary Counter with Parallel Load

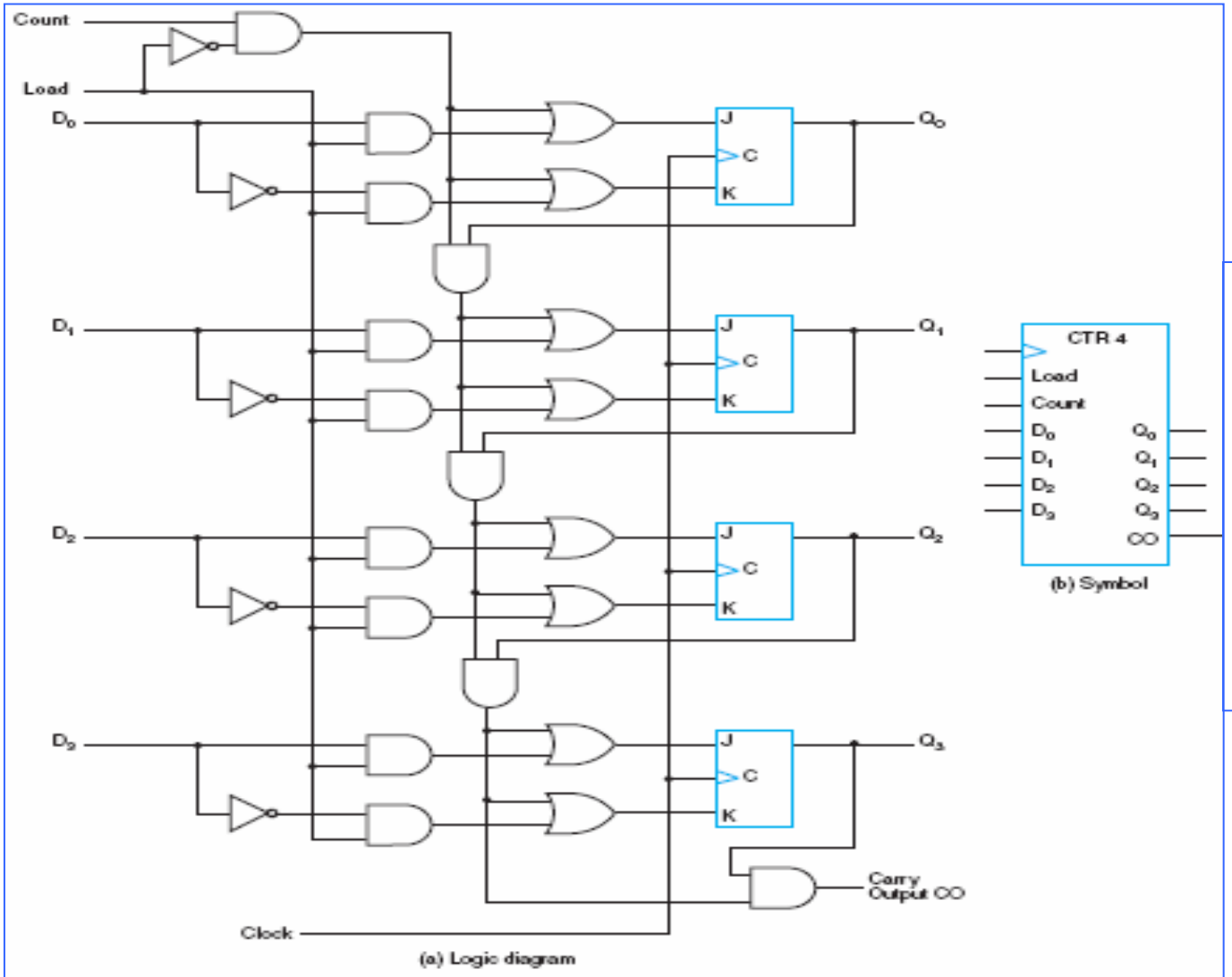


Fig. 5-12 4-Bit Binary Counter with Parallel Load

Load=1, data transfer from input to FFs

Load=0 and Count = 1, works as a binary counter.

Other Counters : BCD Counter

A divide-by-N counter also known as a modulo-N counter is a counter that goes through a repeated sequence of N states. Designed using the same steps as in case of any sequential circuit.

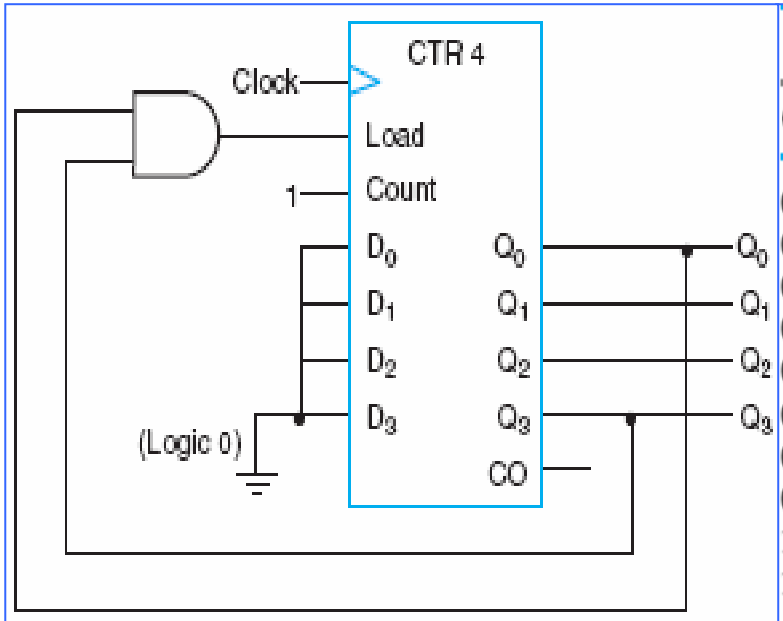
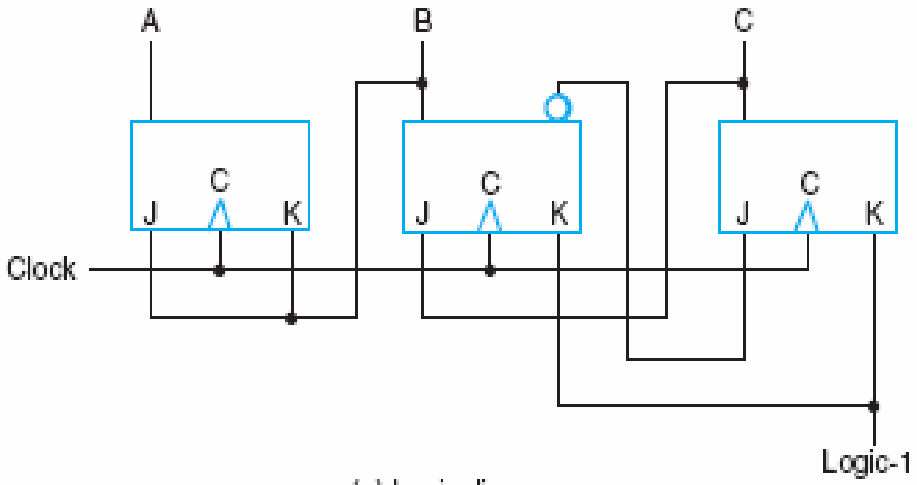


Fig. 5-13 BCD Counter

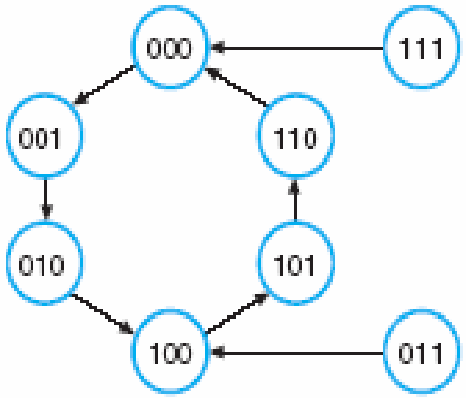
Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	Y	T_{Q8}	T_{Q4}	T_{Q2}	T_{Q1}
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

Table 5-6 State Table and Flip-Flop Inputs for BCD Counter

Other Counters : Arbitrary Count Sequence



(a) Logic diagram



(b) State diagram

Fig. 5-14 Counter with Arbitrary Count

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Table 5-8 State Table and Flip-Flop Inputs for Counter

The simplified FF input equations are:

$J_A = B, K_A = B$

$J_B = C, K_B = 1$

$J_C = B', K_C = 1$