Integrated Circuits (ICs)

Saraju P Mohanty

NOTE

The materials in this lecture are borrowed from the following sources:

- Logic and Computer Design Fundamentals (2nd edition) by M. M. Mano and C. R. Kime.
- Digital Integrated Circuits by J. M. Rabaey.
- Application-Specific Integrated Circuits by M. J. S. Smith.
- Lecture notes of Dr. John Y. Cheung, School of Electrical and Computer Engineering, University of Oklahoma.

Lecture Outline

- Integrated Circuits Categories
- Levels of Integration
- Digital Logic Families
- Characteristics of digital logic families
- Nomenclature of ICs
- Delay of real gates
- Implementation Approaches for Digital ICs
- Digital IC Design Flow
- ASICs in Sun Microsystems SPARCstations1
- Hierarchical Design

What is an Integrated Circuit ?

- An integrated circuits is a silicon semiconductor crystal containing the electronic components for digital gates.
- Integrated Circuit is abbreviated as IC.
- The digital gates are interconnected to implement a Boolean function in a IC .
- The crystal is mounted in a ceramic/plastic material and external connections called “pins” are made available.
- ICs are informally called chips.

Integrated Circuits Categories

There are many different types of ICs as listed below.

IC Categories	**Functions**
Analog ICs	Amplifiers
	Filters
Digital ICs	Boolean Gates
	Encoders/Decoders
	Multiplexers / Demultiplexers
	Flip-flops
	Counters
	Shift Registers
Hybrid ICs	Mixed Signal Processors
Interface ICs	Analog-Digital Converters
	Digital-Analog Converters

Levels of Integration (Chip Complexity)

Categorized by the number of gates contained in the chip.

IC Complexity	Number of Gates	Functional Complexity	Examples
SSI	<10	Basic gates	Inverters, AND gates, OR gates, NAND gates, NOR gates
MSI	10-100	Basic gates	Exclusive OR/NOR
		Sub-modules	Adders, subtractors, encoders, decoders, multiplexers, demultiplexers, counters, flip-flops
LSI	100-1000s	Functional modules	Shift registers, stacks
VLSI	1000s-100,000	Major building blocks	Microprocessors, memories
ULSI	>100,000	Complete systems	Single chip computers, digital signal processors
WSI	>10,000,000	Distributed systems	Microprocessor systems

Levels of Integration (Chip Complexity) …..

- ICs with less than 10 equivalent gates are grouped together and identified as Small Scale Integration (SSI). Chips in this group are mostly simple gates used as glue logic for tying larger components together.
- ICs with 10 to100 equivalent gates are grouped together and identified as Medium Scale Integration (MSI). Chips in this group are mostly simple modules performing a specific elementary function.
- ICs with 100 to few thousand equivalent gates are grouped together and identified as Large Scale Integration (LSI). Chips in this group are also functional modules.
- ICs with several thousand to millions gates are termed Very Large Scale Integration (VLSI), and Ultra Large Scale Integration (ULSI). Chips of these types include microprocessors, microcontrollers, etc.
- Wafer Scale Integration (WSI) refers to devices with many VLSI components connected within a single wafer. This is ideal for constructing devices with many parallel processors

Digital Logic Families

- Various circuit technology used to implement an IC at lower level of abstraction.
- The circuit technology is referred to as a digital logic family.

RTL	Resistor-transistor Logic
DTL	Diode-transistor logic
TTL	Transistor-transistor logic
ECL	Emitter-coupled logic
MOS	Metal-oxide semiconductor
CMOS	Complementary Metal-oxide semiconductor
BiCMOS	Bipolar Complementary Metal-oxide semiconductor
GaAs	Gallium-Arsenide

Digital Logic Families ……

- RTL, DTL, and obsolete.
- TTL are not much used now-a-days.
- ECL can provide high-speed ICs.
- MOS is suitable for high-component density.
- CMOS is preferred for low-power high-performance and high-packing density IC implementation.
- CMOS is widely used technology at present.
- BiCMOS is used where high current and high-speed is necessary.
- GaAs is used for very high speed circuits.

Characteristics of Logic Families

The characteristics of a logic family is expressed in terms of the parameters, such as Fan-in, Fan-out, Noise-Margin, Power Dissipation, and Propagation delay.

- Fan-in: the number of inputs available on a gate.
- Fan-out: the number of standard loads that the output of a typical gate can drive without impairing its performance.
- Noise-Margin: the maximum external noise voltage superimposed on a normal input voltage value that will not cause an undesirable change in the circuit output.
- Power Dissipation: Power consumed / dissipated by a gate.
- Propagation delay: the time for change in value of a signal to propagate from input to output.

IC Nomenclature

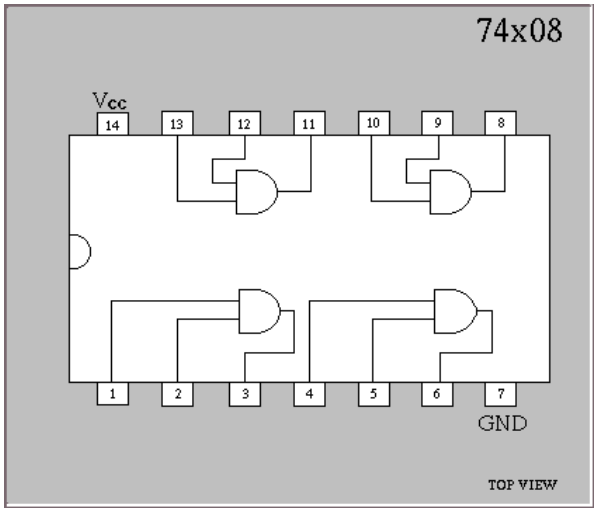
Most chips are identified in a similar way regardless of vendors. Adoption of this notation allows user to select chips with similar functions from a variety of vendors.

- Manufacturer Code:
  (i) SN - Texas Instruments, (ii) DM - National Semiconductor,
  (iii) MC – Motorola, (iv) MM - Monolithic Memories
- Product Line:
  (i) 5 - Military grade TTL products (40C to 100C)
  (ii) 7 - Commercial grade TTL products (0C to 70C), ….., and so on.
- Performance:
  (i) (blank) - Regular, (ii) H - High-speed, (iii) L - Low-power,
  (iii) S –Schottky, (iv) LS - Low-power Schottky, (v) AS - Advanced Schottky, (vi) ALS - Advanced low-power Schottky
- Logic Family:
  (i) 00 - Quad 2-input positive NAND, (ii) 02 - Quad 2-input positive NOR
  (iii) 0 - Hex inverters, (iv) 08 - Quad 2-input positive AND
- Package Type:
  (i) J - Ceramic Dual-In-Line (DIP), (ii) N - Plastic DIP,
  (iii) T -Tin can, (iv) W - Ceramic flat package

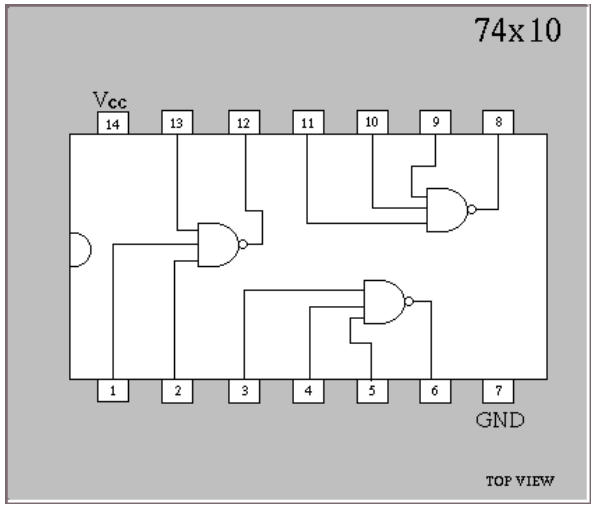
IC Nomenclature : Example ….

	Manufacturer Code	Product Line	Performance Class	Logic Family	Package Type
1	SN	74	LS	00	N
2	MC	54	S	190	T

Chip 1: Texas Instruments, Low-power Schottky, Quad 2-input positive NAND, Plastic DIP, and Chip 2: Motorola, Schottky, Tin can



Qaud 2-input Positive AND Gates



Triple 3-input Positive NAND Gates

Ideal Vs Real Gates

- The ideal gates are perfect switches that provide the output at the same instance when the input is applied.
- In practice, a gate does have a finite nonzero delay.
- The three propagation delay parameters are :
  - high-to-low propagation time (t_{PHL})
  - low-to-high propagation time (t_{PLH})
  - (average) propagation delay (t_{pd})
- Two delay models used during simulation:
  - transport delay
  - inertial delay

Real Gates : Propagation delay

- High-to-low propagation time (t_{PHL}): time delay from the reference voltage at the input to the reference voltage at the output, when output voltage is going from high-to-low.
- Low-to-high propagation time (t_{PLH}): time delay from the reference voltage at the input to the reference voltage at the output, when output voltage is going from low-to-high.
- (Average) propagation delay (t_{pd}): defined as either maximum of t_{PHL} and t_{PLH} or average of the two.
- Usually 50% point on the voltage signal is used as reference, but other references are possible.

Real Gates : Propagation delay ……

NOTE : The 50% point on the voltage signal is used as reference.

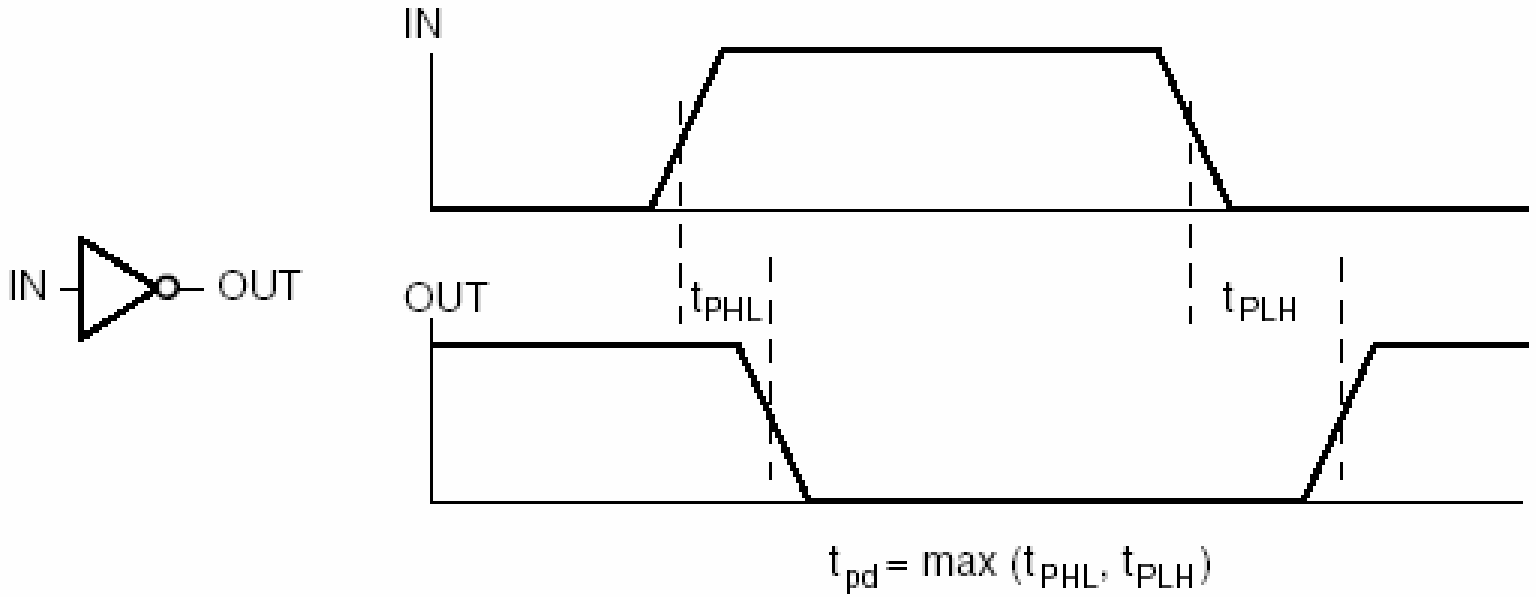


Fig. 2-40 Propagation Delay for an Inverter

Real Gates: Transport Vs Inertial delay

- Inertial delay is intended to model the delay through a gate, in which there is some minimum pulse length that must be maintained before an event is propagated. This minimum pulse length is the rejection time.
- Transport delay, on the other hand, models the delay on a wire, so pulses of any width are propagated.

Real Gates: Transport Vs Inertial delay …….

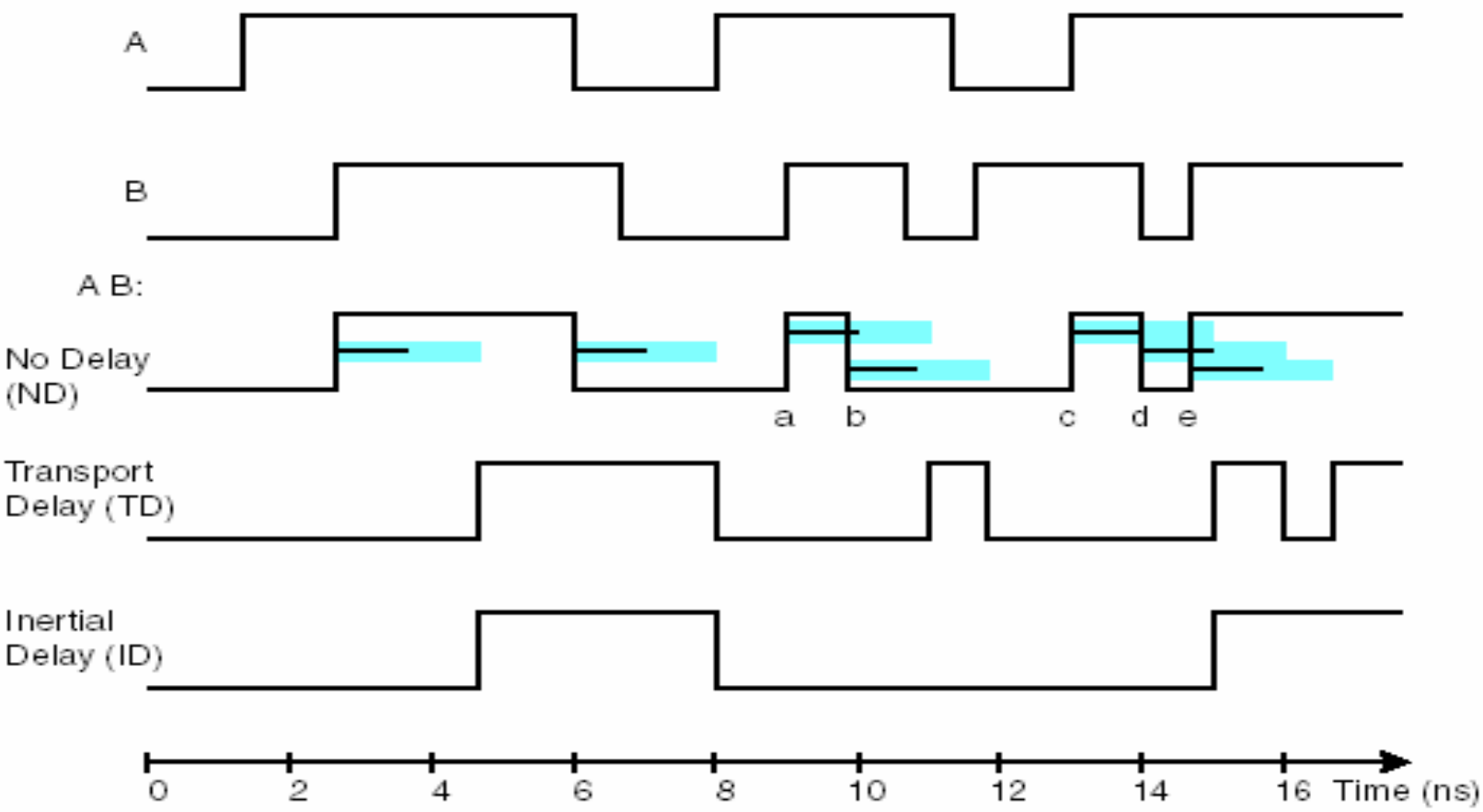


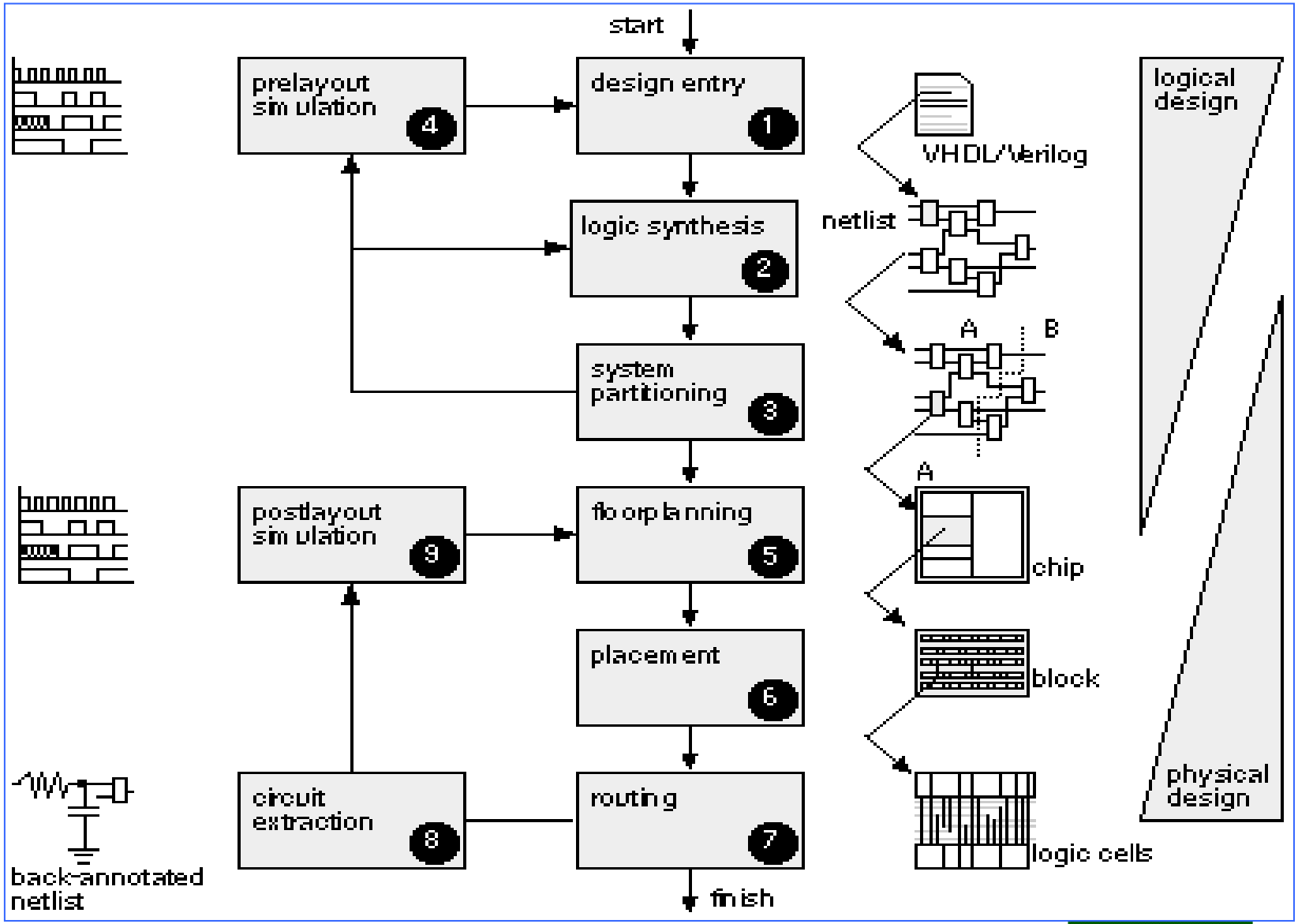
Fig. 2-41 Examples of Behavior of Transport and Inertial Delays

Implementation Approaches for Digital ICs

Implementation Approaches for Digital ICs

- Full-custom: all logic cells are customized. A general purpose microprocessor is designed this way.
- Semi-custom: all of the logic cells are from predesigned cell libraries (reduces the manufacture lead time of the IC)
- Standard-cell based IC uses predesigned logic cells such as AND gates, OR gates, MUXs, FFs,.., etc.
- Macrocells (also called megacells) are larger predesigned cells, such as microcontrollers, even microprocessors, etc.
- Gate-Array, Sea-of-Gates or prediffused arrays contains array of transistors or gates which can be connected by wires to implement the chip.
- Programmable-Logic-Array (PLA) is an example of fuse-based FPGA design. (NOTE: Fuse-based, nonvolatile and volatile are three types of FPGAs)

Digital IC Design Flow



Digital IC Design Flow

- Design entry : Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry .
- Logic synthesis : Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a netlist—a description of the logic cells and their connections.
- System partitioning : Divide a large system into ASIC-sized pieces.
- Prelayout simulation : Check to see if the design functions correctly.
- Floorplanning : Arrange the blocks of the netlist on the chip.
- Placement : Decide the locations of cells in a block.
- Routing : Make the connections between cells and blocks.
- Extraction : Determine the resistance and capacitance of the interconnect.
- Postlayout simulation : Check to see the design still works with the added loads of the interconnect.

A case study follows …….

Case Study: SUN Microsystems SPARCstation1

- SPARCstation 1 is one of the first workstations to make extensive use of ASICs to achieve the following:
  - Better performance at lower cost
  - Compact size, reduced power, and quiet operation
  - Reduced number of parts, easier assembly, and improved reliability
- The SPARCstation 1 contains about 50 ICs on the system motherboard—excluding the DRAM used for the system memory (standard parts).
- The SPARCstation 1 designers partitioned the system into the nine ASlCs and wrote specifications for each ASIC.
- During the design process, the Sun engineers simulated the entire SPARCstation 1—including execution of the Sun operating system (SunOS).

Case Study: SUN Microsystems SPARCstation1 ……

The ASICs in the Sun Microsystems SPARCstation 1		
SPARCstation 1 ASIC		**Gates (k-gates)**
1	SPARC integer unit (IU)	20
2	SPARC floating-point unit (FPU)	50
3	Cache controller	9
4	Memory-management unit (MMU)	5
5	Data buffer	3
6	Direct memory access (DMA) controller	9
7	Video controller/data buffer	4
8	RAM controller	1
9	Clock generator	1

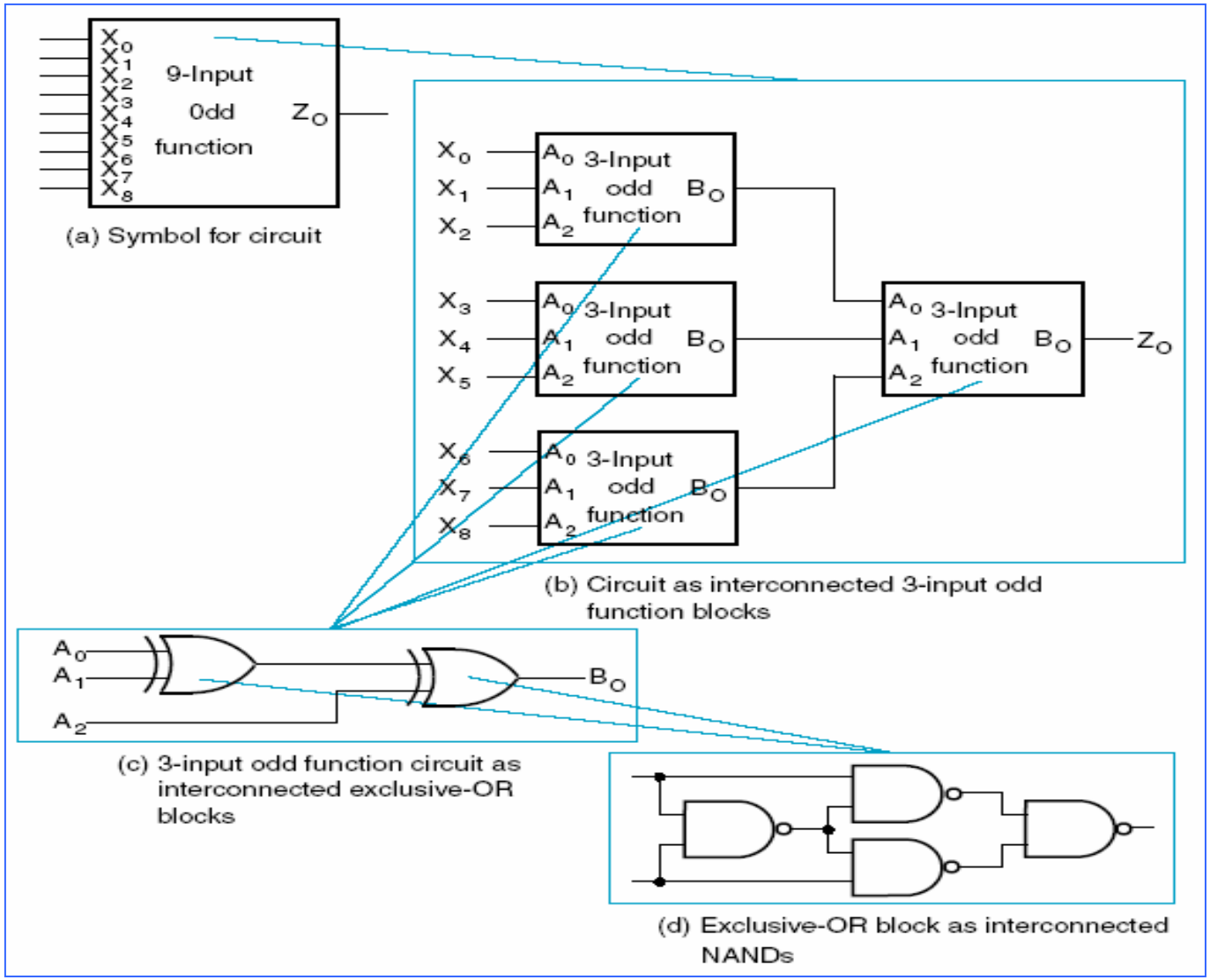
Case Study: SUN Microsystems SPARCstation1 ……

The CAD tools used in the design of the Sun Microsystems SPARCstation 1		
Design level	**Function**	**Tool**
ASIC design	ASIC physical design	LSI Logic
	ASIC logic synthesis	Internal tools and UC Berkeley tools
	ASIC simulation	LSI Logic
Board design	Schematic capture	Valid Logic
	PCB layout	Valid Logic Allegro
	Timing verification	Quad Design Motive and internal tools
Mechanical design	Case and enclosure	Autocad
	Thermal analysis	Pacific Numerix
	Structural analysis	Cosmos
Management	Scheduling	Suntrac
	Documentation	Interleaf and FrameMaker

Hierarchical Design of Digital ICs

- In order to deal with large and complex circuits design-and-conquer approach is used.
- The design is broken into blocks and the blocks are connected to get the overall chip.
- The design-and-conquer approach is referred to as hierarchical design.
- There are several advantages of hierarchical design.
  - Reduction of complexity of the design
  - At the lowest level of hierarchy a program or description can serve as model and schematics not needed.
  - Block reusability

Hierarchical Design of Digital ICs : Example



Hierarchical Design of Digital ICs : Example

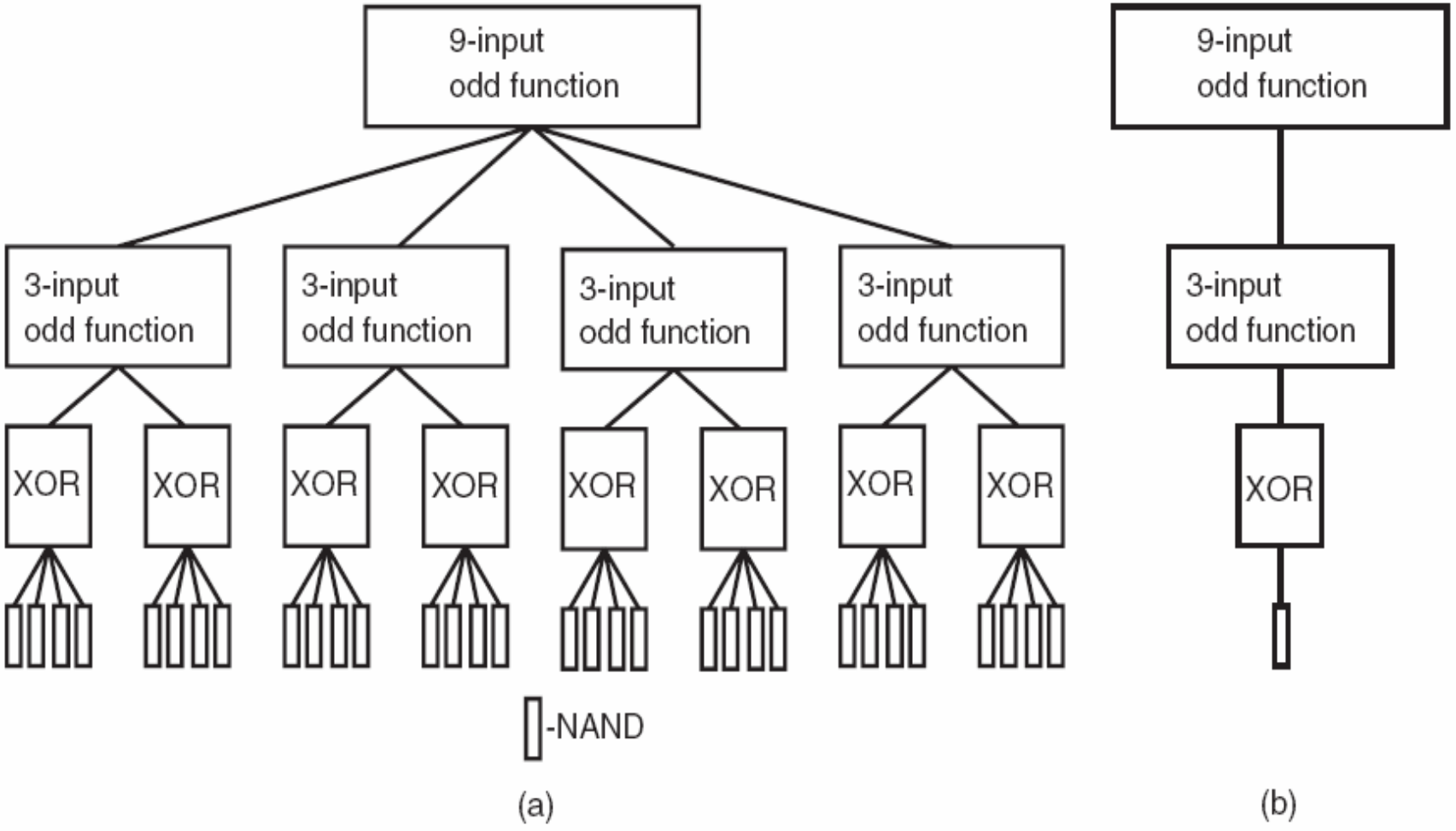


Fig. 3-3 Diagrams Representing the Hierarchy for Figure 3-2

Logic Synthesis

- Logic synthesis transforms an HDL description of a circuit into an optimized netlist representing storage elements and combinational logic.
- Sequences of processes that occur in a tool during logic synthesis are :
  - Analysis: checks the syntax and semantic and produces and intermediate format
  - Elaboration: the design hierarchy is flattened to an interconnection of module
  - Initialization: initializes the variables in simulation model
  - Simulation: execute the simulation model

Logic Synthesis ……

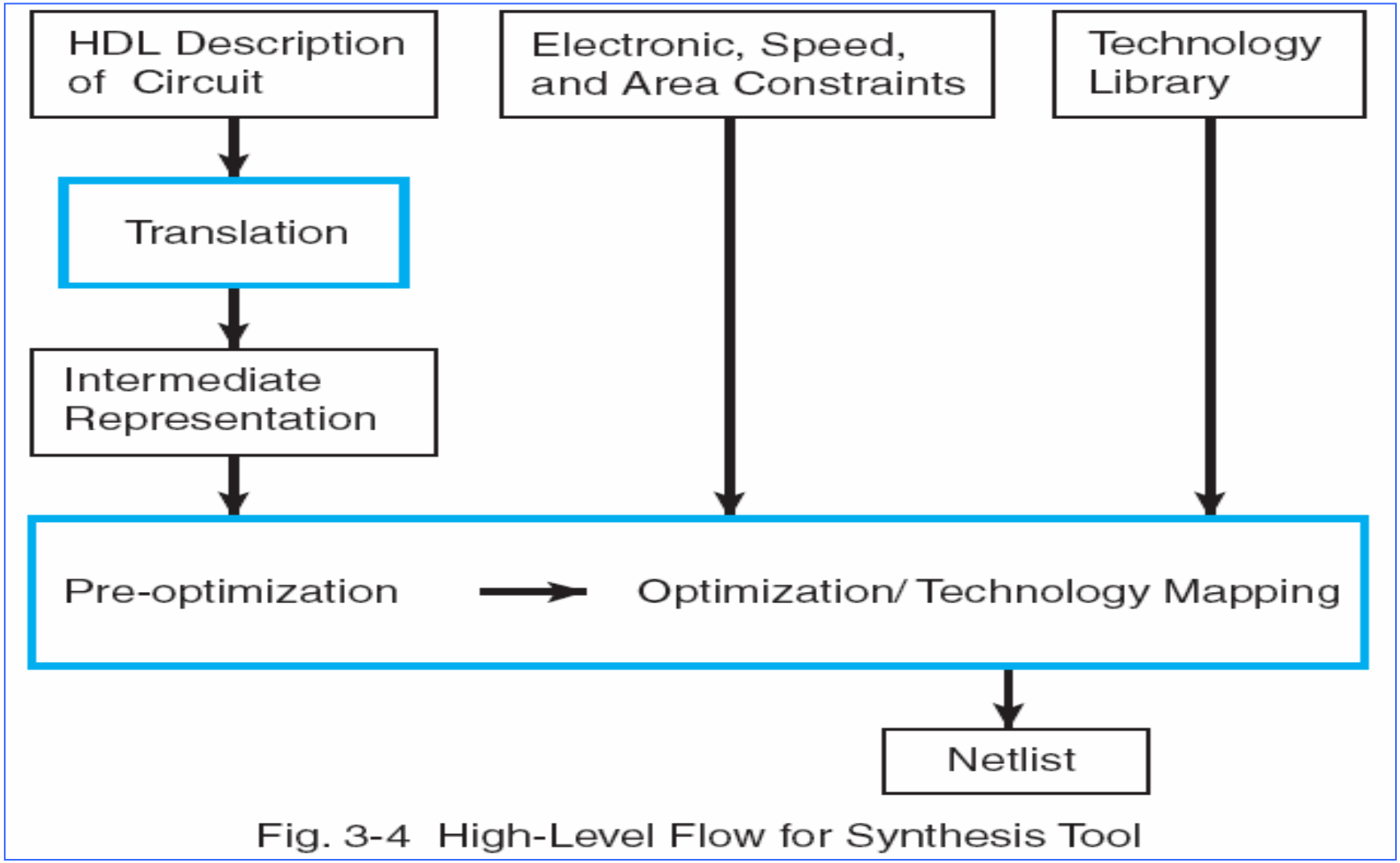


Fig. 3-4 High-Level Flow for Synthesis Tool