Memory and Programmable Logic Devices

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- Basics of Memory and PLDs
- Random Access Memory (RAM)
- RAM Vs ROM
- SRAM Vs DRAM
- Volatile Vs Nonvolatile Memory
- RAM Integrated Circuits
- SRAM Bitslice Model
- SRAM Chip
- Tri-state Buffers

Sources

- Logic and Computer Design Fundamentals by M. M. Mano and C. R. Kime.
- Dr. Valavanis lectures

Memory and PLD Basics

- Memory is a collection of binary storage cells together with associated circuits needed to transfer information into and out of the cells.
- Additional electronic circuits are used for storing and retrieving information.

Memory and PLD Basics: Types of Memory

- There are two types of memory that are used commonly in a computer:
  - Random-Access Memory (RAM)
  - Read-Only Memory (ROM)
- Write operation – the process of storing new information in memory.
- Read operation – the process of transferring the stored information out of memory.
- RAM – performs both Read and Write operations.
- ROM – performs only the Read operation (the information stored in it cannot be altered in any way).

Memory and PLD Basics: Types of PLD

- PLD – An integrated circuit with internal logic gates and/or connections that can in some way be changed by a programming process.
- Programming – A hardware procedure that specifies the bits that are inserted into the hardware configuration of the device.
- ROM is a programmable logic device, PLD.
- Other PLDs – Programmable Logic Array (PLA), Programmable Array Logic (PAL) device, Complex Programmable Logic Device (CPLD), and Field-Programmable Gate Array (FPGA).
- Simplest PLD technology – uses fuses, programming is done by blowing the fuses along the paths that must be removed to obtain the configuration of the function.

Memory and PLD Basics: Types of PLD …

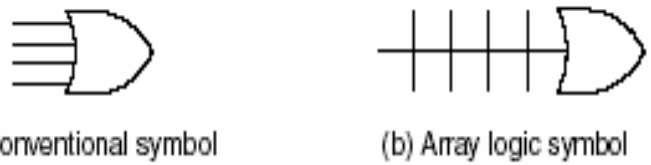


Fig. 6-1 Conventional and Array Logic Symbols for OR Gate

- Typical PLD may have hundreds of millions of gates.
- Need to use a special gate symbol to represent technologies with high fan-ins in a concise form.
- Array Logic – Instead of having multiple input lines to the gate, we draw a single line to the gate. The input lines are drawn perpendicular to this line and are selectively connected to the gate.
- Fuse map – Graphics representation marked with selected connections.

Random Access Memory

- Memory is a collection of binary storage cells together with associated circuits needed to transfer information into and out of the cells.
- Memory cells can be accessed to transfer information to or from any desired location.
- RAM – Time to access memory cells remains the same regardless of location, hence the name.
- On the other hand, Serial Memory – Time to access memory varies with location.
  - –Example: Magnetic disk or tape.
  - –Time to access the desired location depends on where the location is relative to the current physical position of the disk or tape.
- Word – An entity of bits that moves in and out of memory as a unit.
  - – A group of 1's and 0's that represents a number, an instruction, one or more alphanumeric characters, or other binary – coded information.
- Byte – A group of 8 bits.
- Most memories use words that are multiples of 8 bits in length.

Random Access Memory

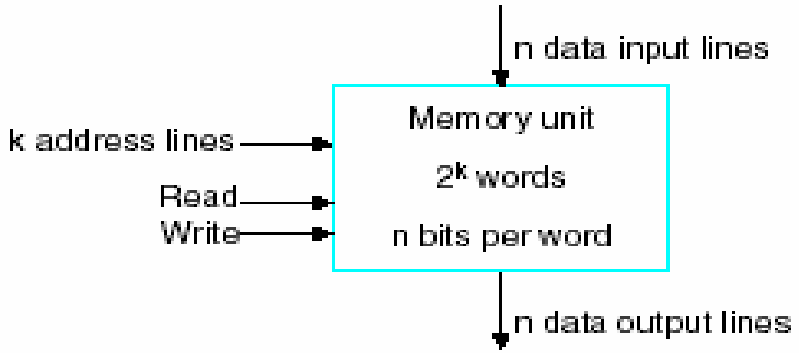


Fig. 6-2 Block Diagram of Memory

- n data input lines provide the information to be stored in the memory.
- n data output lines supply information coming out of memory.
- k address lines specify the particular word chosen among the many available.
- Write input causes binary data to be transferred into memory.
- Read input causes binary data to be transferred out of memory.

RAM: Memory Words and Addresses

- The memory unit is specified by the number of words it contains and the number of bits in each word.
- Address – The identification number assigned to each word in memory. Address lines select one particular word.
- K address lines give addresses in the range from 0 to $2^k - 1$.
- A specific word is selected by specifying a k-bit address. A decoder accepts this address and opens the paths needed to select the word specified.
- Units for Computer Memory:

  Memory referred in words or bytes using letters K (kilo), M (Mega), or G (Giga). K = 2^{10}, M = 2^{20}, and G = 2^{30}

RAM: Memory addresses and contents

Memory address		
Binary	Decimal	Memory contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	⋮	⋮
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Fig. 6-3 Contents of a 1024 × 16 Memory

- Figure shows the possible contents of the first three and last three words of memory. Memory has capacity = 1K words.
- Each word = 16 bits.
- 1K = 1024 = 2^{10} words = 2^{10} X 16 bits = 2048 bytes = 2K bytes.
- 2^{10} words need 10 bits to address them.
- Address ranges from 0000000000 to 1111111111.

RAM: Write and Read operations

- Write – A transfer into memory of a new word to be stored.
- Read – A transfer of a copy of a stored word out of memory.
- Steps for a Write:
  - Apply the binary address of the desired word to the address lines.
  - Apply the data bits that must be stored in memory to the data input lines.
  - Activate the Write input.

  The bits from the data input lines are stored in the word specified by the address lines.
- Steps for a Read:
  - Apply the binary address of the desired word to the address lines.
  - Activate the Read input.

  The bits from the word that has been selected by the address are taken and applied to the data output lines.

RAM: Memory Chip

Memory is made up of RAM chips plus additional logic circuits. RAM chips provide the two control inputs for read and Write operations. A separate inputs, Chip Select to select the chip to be read from or written to.

Chip select CS	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	Memory operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

Table 6-1 Control Inputs to a Memory Chip

- Read/Write' signal determines the operation (Read or Write) to be performed.
- The Chip Select is used to enable the particular RAM chip or chips containing the word to be accessed.
- Chip Select – Signal to access chips.
- Memory Enable – Signal to access the entire memory.

RAM: Timing Waveforms

- Operation of Memory Unit is controlled by an external device, like the CPU.
- CPU is synchronized by its own clock pulse.
- Access time of memory Read operation – The maximum time from the application of the address to the appearance of the data at the Data Output.
- Write cycle time – The maximum time from the application of address to the completion of all internal memory operations required to store a word.
- CPU must provide the memory control signals in such a way as to synchronize its own internal clocked operations with the read and write operations of memory.
- Access time and Write cycle time must be related within the CPU to a period equal to a fixed number of CPU clock cycle pulse periods.

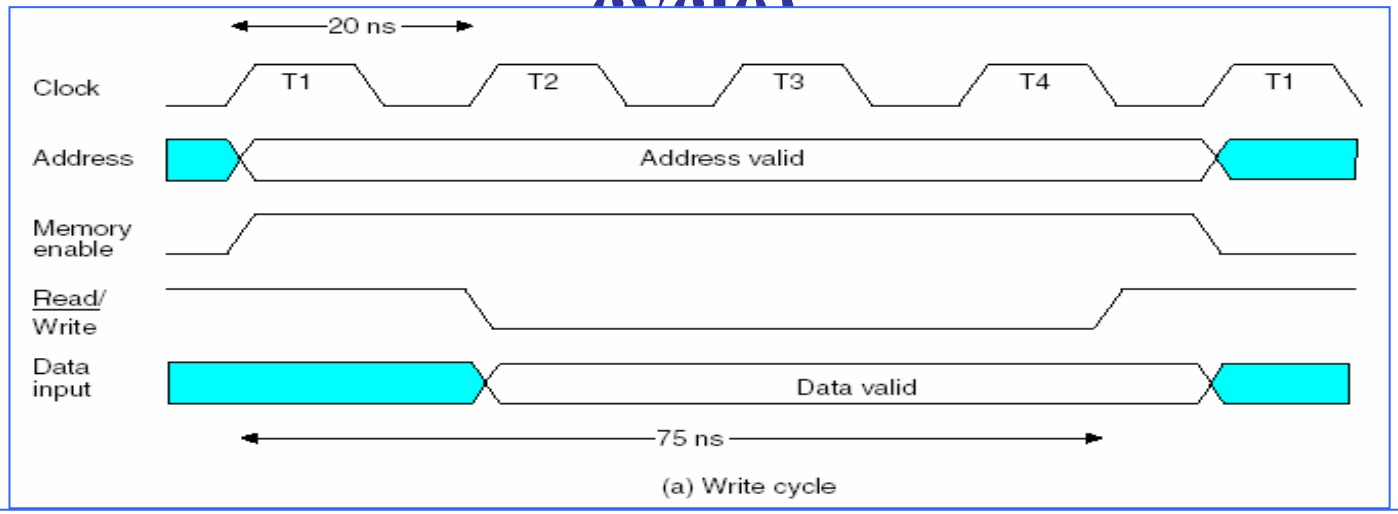
RAM: Timing Waveforms Example

- Consider a CPU operating with a clock frequency of 50MHz → period of 1/50 = 20ns (1ns=10^{-9} s) for one clock pulse. Also consider that CPU communicates with a memory with access time of 65ns and a write cycle time of 75ns.

Then….

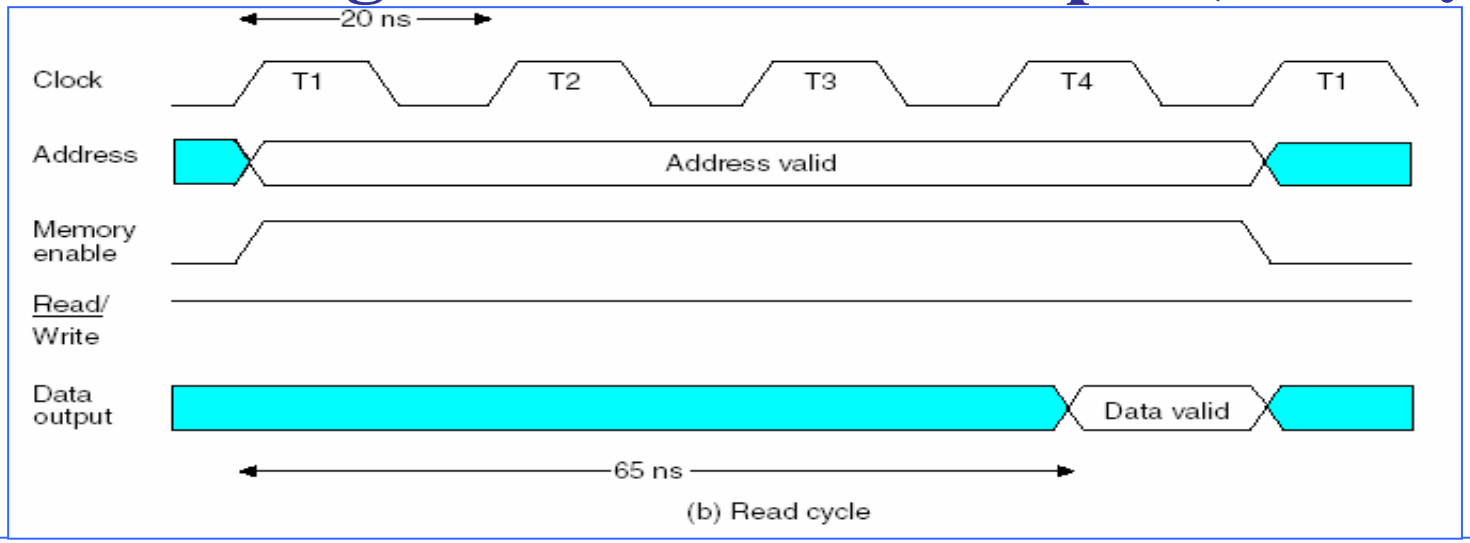
The number of clock pulses required for a memory request = max (access time, write cycle time) = 75ns → at least 4 clock pulses to each memory request.

RAM: Timing Waveforms Example (Write cycle)



- Consider CPU with 50MHz clock and memory with a 75ns write cycle time.
- The address is provided and Memory enable set to high at the positive edge of the T1 pulse.
- The data is applied at the positive edge of T2 pulse.
- Cross-lines in Address and Data waveforms designate a possible change in value of the multiple lines.
- Shaded regions represent unspecified values.
- The Read/Write' signal must stay at 0 long enough after application of the address and Memory Enable to allow the write operation to complete.

RAM: Timing Waveforms Example (Read cycle)

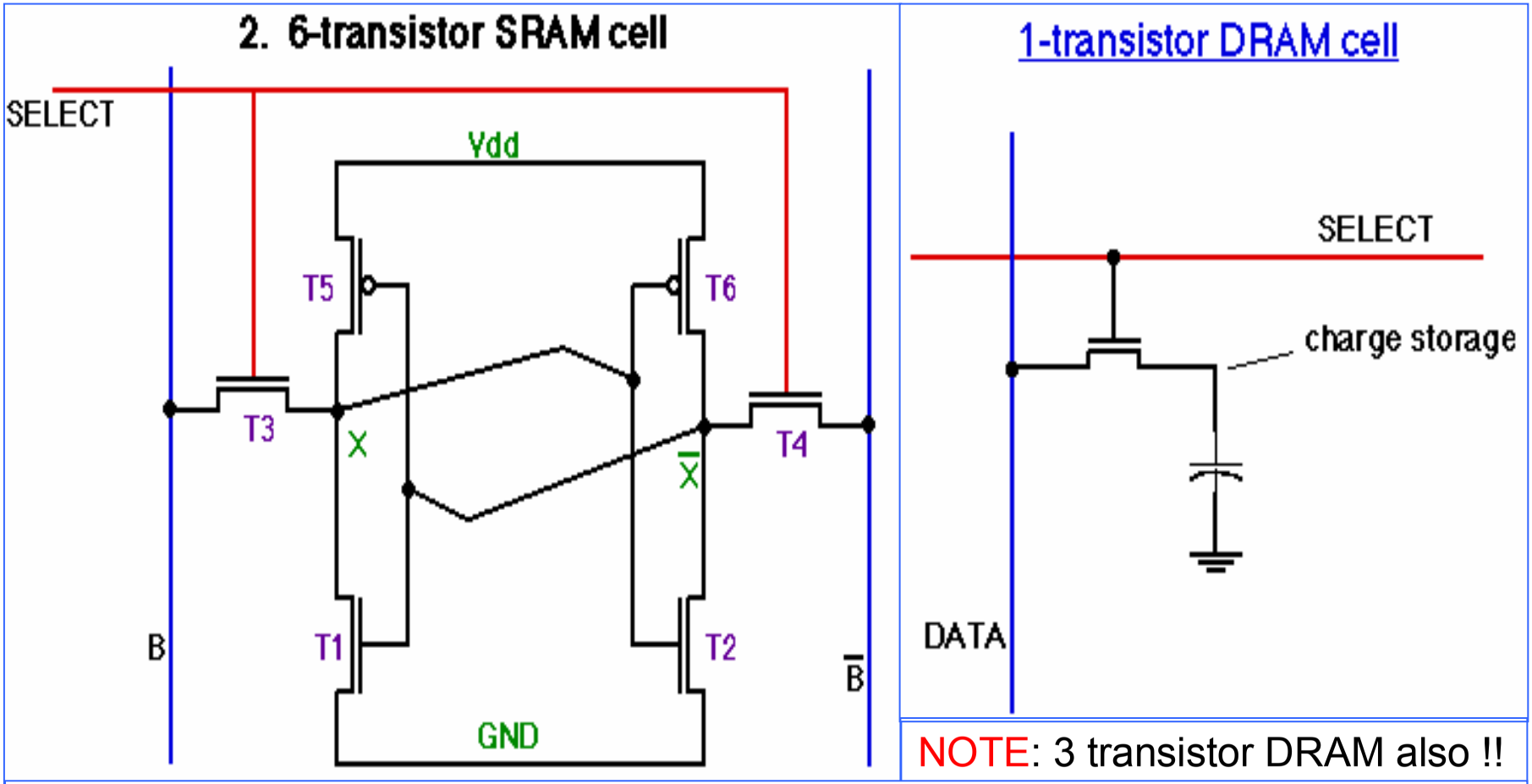


- CPU applies the address, sets the Memory Enable to 1, and sets Read/Write' to 1 to designate a read operation, all at the positive edge of T1.
- The memory places the data of the word selected by the address onto the data output lines within 65ns from the time that the address is applied and the memory enable is activated.
- The CPU transfers the data into one of its internal registers during the positive transition of the next T1 pulse, which can also change the address and controls for the next memory request.

RAM: SRAM Vs DRAM

- Integrated Circuit RAM is of two types : Static and Dynamic.
- Static RAM (SRAM) – consists of internal latches that store the binary information. The stored information remains valid as long as power is applied to the RAM.
- Dynamic RAM (DRAM) – stores the binary information in the form of electric charges on capacitors. The stored charge on the capacitors tends to discharge with time, so, the capacitors must be periodically recharged by refreshing the DRAM.
- Refreshing the DRAM is done by cycling through the words every few milliseconds, reading and rewriting them.
- DRAM offers reduced power consumption and larger storage capacity.
- SRAM is easier to use and has shorter read and write cycles, and doesn't require any refresh.

RAM: SRAM Vs DRAM …



NOTE: 3 transistor DRAM also !!

SRAM: Data is to given at B and B', stores B value.

DRAM: Data is stored in the capacitor.

Source: http://chall.ifj.edu.pl/~szczygie/slides/lectures.html

RAM: SRAM Cell

Storage part is modeled by an SR latch. Inputs enabled by Select signal. Select=1 → stored content determined by B and B'. Select =0 → stored content is held.

Also, Select = 0 → C, C' are 0, Select = 1 → C has stored value and C' its complement.

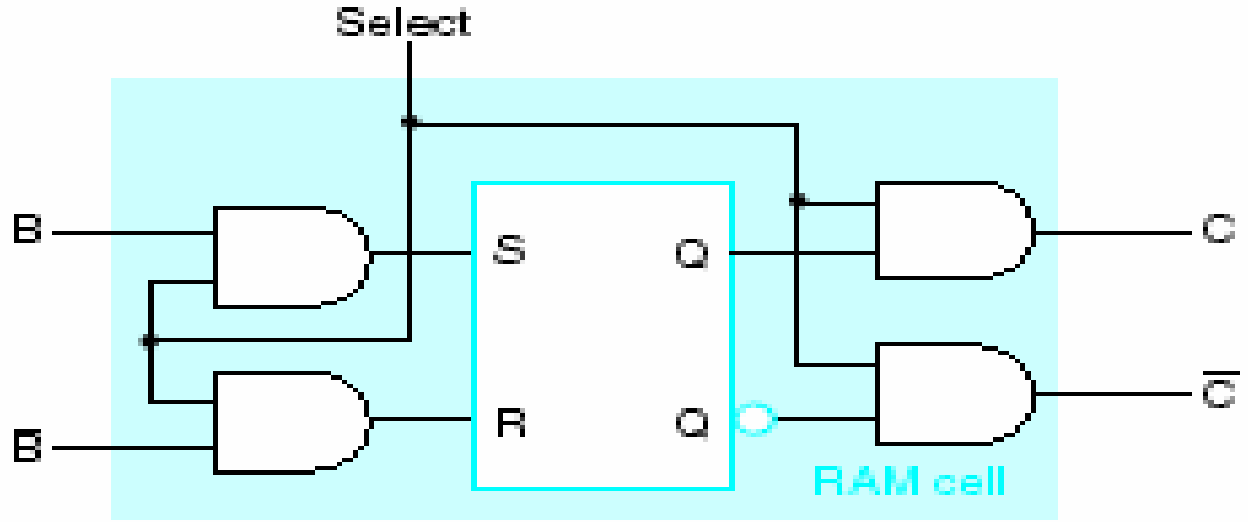
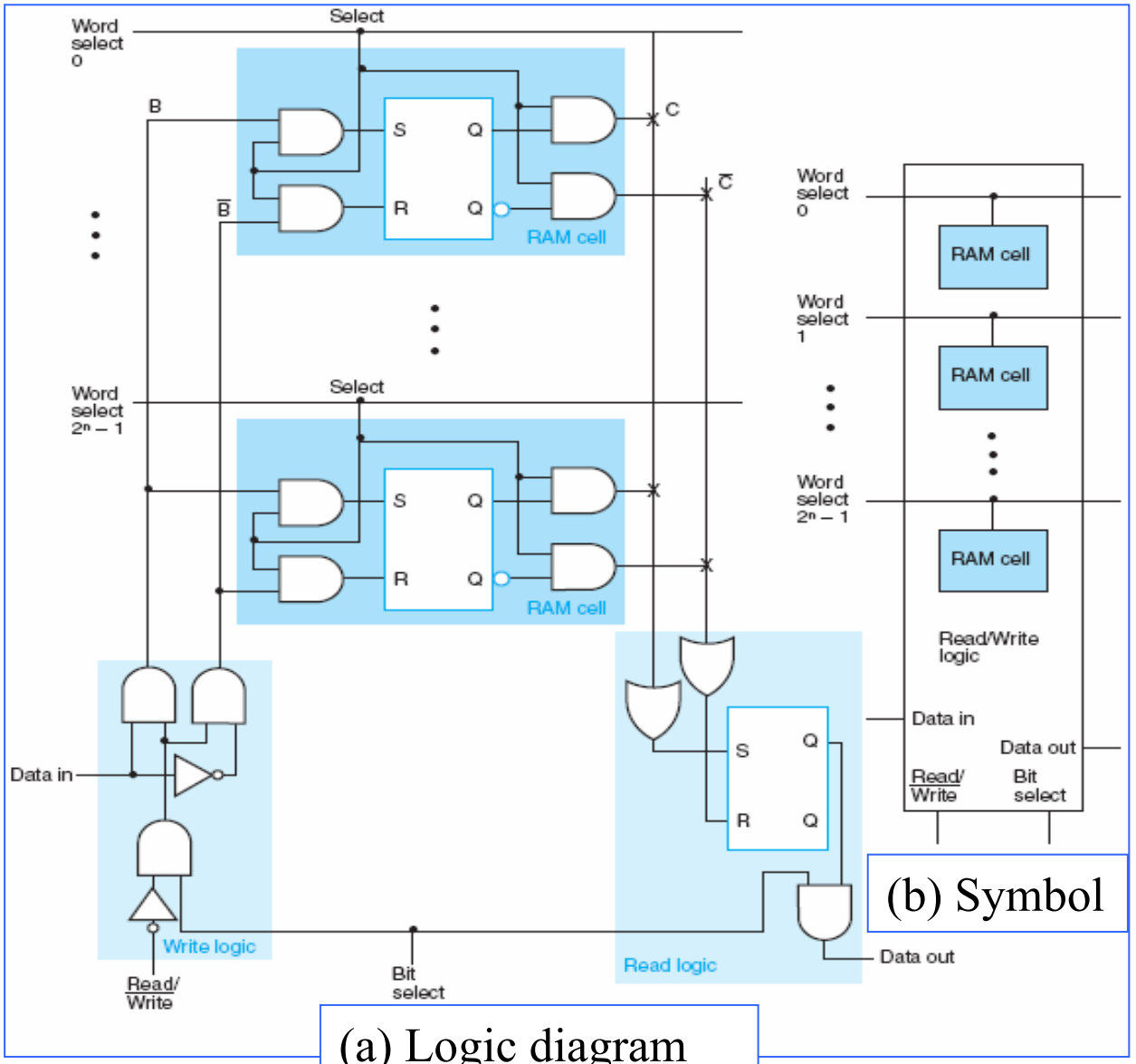


Fig. 6-5 Static RAM Cell

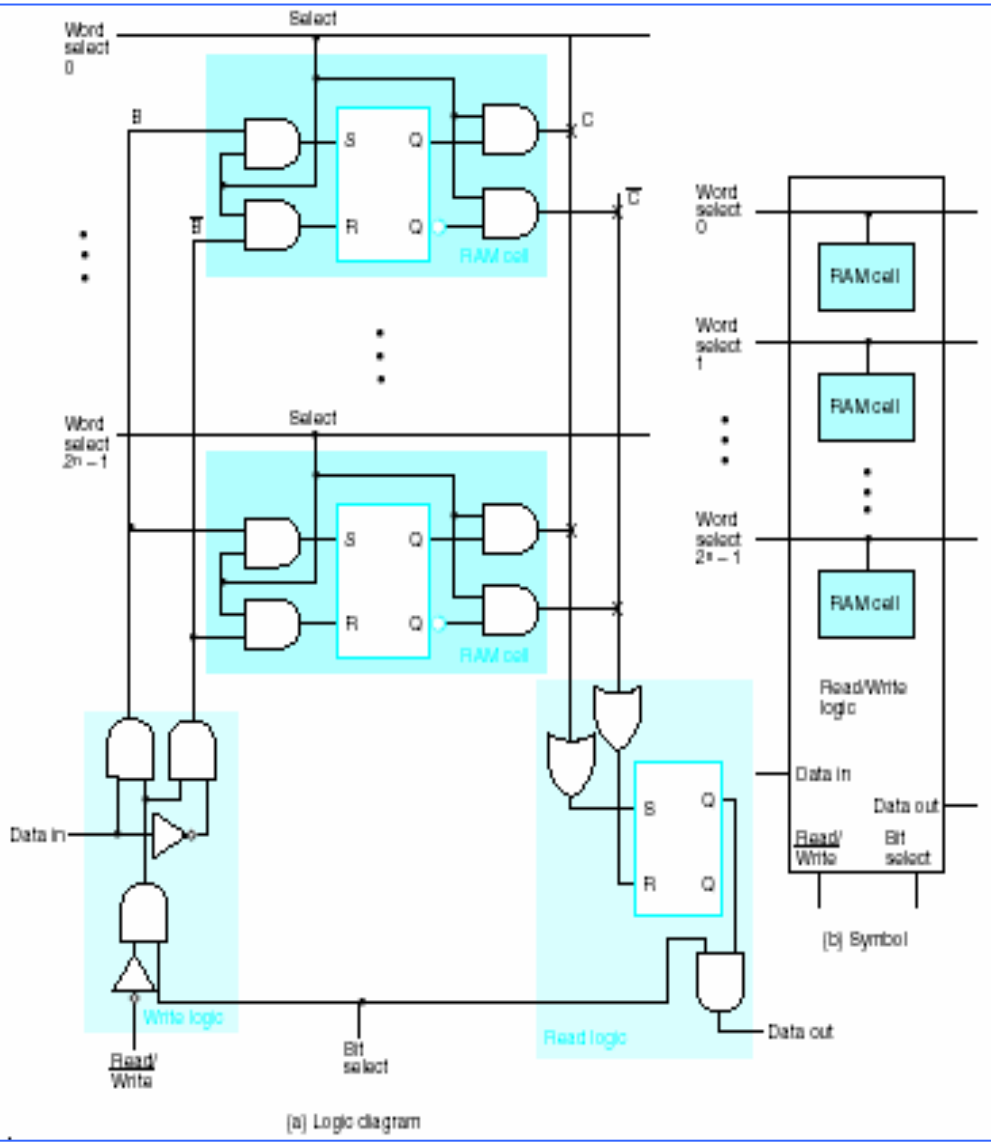
RAM: Volatile and Non-Volatile Memory

- Volatile Memory – Memory unit that loses stored information when power is turned off.
  - Integrated circuit RAMs (static and dynamic) are volatile, since, binary cells need external power to maintain the stored information.
- Non-Volatile Memory – Memory unit that retains the stored information even after the removal of power.
  - Magnetic disks are non-volatile, because, the data stored on the magnetic components is represented by the direction of magnetization, which is retained after power is turned off.
  - ROMs are another example of non-volatile memories.

RAM Integrated Circuits: RAM bit slice model



RAM ICs: RAM bit slice model …



Only one word is written at a time.

Each RAM cell is highlighted in blue. Loading of a cell latch now controlled by a Word Select input. When 0 → S, R are 0 and latch cell contents unchanged. When 1 → value to be loaded controlled by B, B' from the Write Logic

In order for either B, B' to be 1 and potentially change the stored value, Read/(Write)' must be 0 and Bit Select 1. Then, Data In value and its complement are applied to B and B' to set or reset the latch in the RAM cell selected. If Data In is 1 → latch is set to 1, if Data In is 0 → latch is reset to 0, completing the write operation.

RAM ICs: 1-bit RAM bit

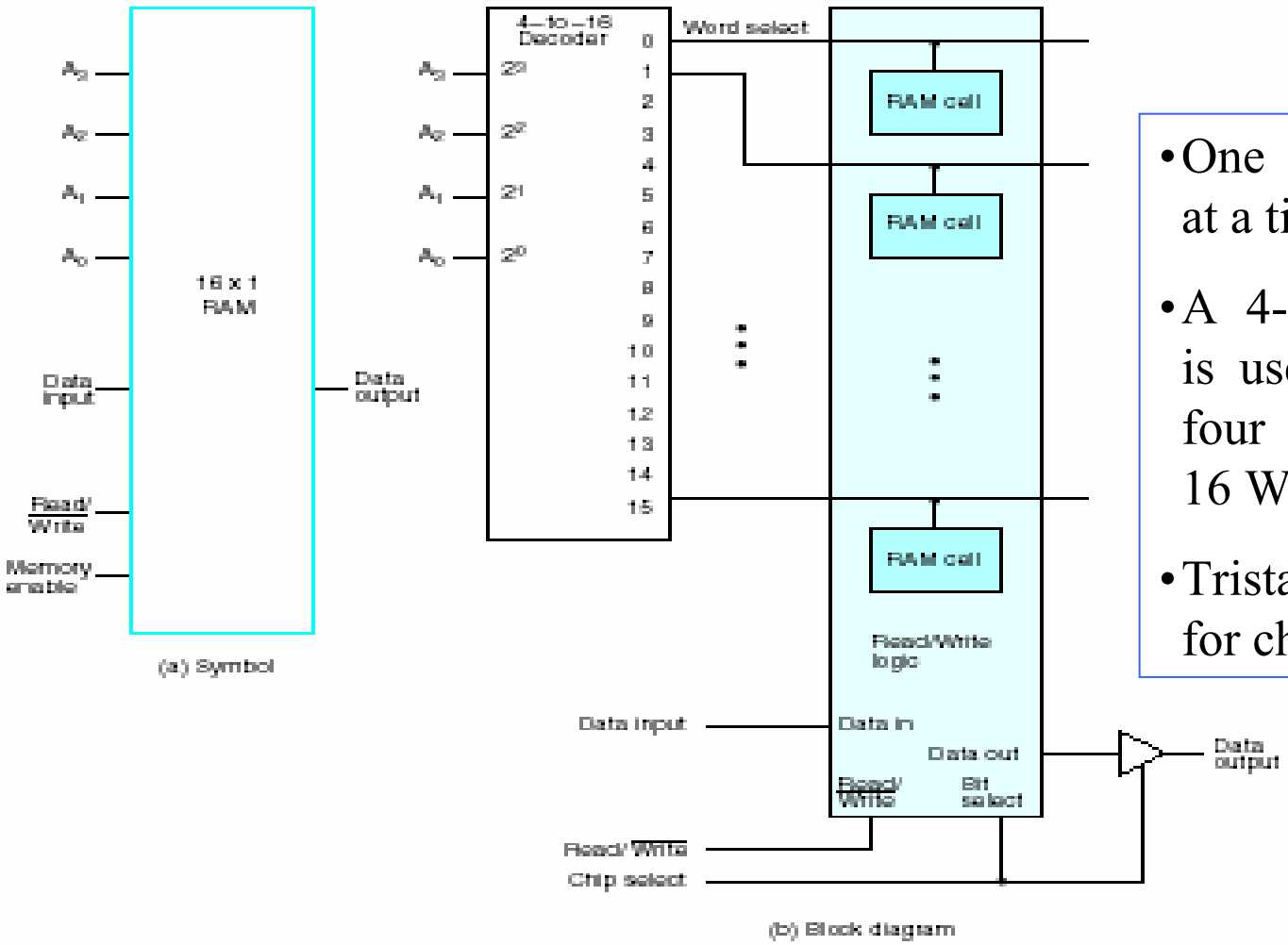
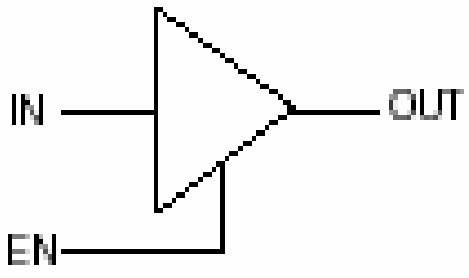


Fig. 6-7 16-Word by 1-Bit RAM Chip

- One word is selected at a time.
- A 4-t-16-line decoder is used to decode the four address bits into 16 Word Select bits.
- Tristate buffer is used for chip selection.

RAM ICs: Three-state buffers



(a) Logic symbol

EN	IN	OUT
0	X	HI-Z
1	0	0
1	1	1

(b) Truth table

Fig. 6-8 Three-state Buffer

This is the hi-impedance state

Hi-Z behaves like an open circuit → appears that the output is disconnected. When connected together, form a multiplexed line. By using three-state buffers on the outputs of RAM chips, these outputs can be connected together to provide the word from the chip being read on the bit lines attached to the RAM outputs. Enable signals correspond to the Chip Select inputs on the RAM chips.

RAM ICs: Coincident Selection

- Inside a RAM chip, the decoder with k inputs and 2^k outputs requires 2^k AND gates with k inputs per gate if a straightforward design is used.
- Total number of decoder gates can be reduced by employing two decoders with a **coincident selection** scheme. In one possible configuration two **k/2-input** decoders are used instead of one **k-input** decoder. One controls the word select lines, the other the bit select lines. → **two dimensional matrix selection scheme**.
- Consider RAM chip with m words with 1 bit per word, then the scheme selects the RAM cell at the intersection of the Word Select row and the Bit Select column. ***Word select name is changed to Row Select.*** An output from the added decoder that selects one or more bit slices is referred to as **Column Select**.

RAM ICs: Coincident Selection ….

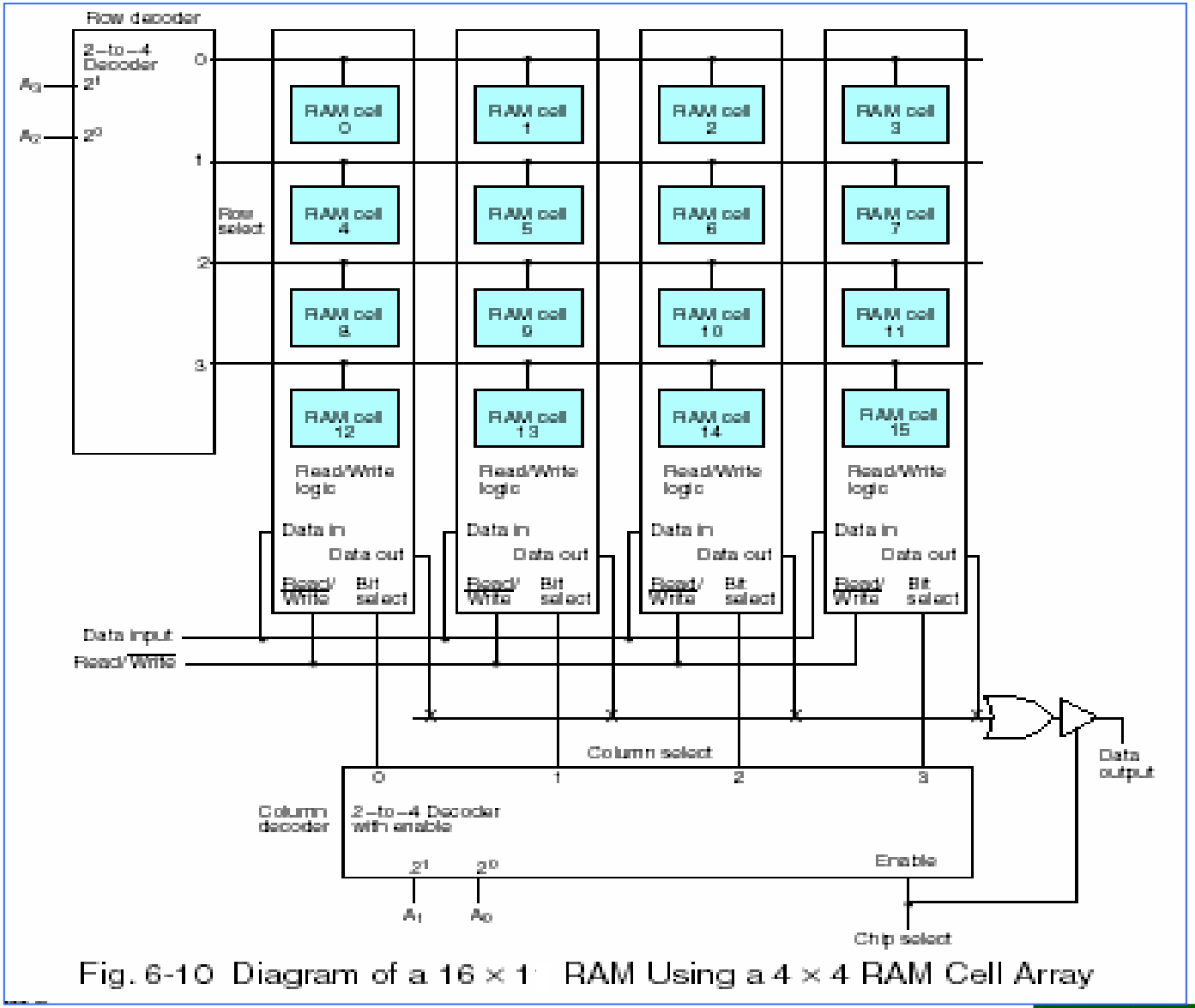


Fig. 6-10 Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array

RAM ICs: Coincident Selection ….

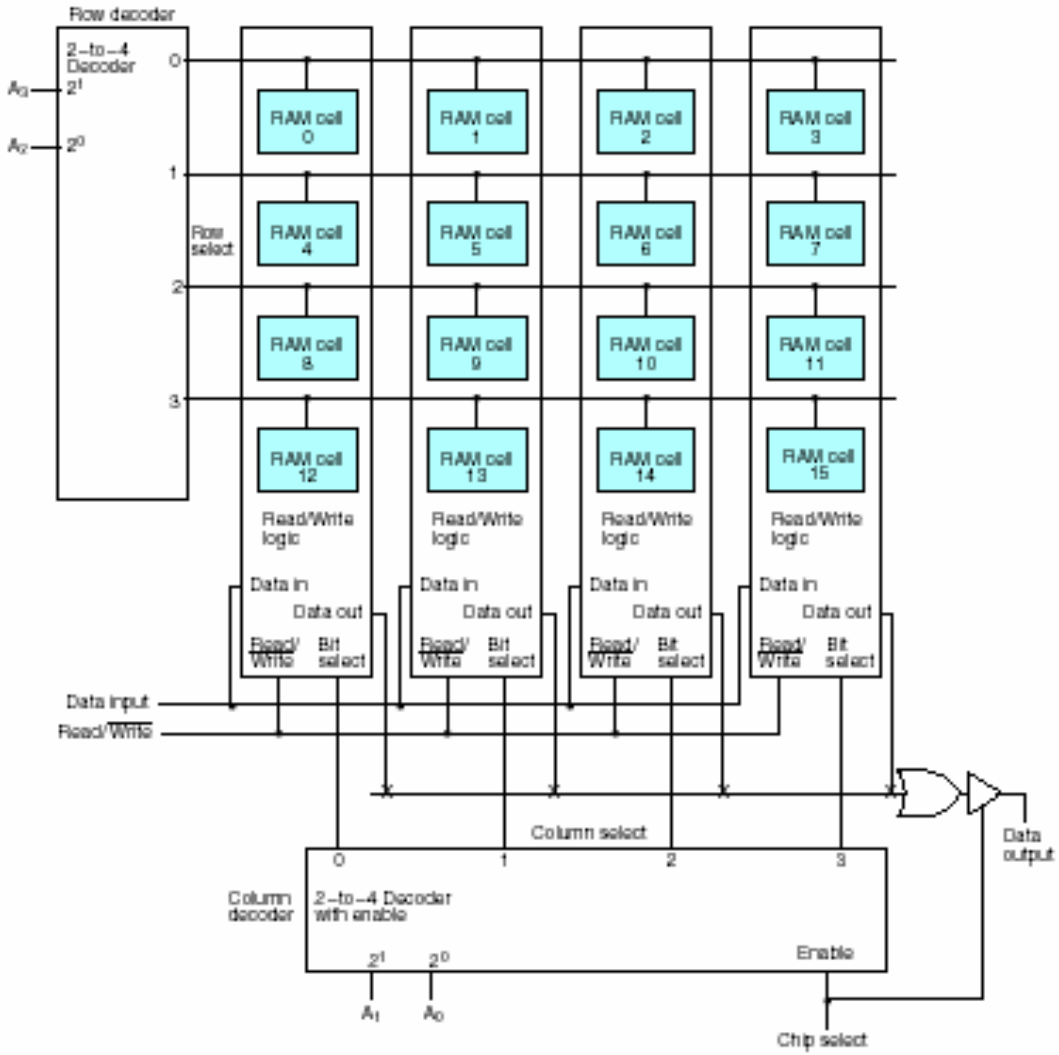


Fig. 6-10 Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array

4 RAM bit slices of 4 bits each, total of 16 RAM cells in a 2-D array.

The two most significant address inputs go through the 2-to-4 line row decoder to select one of the four rows of the array. The two least significant address inputs go through the 2-to-4 line column decoder to select one of four columns of the array.

Column decoder is enabled with the Chip Select input. When 0 all outputs of the decoder are 0, none of the cells is selected → prevents writing into any RAM cell in the array. When 1, a single bit in the RAM is accessed.

RAM ICs: Coincident Selection ….

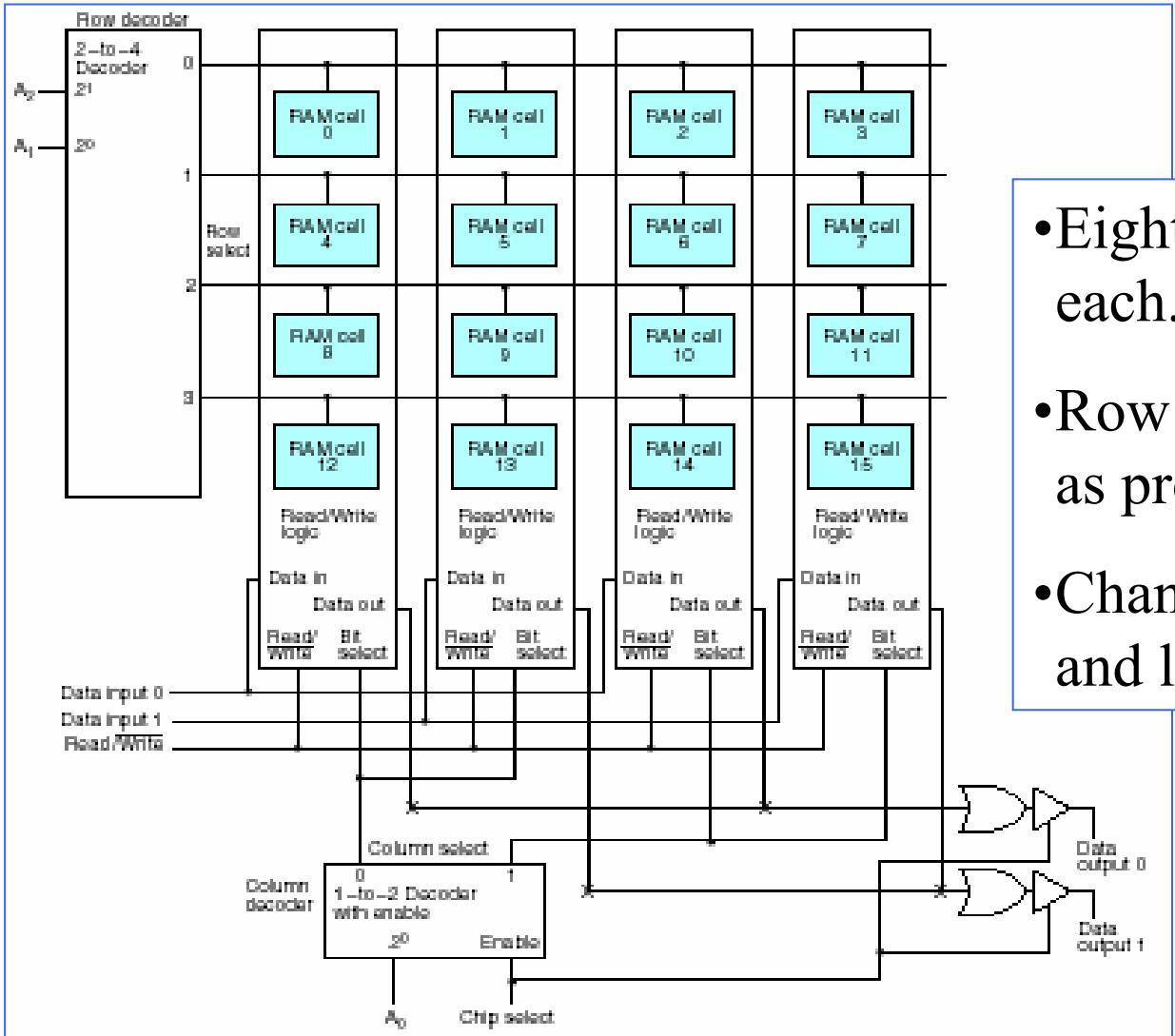


Fig. 6-11 Block Diagram of an 8 × 2 RAM Using a 4 × 4 RAM Cell Array

- Eight word of two bits each.
- Row decoding is same as previous.
- Change in the column and logic output.