# Memory and Programmable Logic Devices

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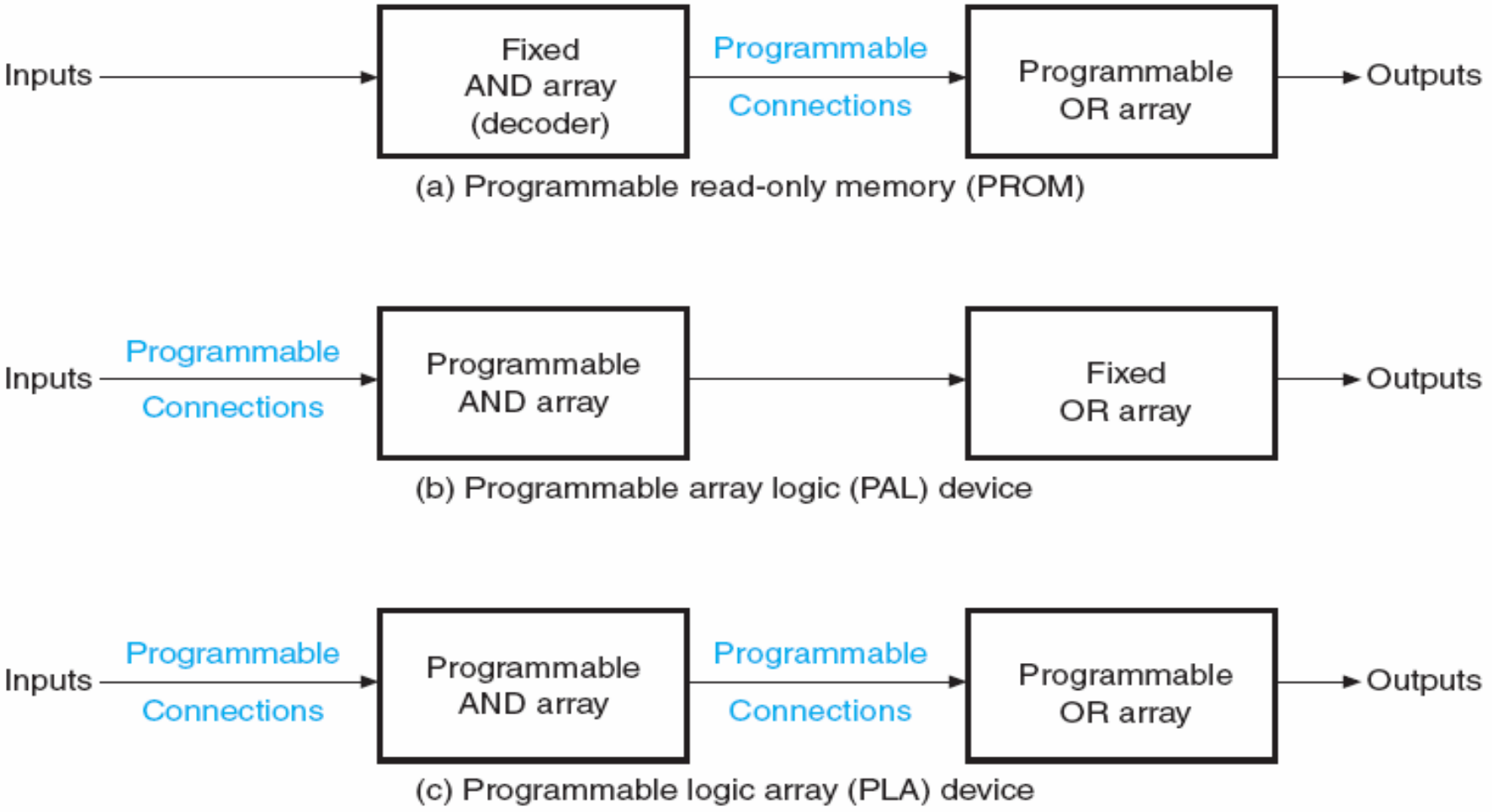
## Part 3

- Three types of PLDs
- Programmable Logic Array
- Programmable Array Logic Devices
- VLSI Programmable Logic Devices

Sources

– Logic and Computer Design Fundamentals by M. M. Mano and C. R. Kime.

# Three Majors Types of PLDs




The three major types of PLDs differ in the placement of programmable connections in the AND-OR array.

# Three Majors Types of PLDs

- Programmable Read-Only Memory (PROM): Has fixed AND array constructed as decoder and programmable connection for the output OR gates. PROM implements Boolean functions in sum-of-minterms form.
- Programmable Array Logic (PAL): Has fixed OR array and programmable connection AND array. The AND gates are programmed to provide the product terms for the Boolean functions, which are logically summed in each OR gate.
- Programmable Logic Array (PLA): Has programmable connections for both AND and OR arrays. The product terms in the AND array may be shared by any OR gate to provide the required sum-of-products implementation.

# Programmable Logic Array (PLA)

- Similar to PROM, but does not provide full deocding of the variables and does not generate all the minterms.
- The decoder is replaced by an array of AND gates that can be programmed to generate product terms of the input variables.
- The product terms are then connected to OR gates to provide the sum-of-products for the Boolean function.

# Programmable Logic Array : Example

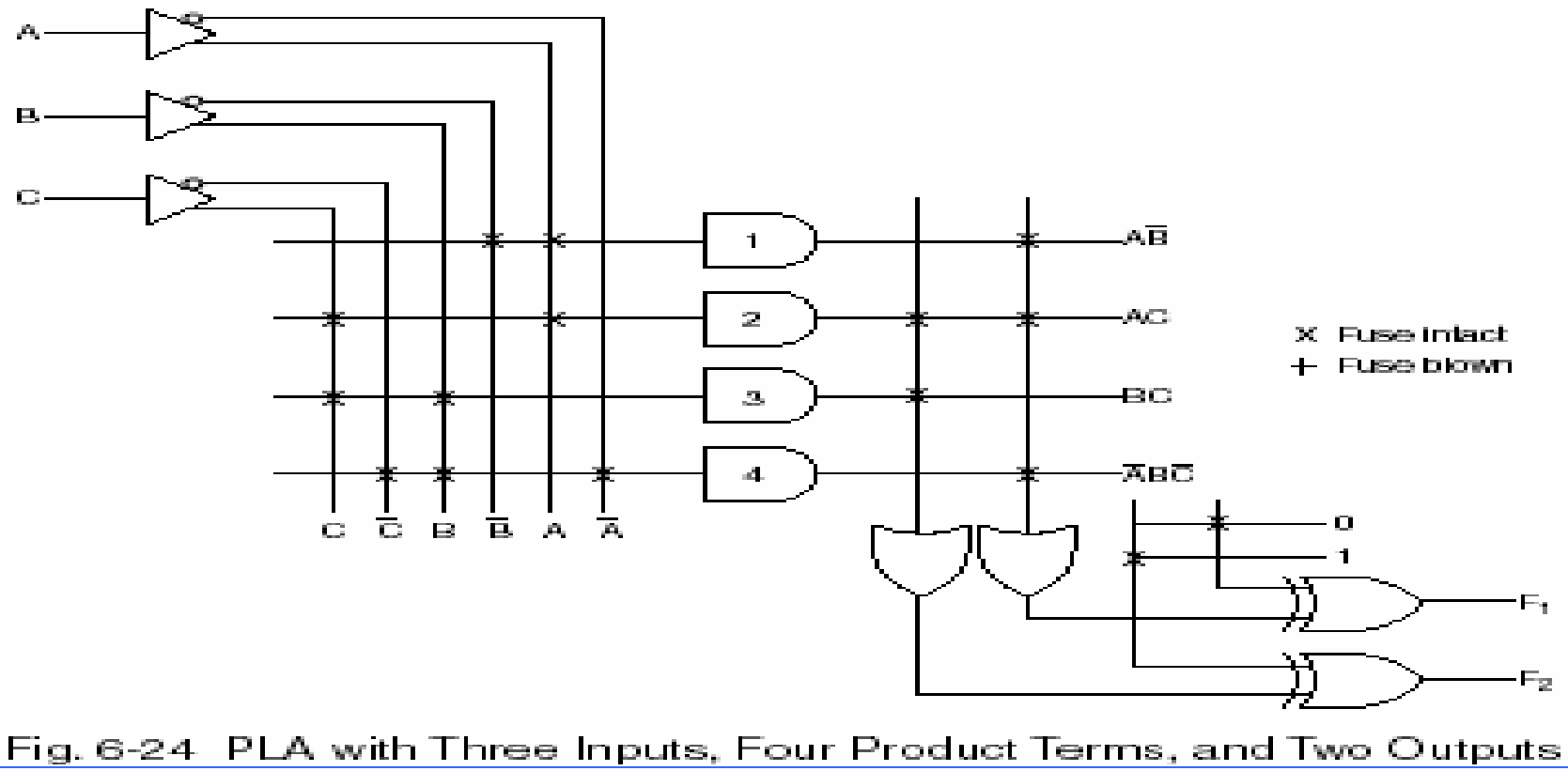



Fig. 6-24 PLA with Three Inputs, Four Product Terms, and Two Outputs

The Boolean functions implemented in the above PLA are: $F_1$=AB'+AC+A'BC' and $F_2$=(AC+BC)'. The output is complemented or left in its true form, depending on the programming of the connection associated with the XOR gate.

# Programmable Logic Array: Example…

- The fuse map of a PLA is specified in a tabular form.
- The table consists of three sections. The 1st section lists the product term numbers. The 2nd section specifies the paths between inputs and AND gates. The 3rd section specifies the paths between the AND and OR gates.
- For each product term the inputs are marked 1, 0, or -, depending on its appearance in the product.

| | | Inputs | | | Outputs | |
|---|---|---|---|---|---|---|
| | Product term | A | B | C | (T) $F_1$ | (C) $F_2$ |
| $A\overline{B}$ | 1 | 1 | 0 | — | 1 | — |
| $AC$ | 2 | 1 | — | 1 | 1 | 1 |
| $BC$ | 3 | — | 1 | 1 | — | 1 |
| $\overline{A}B\overline{C}$ | 4 | 0 | 1 | 0 | 1 | — |

Table 6-4 Programming Table for the PLA in Figure 6-24

For each output variable we may have T (true) or C (complement) for controlling the output XOR gate.

# Programmable Logic Array: Size

- The size of a PLA is specified by the number of inputs, the number of product terms, and the number of outputs.
- For n inputs, k product terms, and m outputs, the internal logic of PLA consists of n buffer-inverters gates, k AND gates, m OR gates, and m XOR gates. There are 2n*k programmable connections, between the inputs, and the AND arrays, k*m programmable connections between the AND OR arrays, and m programmable connections associated with the XOR gates.
- In designing a digital system with PLA, there is no need to show the internal connections of the unit. All that is needed is a PLA programming table from which PLA can be programmed to supply the required logic.

# Programmable Array Logic (PAL) Devices

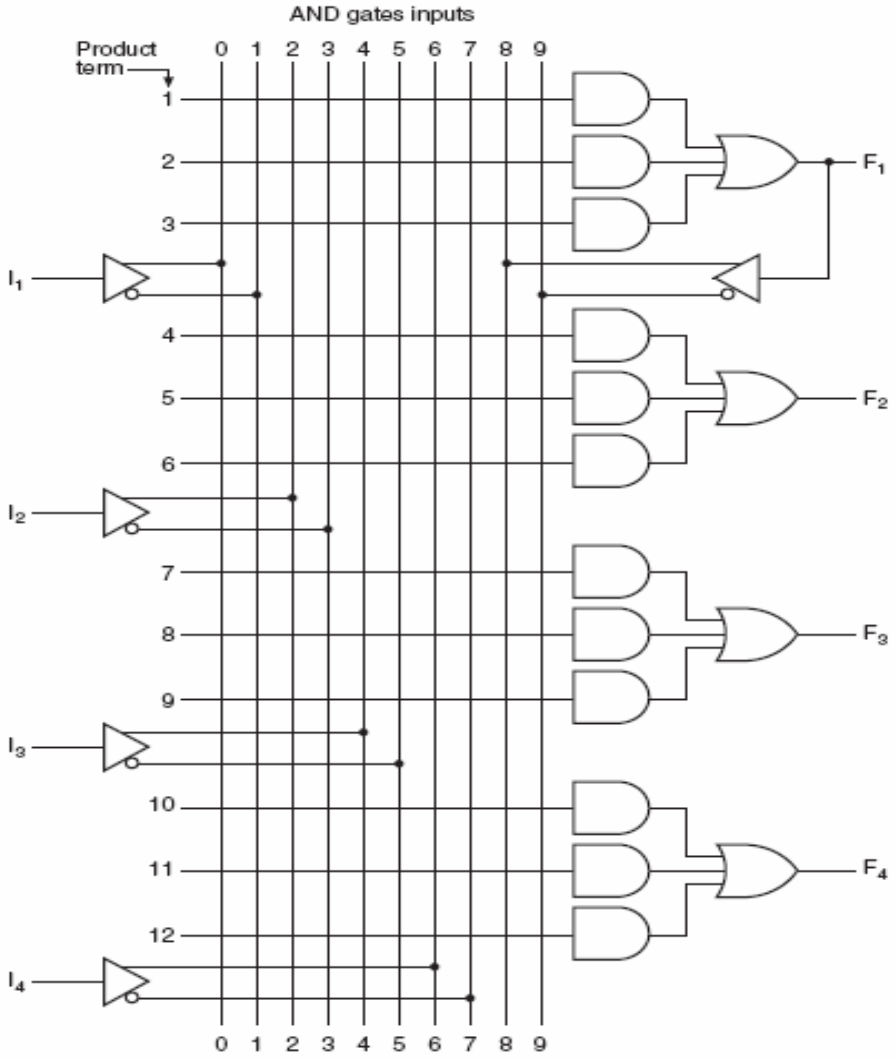



Fig. 6-26 PAL® Device with Four Inputs, Four Outputs, and a Three-wide AND-OR Structure

The PAL devices are easy to program, as only the AND gates are programmable, but it is not as flexible as the PLA.

Each input has a buffer-inverter gate and each output is generated by a fixed OR gate. Device has four sections, each composed of a three-wide AND-OR array, meaning that there are three programmable AND gates in each section. Each AND gate has 10 programmable input connections, indicated in the diagram by the 10 vertical lines.

# VLSI Programmable Logic Device

- The gate arrays have gates in the range 1000-1,000,000, typically called complex programming logic devices (CPLDs) or field-programming gate arrays (FPGAs).
- Properties:
  - Substantial amount of uncommitted combinational logic
  - Pre-implemented flip-flops, and
  - Programmable interconnections between the combinational logic, flip-flops, and the chip input/output.

# VLSI Programmable Logic Device ….

- The VLSI PLDs, differ significantly from vendor to vendor.
- Three vendors:
  - Actel
  - Xilinx
  - Altera
- Reference: Brown, S., and Rose, J., "*FPGA and CPLD Architectures: A Tutorial*", IEEE Design & Test of Computers, pp. 42-57, 1996.

# VLSI Programmable Logic Device: Altera

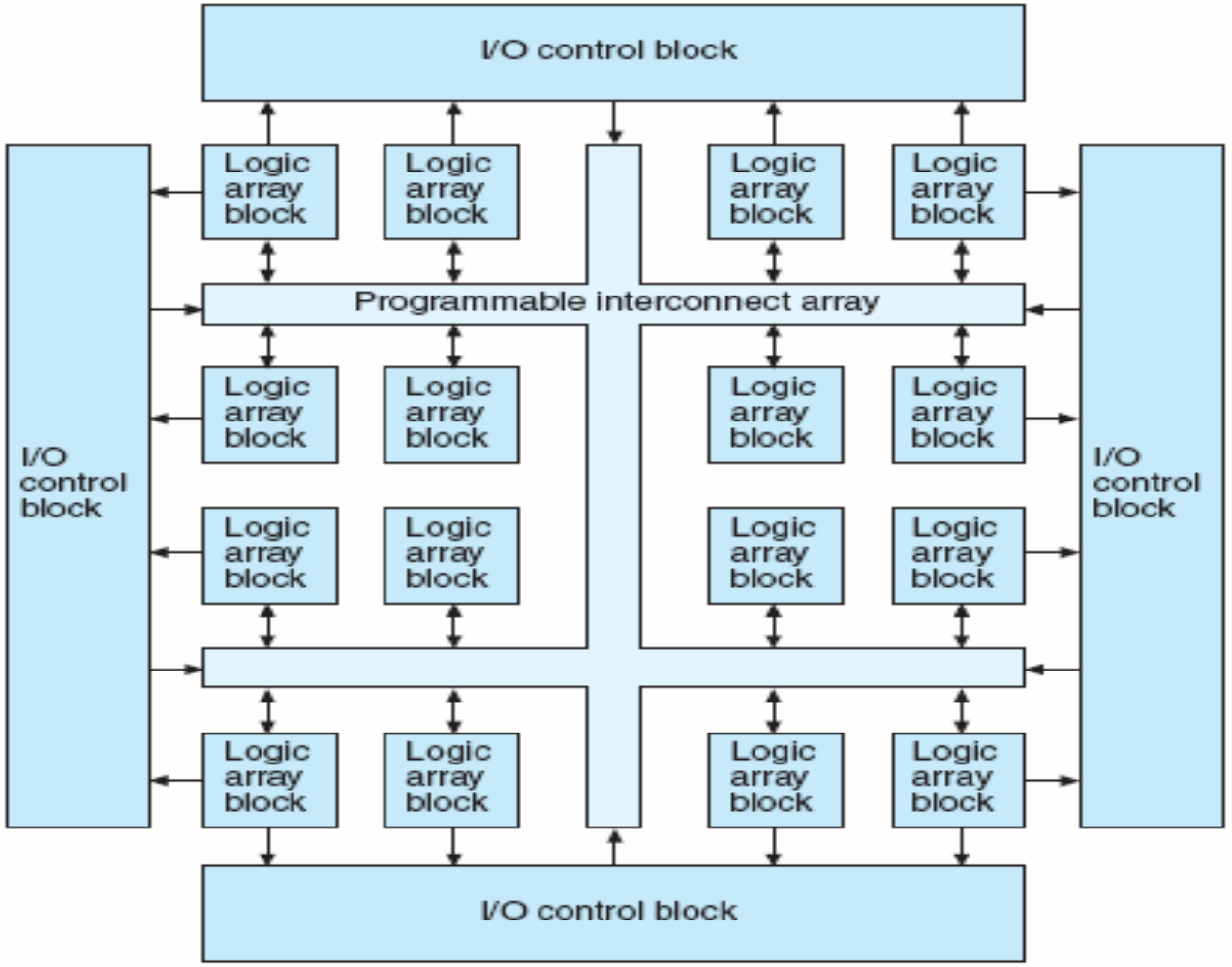



Fig. 6-28 Altera® MAX 7000™ Structure (Reprinted with Permission of Altera Corporation,© Altera Corp., 1991)

# VLSI Programmable Logic Device: Altera

- Based on an EEPROM floating gate technology.
- There are 16 identical logic array blocks, all of whose outputs feed into the programmable interconnect array.
- The programmable interconnect arrays also receive inputs from the I/O control blocks.
- Connections can be programmed from all signals within the programmable interconnection array to the inputs of the logic array block.
- Each logic array block has 16 macrocells, each with a flip-flop and basic combinational circuits.
- Each macrocell in the logic array blocks around the outer edge is connected to I/O control blocks.

# VLSI Programmable Logic Device: Xilinx

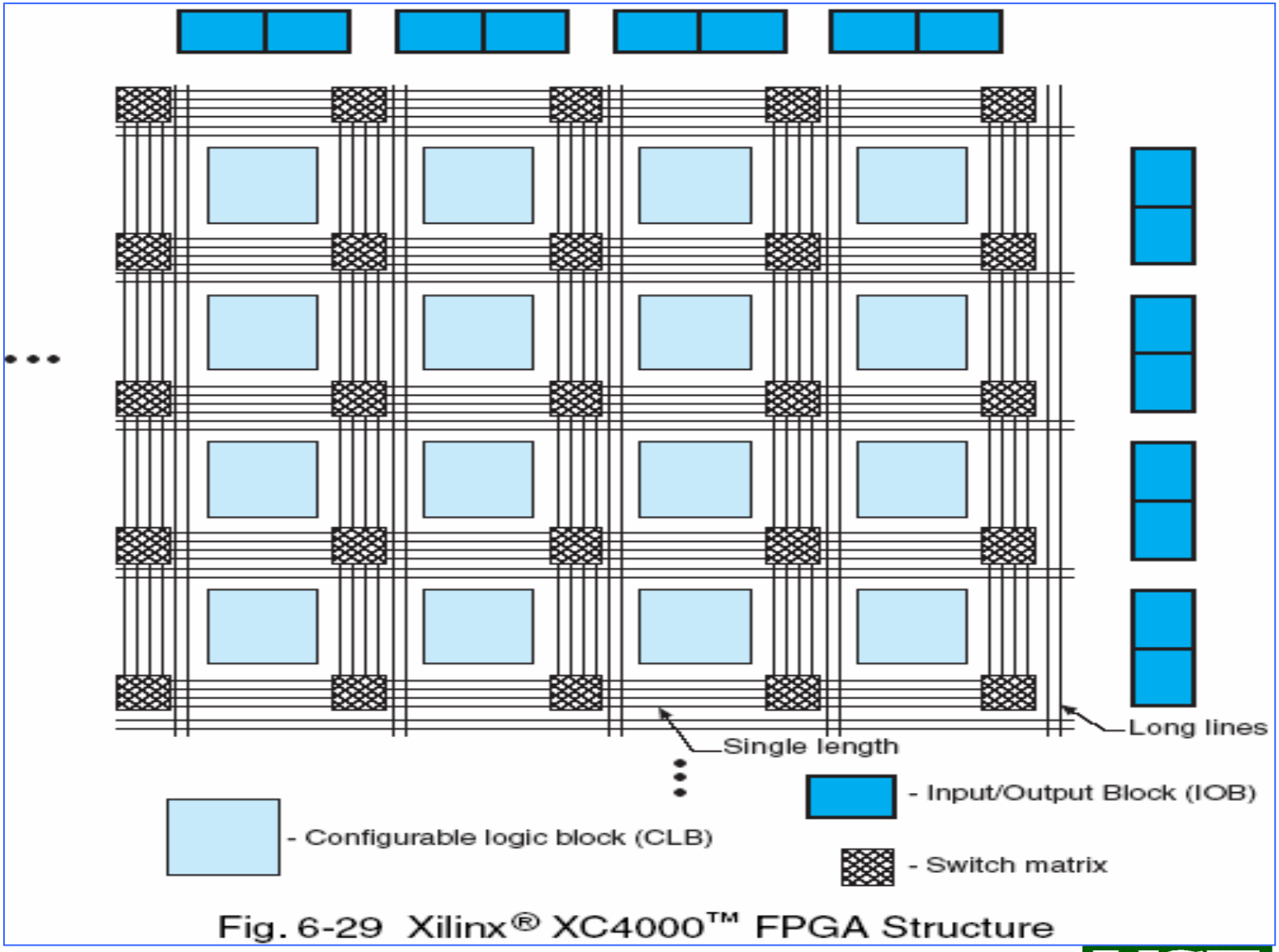



Fig. 6-29 Xilinx® XC4000™ FPGA Structure

# VLSI Programmable Logic Device: Xilinx …

- The logic is implemented in an array of programmable blocks of logic called configurable logic blocks (CLBs).
- The input to and output from the array is handled by input or output blocks (IOBs).
- Connections among CLBs and IOBs are programmed.
- Xilinx uses SRAM technology to store the programming information.
- Three techniques used to control the SRAM bits:
  - Pass transistor control
  - Multiplexer control
  - Lookup table implementation

# VLSI Programmable Logic Device: Xilinx …

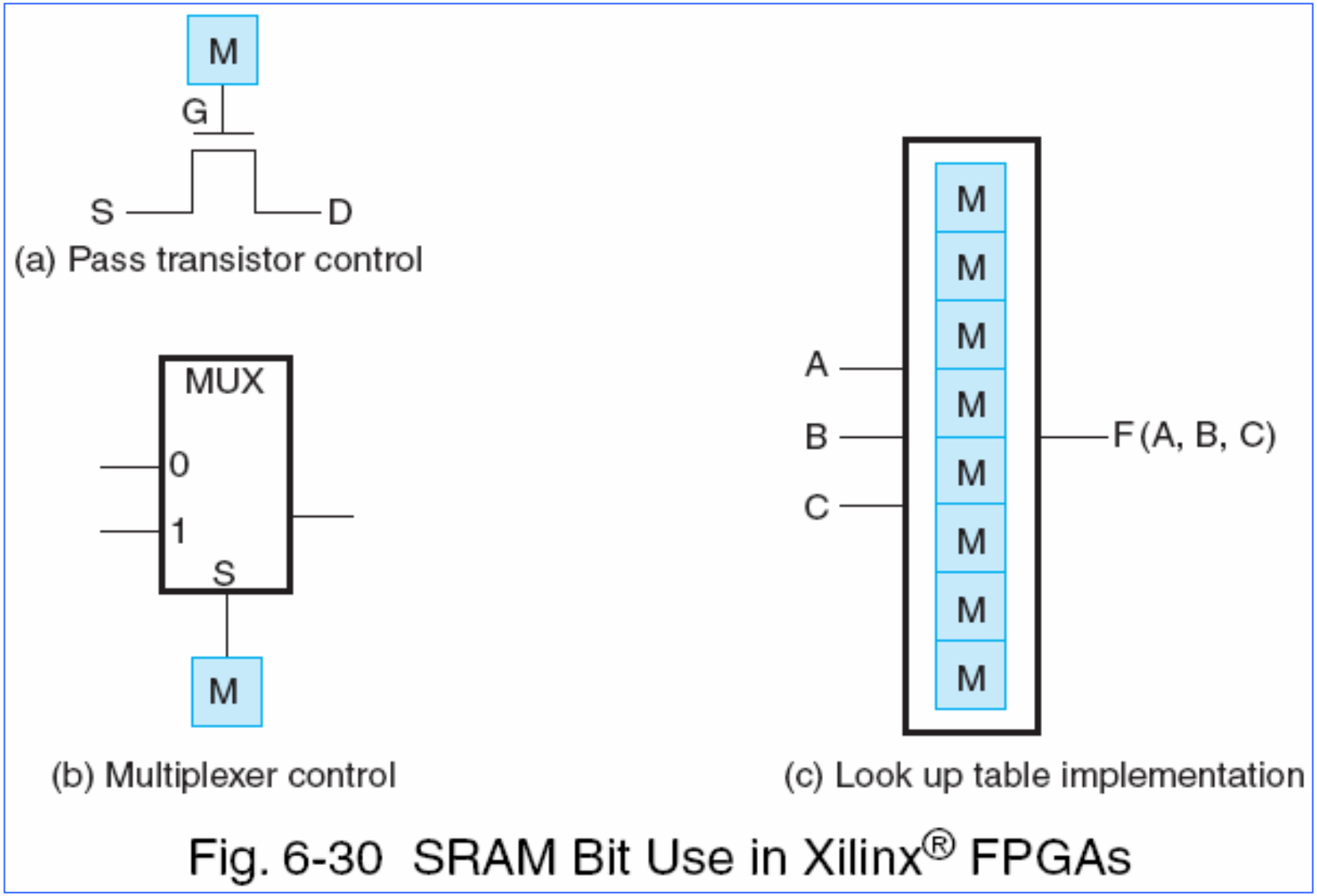



Fig. 6-30 SRAM Bit Use in Xilinx® FPGAs

# VLSI Programmable Logic Device: Xilinx …

- Long Lines: Wiring segments spanning entire length of the array
- Single Length Wiring: Span a single CLB (similarly, double length wiring)
- Interconnection is done using switching matrix.
- Fig a: Four segments, six transistors each, one vertical one horizontal, and four diagonal.


(a) Switch Matrix Transistors (b) Examples of Connections

Fig. 6-31 Example of Xilinx® Switch Matrix (Adapted

# VLSI Programmable Logic Device: Xilinx …

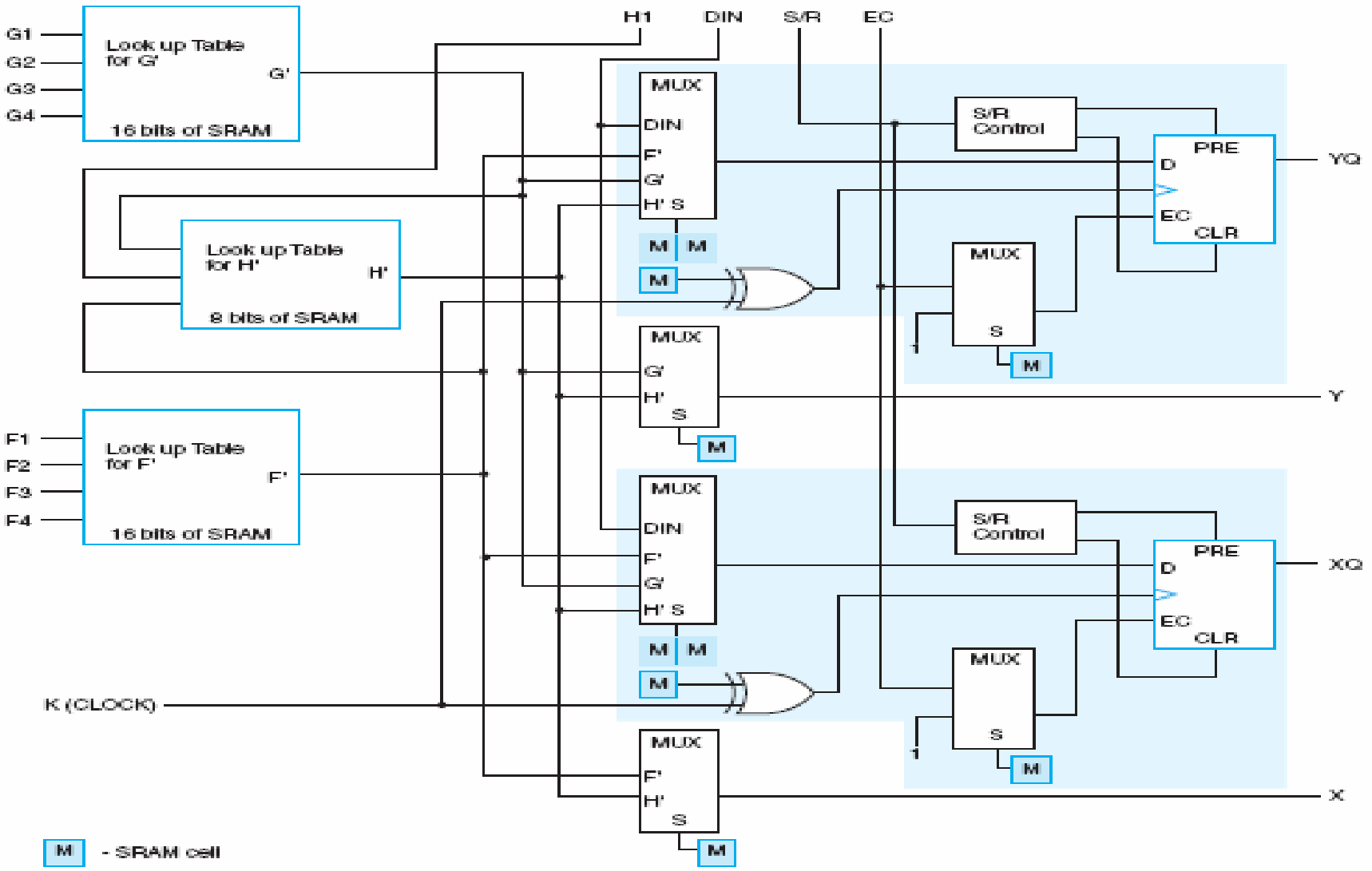



Fig. 6-32 Simplified Diagram of a Xilinx® Configurable Logic Block

# VLSI Programmable Logic Device: Xilinx …

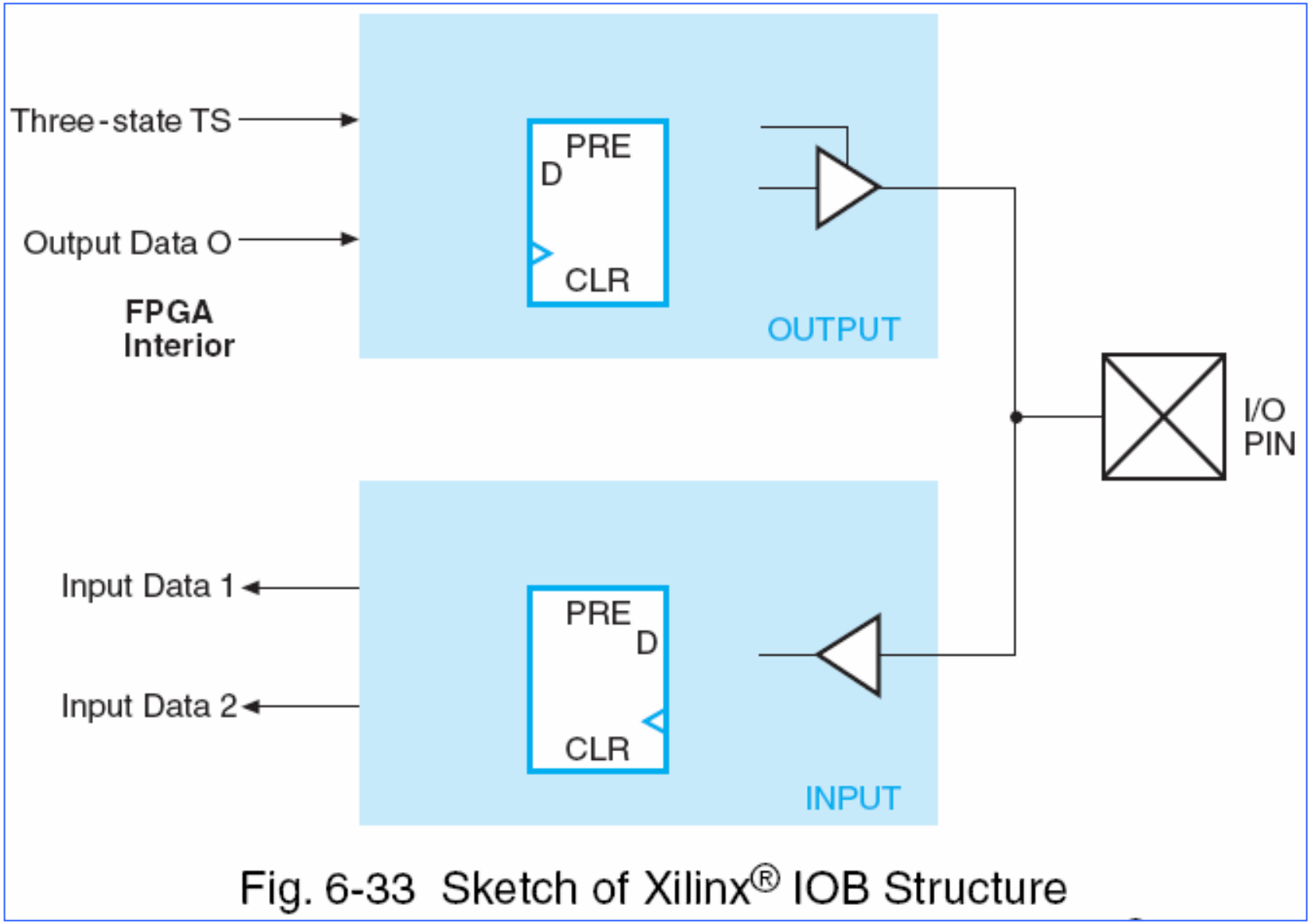



Fig. 6-33 Sketch of Xilinx® IOB Structure