Lab 1 (16 Sep 2004): CSCI 4330 /5330: Digital Systems Design with VHDL

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Lab Policy and Rules: **Attendance for the labs is mandatory**. Every Thu day new lab assignment will be given. Students need to work on it and demo during the lab session on immediate Thu day. Then, give a report including description of the work, schematic diagram or VHDL code, and simulation waveform in the class on immediate Tues day, after the demo. For example: If 16th Sep (Thu) new lab work is given then it needs be completed and demo should be shown by 23rd Sep (Thu), and the report is due 28th Sep (Fri).

Lab1: This is the first lab, we will do small schematic design and simulations, and demo may or may not be needed. But, report is **due 21st Sep (Tue).** Following one/two circuits will be simulated depending on time availability.

1. Logic function of Fig 2.30 (page-834 or page-60), discussed in last lecture.
2. Design and simulation of circuit of problem 3.3 (page-154).