Lab 2 (23 Sep 2004): CSCI 4330 /5330: Digital Systems Design with VHDL

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1. Do schematic designs of the circuit shown in Figure P3.1 (page-153), simulate the circuit, and check if this matches with the truth table you obtained in written assignment 1.
2. Repeat above for the circuit shown in Figure P3.2 (page-153).
3. If any thing remains undone from the previous lab assignment (Lab1).