Lab 4 (7 Oct 2004): CSCI 4330 /5330: Digital Systems Design with VHDL

Instructor: Saraju P. Mohanty

1. Using VHDL design a 4-bit ripple carry adder and simulate it for functional correctness.
2. Using VHDL design a 4-bit carry lookahead adder and simulate it for functional correctness. You need to mention in the lab report what differences do you observe in the design (1) and (2).
3. Modify one of the above designs for 4-bit subtractor and do its functional verification.
4. Merge the design (1) and (3), or (2) and (3) and design a unit that can do both 4-bit addition and 4-bit subtraction. You need to insert a control signal to choose either addition or subtraction.