Lab 7 (28 Oct 2004): CSCI 4330 /5330: Digital Systems Design with VHDL

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Consider a register file with 6 ports; four input ports and two output ports. Three input ports take register numbers as input and other input port takes data. Two output ports provide output data. Additionally, there are read/write signal, clear signal etc. You need to model such as register file circuit using structural VHDL. Define appropriate port interface for each component, which should be parameterized. However during instantiation chose a size of your choice, say 4-bit to match with all our designs so far in previous lab works.