Lab 8 (4 Nov 2004): CSCI 4330 /5330: Digital Systems Design with VHDL
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In this lab you need to design a small prototype datapath circuit and simulate it. Let assume that the datapath consists of an ALU and a register file. The operations to be supported are, (i) addition, (ii) subtraction, (iii) multiplication, (iv) OR, (v) AND, (vi) NOT, (vii) NAND, (viii) NOR, and (ix) XOR. The register file is used to store the data; data is read from the register file and the result is written back to the register file.