WELCOME TO

CSCI 4330 or CSCI 5330
Digital System Design with VHDL

Instructor: Saraju P. Mohanty, Ph. D.

CSCI 4330 or CSCI 5330
Digital System Design with VHDL

Things to do:

- Instructor's introduction
- Student's attendance
- Student's introduction
- Prerequisite form fill up

Class Time and Venue

- **Course Homepage:**
  http://www.cs.unt.edu/~smohanty/teaching/DigitalSystemDesignWithVHDLfall2004
- **Class Timing and Venue:**
  TR 2:00-3:20pm and NTRP B192 (NOTE: From 16th Sep 2004 every Thu Day class will be a laboratory session in NTRP F218).
- **Instructor's Office:**
  Office Hours: MW 2:00-3:20pm (any other time possible by appointment through email)
  Room: NTRP F277
  Email: smohanty@cs.unt.edu
  Homepage URL: http://www.cs.unt.edu/~smohanty/

Course Syllabus and Description

Course objectives:

- This course is about design of digital systems using a hardware description language, VHDL.

- Students will be taught about the building of the individual components of a computer such as ALU, register file, and RAM, and how to put them together in constructing a computer.

- Students will acquire practical working knowledge of creating digital circuits using Computer-Aided-Design (CAD) tools.

Course Syllabus and Description ….

- **Prerequisites:** Minimal knowledge of computer logic design. Students with no background need to talk to the instructor.
- **Level of the Course:** The course is designed for junior or senior undergraduates and first year graduate students.
- **Text Book:** Fundamentals of Digital Logic with VHDL Design, Stephen Brown and Zvonko Vranesic, Mc-Graw-Hill (2nd edition). Book website: http://auth.mhhe.com/engcs/electrical/brownvranesic/index_vhdl.mhtml.
- **Reference Book:** Designers guide to VHDL, Peter J. Ashenden, Morgan Kaufman Publishers, or The Student's Guide to VHDL, Peter J. Ashenden. Website: http://www.ashenden.com.au/
- **Course Software:** Students should have access to a computer to do the assignments and projects. The computer may be either one's own PC/laptop or a PC in general access laboratory. The student's edition free software from Altera (http://www.altera.com/)

Course Syllabus and Description ….

Selected Topics (Tentative):

- Basics of digital design
- Design of combinational functional blocks (e.g. decoders, multiplexers, adder, multipliers, etc.)
- Design of sequential functional blocks (e.g. registers, counters, etc.)
- Design of Memory elements
- Building simple and pipelined datapaths (ALU, register file and their interconnection paths)
- Sequencing and control -- hardwired control and microprogrammed control
- Single-cycle computer, multi-cycle computer, a pipelined computer design
- Much more ……..

What will you gain from this course ??

- Learning a new language VHDL (item in CV)
- Learning CAD tools (item in CV)
- Designing and simulating hardware units, such as adders, subtractors, multipliers, etc.
- Understanding inner details of processors
- Designing processors of your own

Course policy

- **Attendance for this course is mandatory** . In case of absence due to unavoidable reasons, substantial documented evidence needed.

- Several **assignments** including exercise problems and design works using VHDL will be given. The written or typed solutions for exercise problems and reports for VHDL design works must be submitted in the class by 3:20pm of announced deadline, else **there will be late penalty of 20%**. Under no circumstances late assignment will be accepted two days after deadline and score for such assignment will be zero.

- Several surprise **quizzes** will be given in the class. There will be no make up quiz for any student under any circumstances.

Course policy …..

- **There will be three tests of equal weightage.** There will be no final test. The tests will be approximately evenly spaced throughout the semester.
- Any makeup test will not be given unless substantial documented evidence is provided for a reasonable excuse of absence. In the absence of the documented evidence, score for the test will be zero.
- Any questions regarding the test grades should be clarified **a week of returning the test**.
- There will be an additional project work for the graduate students.
- All news will be announced in **news section** of course home page. **Students are expected to check this section from time to time.**
- **Dishonesty in this class will be handles as per the University of North Texas policy (http://www.unt.edu/csrr/).**

Tests Dates

Test No	Test Date	% of Final Grade (Undergraduate)	% of Final Grade (Graduate)
Test1	28th Sep 2004 (Tue)	20	16
Test2	26th Oct 2004 (Tue)	20	16
Test3	30th Nov 2004 (Tue)	20	16

NOTE: (i)Tests will be closed book and closed notes, but calculators are allowed.

(ii) Test dates will not be changes under any circumstances.

Grading Procedure

Undergraduate Grade Distribution

Items	% of Final Grade
Tests	60
Assignments	30
Quizzes and Attendance	10

Graduate Grade Distribution

Items	% of Final Grade
Tests	48
Assignments	24
Quizzes and Attendance	8
Project	20

Grading Policy

A >= 90
90 > B >= 80
80 > C >= 70
70 > D >= 60
60 > F

NOTE: (i) Grading policy may change if University or Dept. decide so.

(ii) There will be no border grade concessions.

Some Questions ??

- What's the background of individual student ?
- Why are they taking this course ?
- What's their expectation from this course ?
- How much time can a students spend on this course per week ?
- Has a student ever done logic design course ?
- Has a student ever done computer organization, computer architecture, etc. courses ?