Quartus II 4.1 Software Installation and Use (Instructor: Saraju P. Mohanty)

- Installation of Quartus II 4.1 Software
- Getting free license for the software
- Creation of Projects
- Simulations of a Schematic Circuit

NOTE: Many slides are borrowed from
http://www.cs.utsa.edu/~danlo/research/VHDL/quartus2tutorial.htm

Getting the Software and License

- We need a CAD software called “Altera Quartus II” for digital logic simulation in this class.
- Your textbook has a CDROM of this software package on the back cover containing 4.0 version.
- You may download the Web Edition Software directly from Altera website: https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp
- You may obtain a license file from Altera for either 4.0 or 4.1 here: https://mysupport.altera.com/login/signin.asp

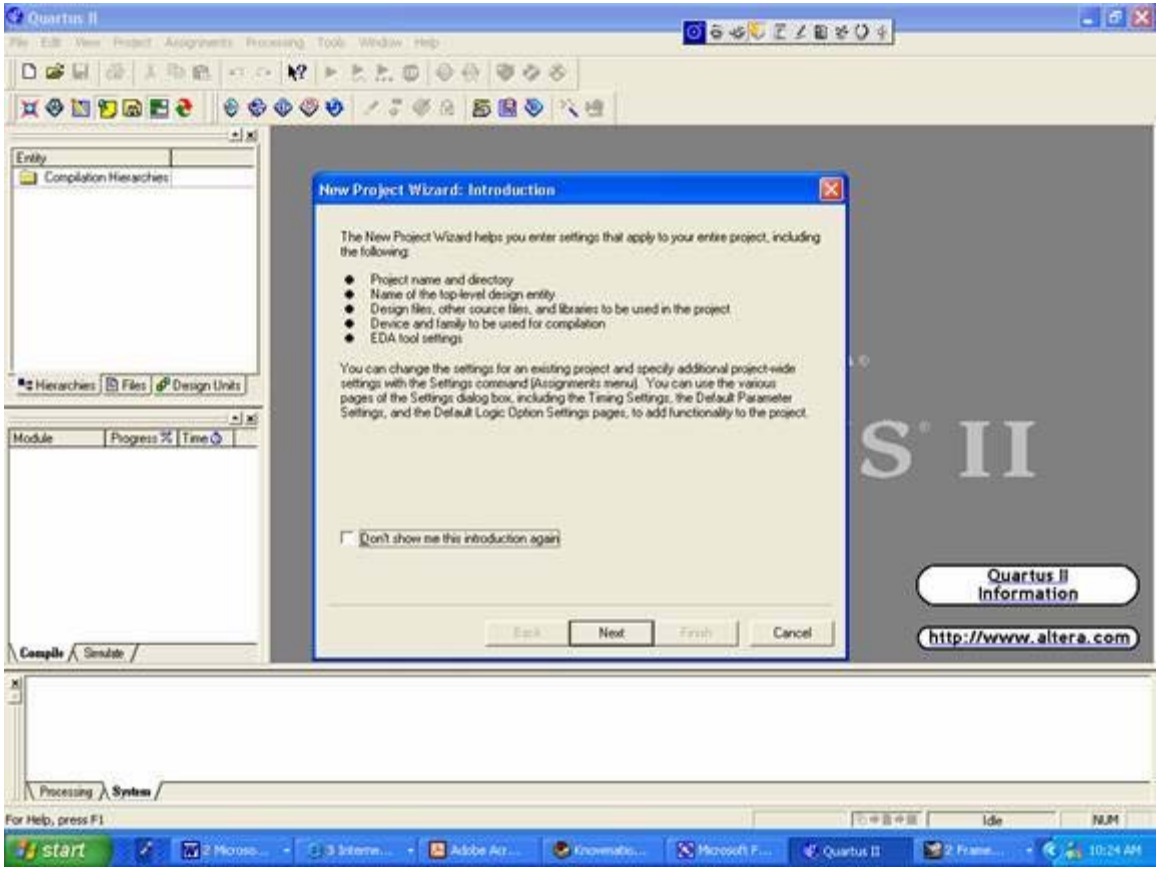
Installing the Software and License

- Install the software by executing the file: quartusii_41_web_edition_single
- Save your license file to your computer's hard drive. Altera recommends saving the file into your c:/quartus directory with a ".dat" file name extension.
- In the Quartus II software, choose License Setup (Tools Menu).
- In the License File box type or browse to the full path and file name of the file you saved before.

Project Creation: New Project

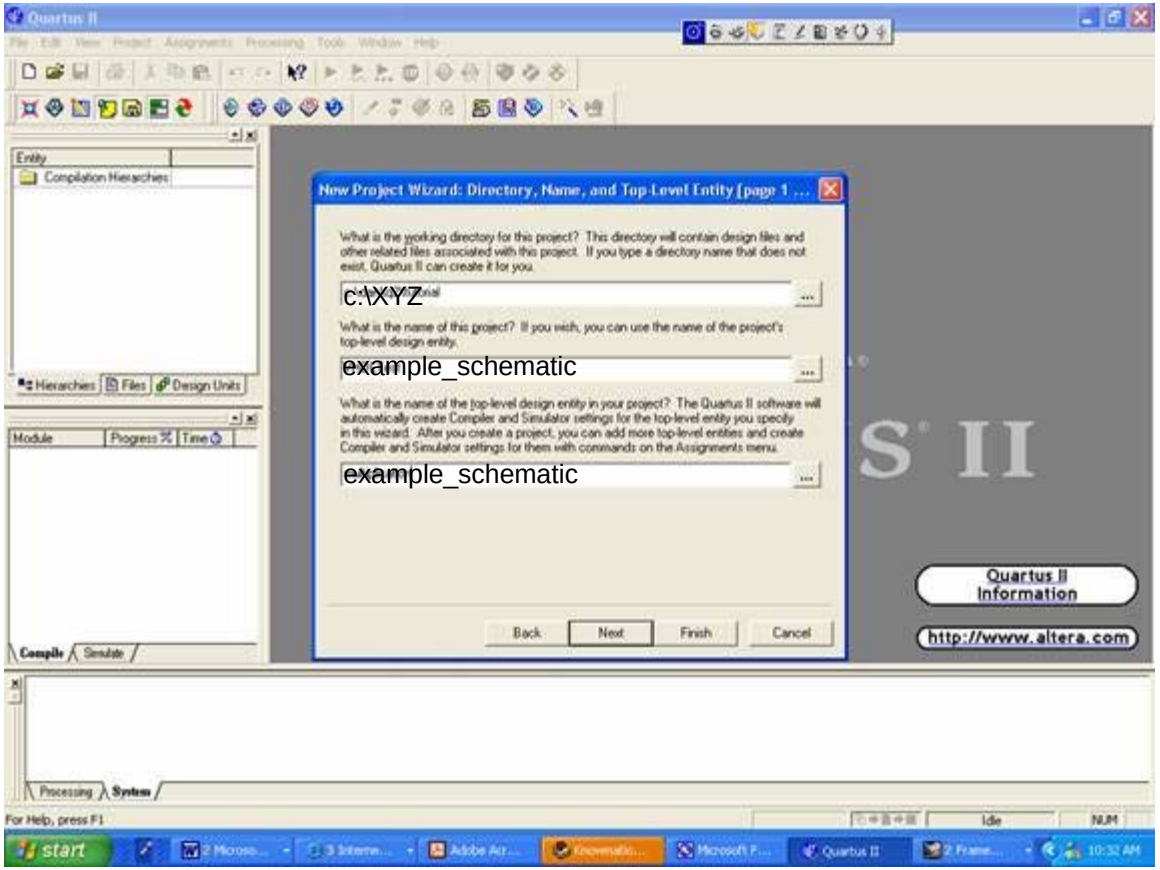
- Every design in Quartus II has to be in a project.
- A project includes project name and directory, name of the top-level design entity, design files (VHDL or schematic), libraries, timing info, devices, etc.
- Quartus II allows us to use thirty party EDA tools. Thus, this EDA setting is included in the project as well.

[File]->[New Project Wizard]



Project Creation: Working Directory

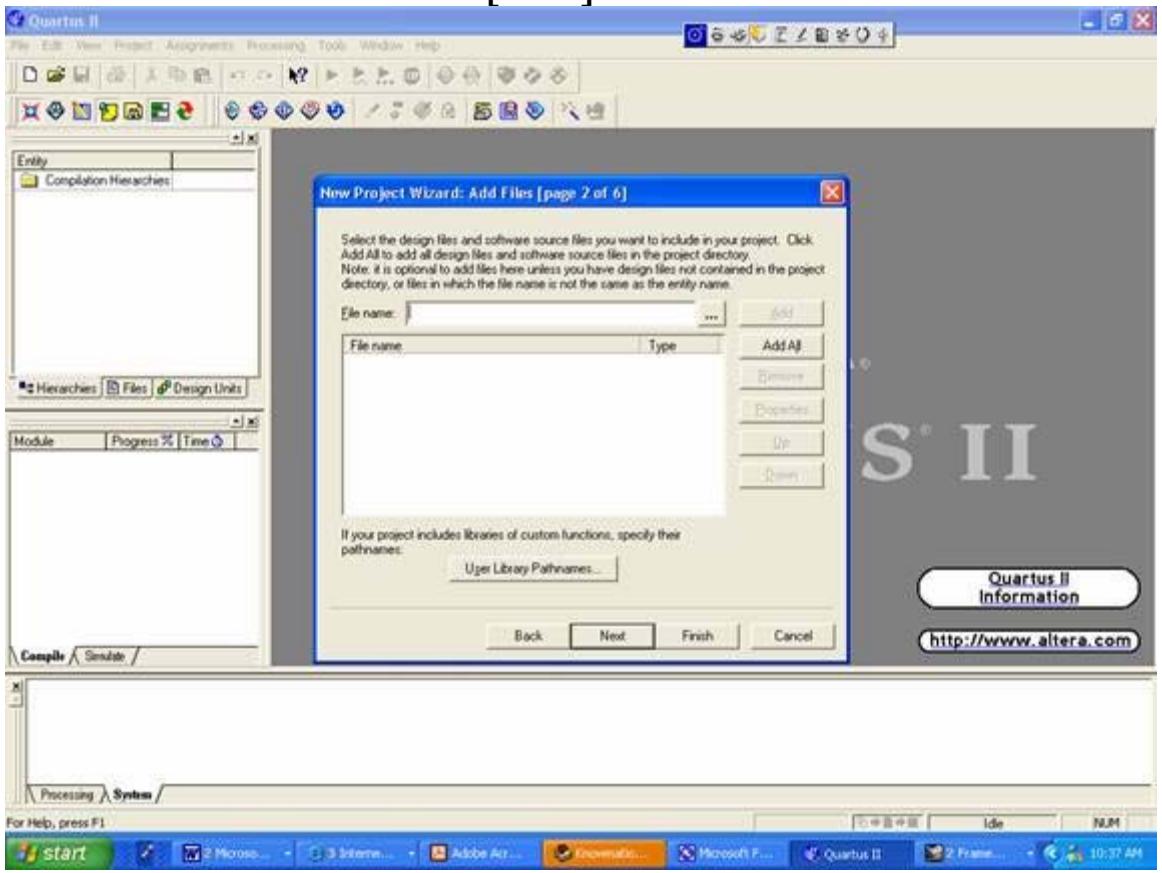
- Click [Next]



- Type “c:\XYZ” in the first textbox. This will be the working directory for the project.
- Then type “example_schematic” in the second textbox. This will be the name of the project.
- Type “example_schematic” in the third textbox as a top-level design entity.

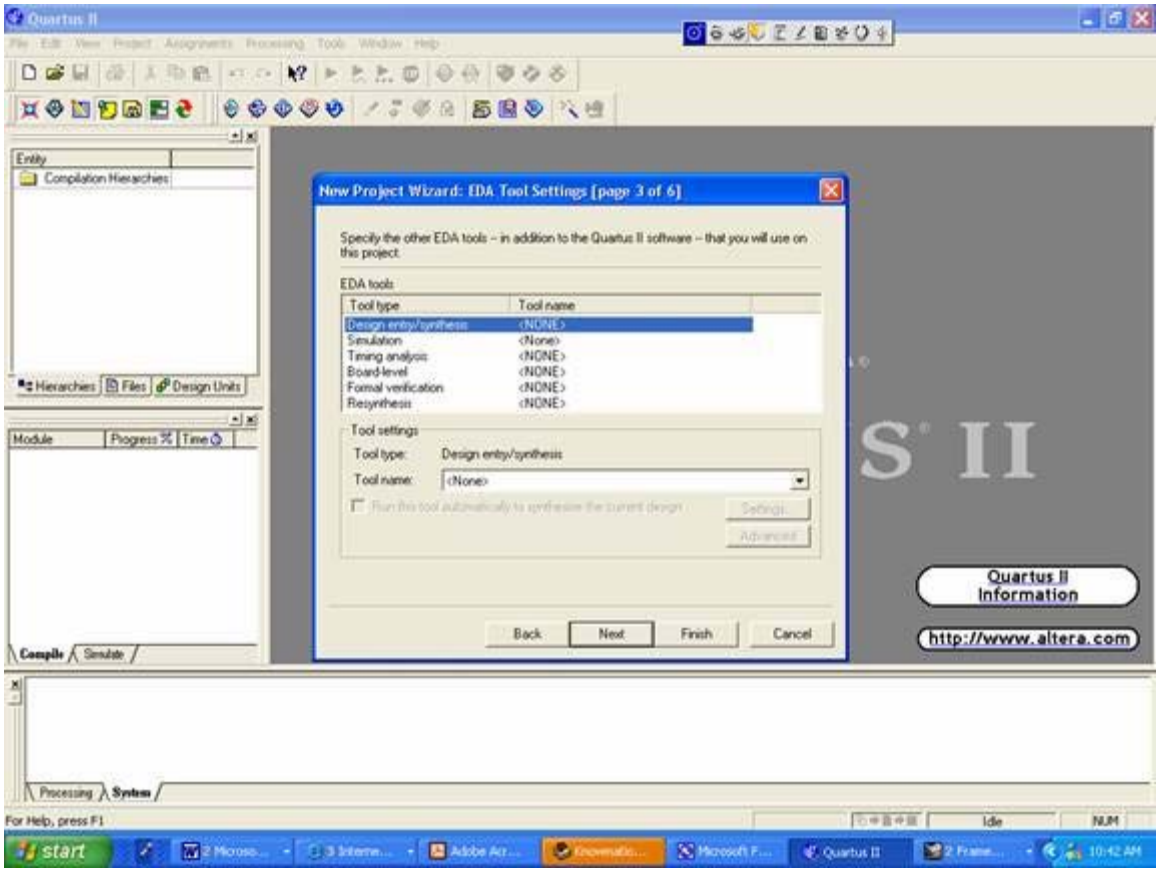
Project Creation: Add Files

- Click [Next], a pop-up window asks you “Directory c:\XYZ” does not exist. Do you want to create it?” Click [Yes].



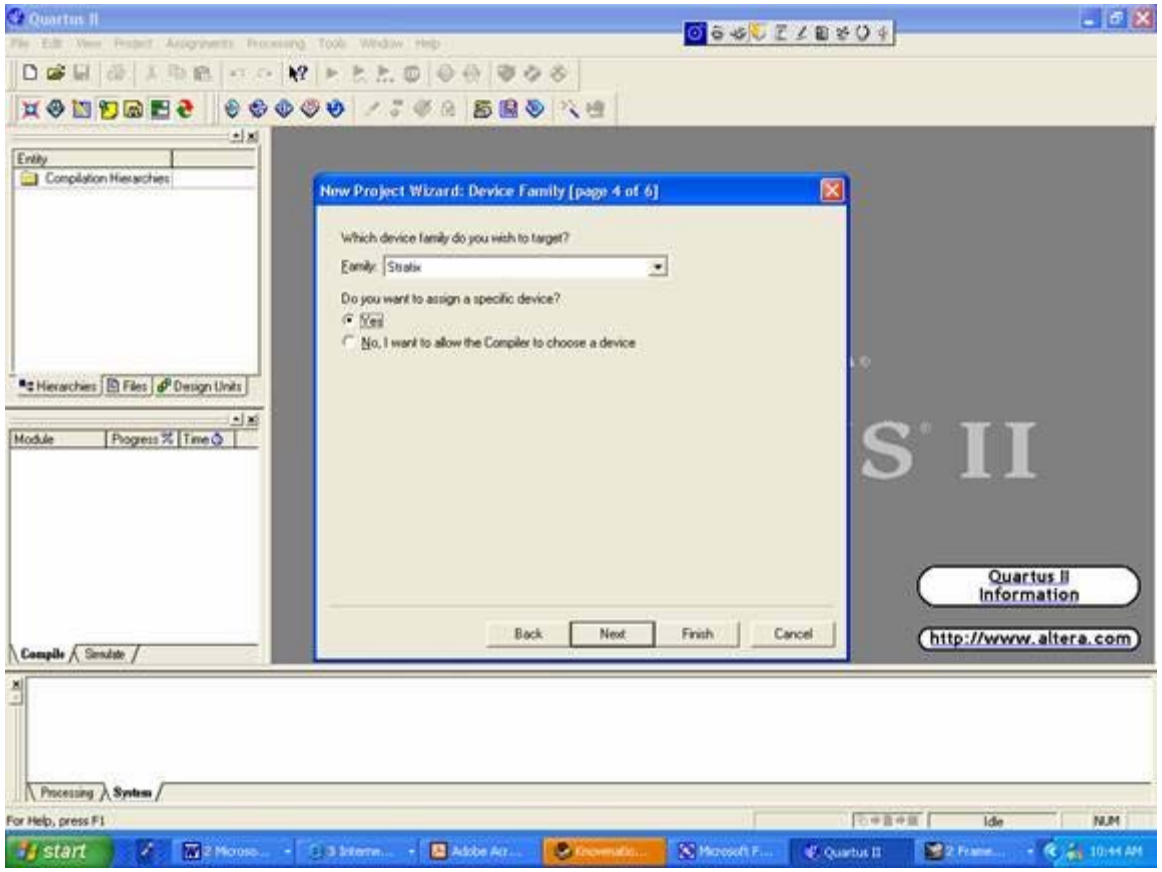
- This window asks you if you have design files and software source files to include in the project and set the path to user-defined libraries. Simply click [Next].

Project Creation: Using External EDA Tools



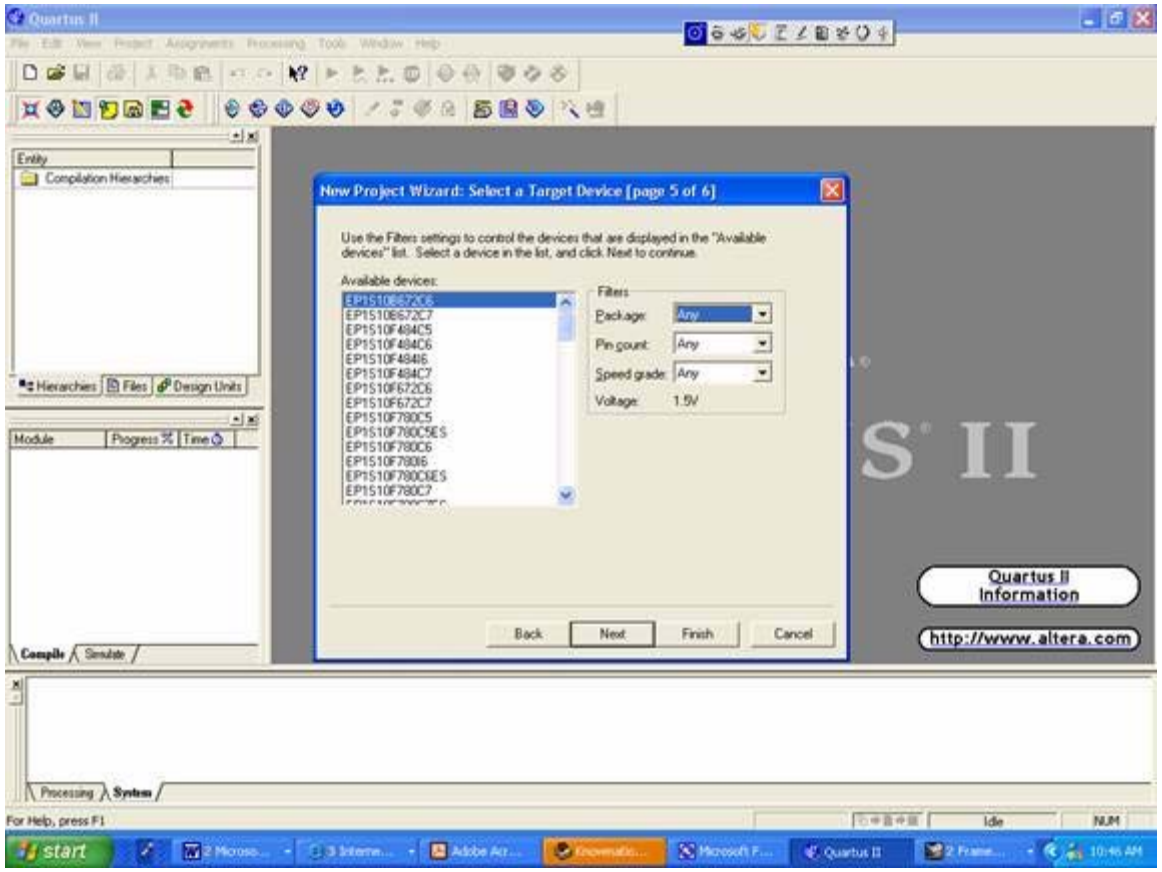
This window specifies other EDA tools to be used in this project. Simply click [Next] to use the Quartus II only.

Project Creation: Device Family



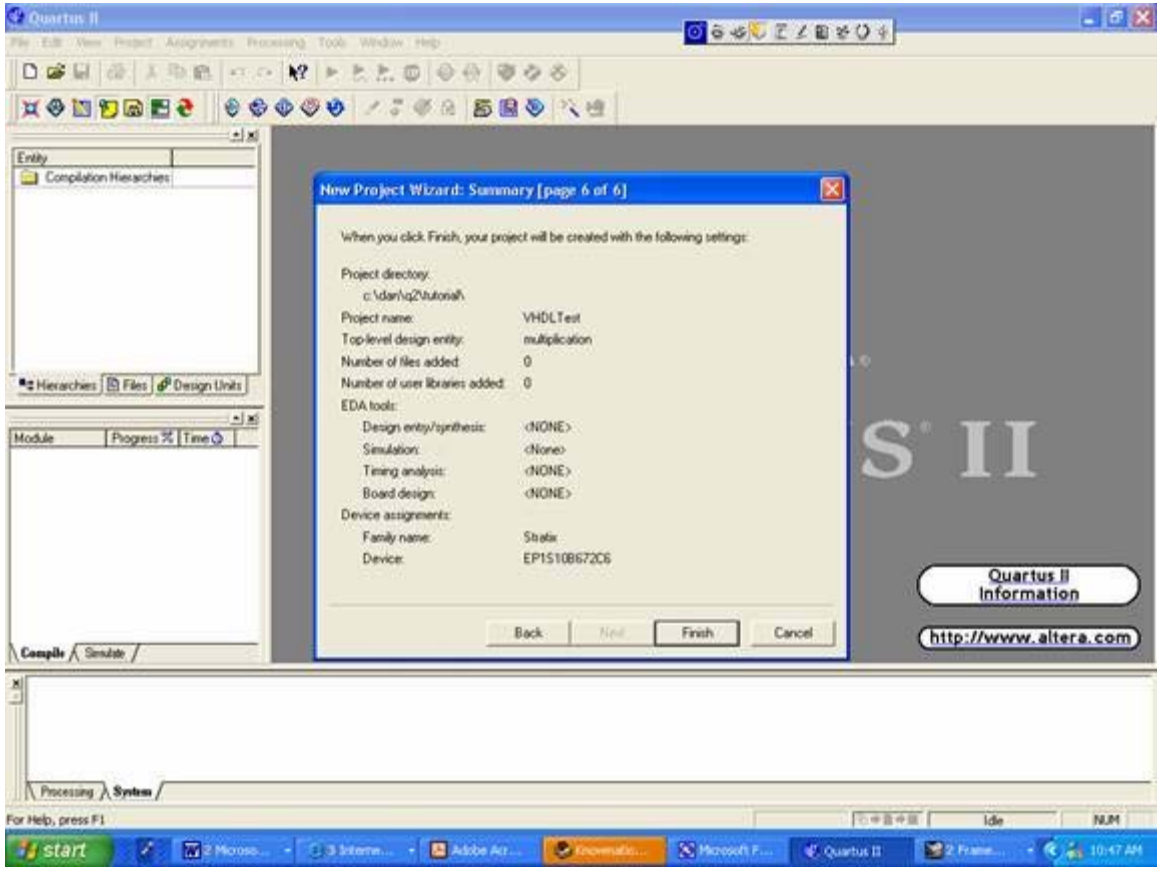
This selects device family to be targeted. Say, choose "Stratix" or any other family and [Yes]. Then Click [Next].

Project Creation: Specific Device



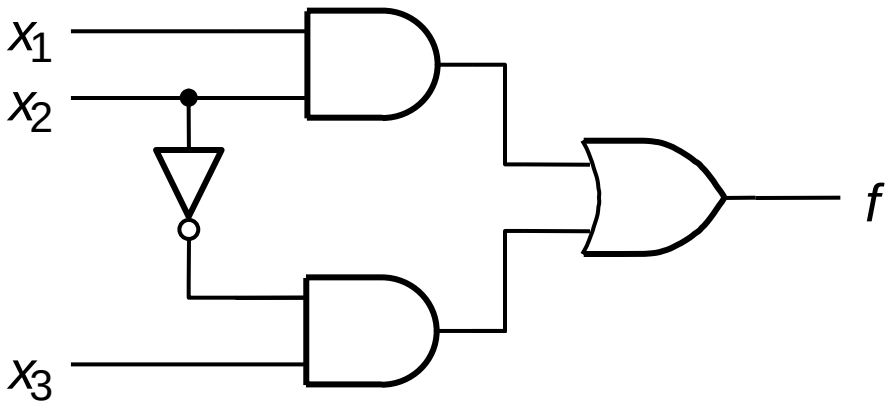
This selects a specific Stratix device. Choose "EP1S10B672C6" and click [Next].

Project Creation: New Project Created



Click [Finish].

Simple Design Example: The Circuit



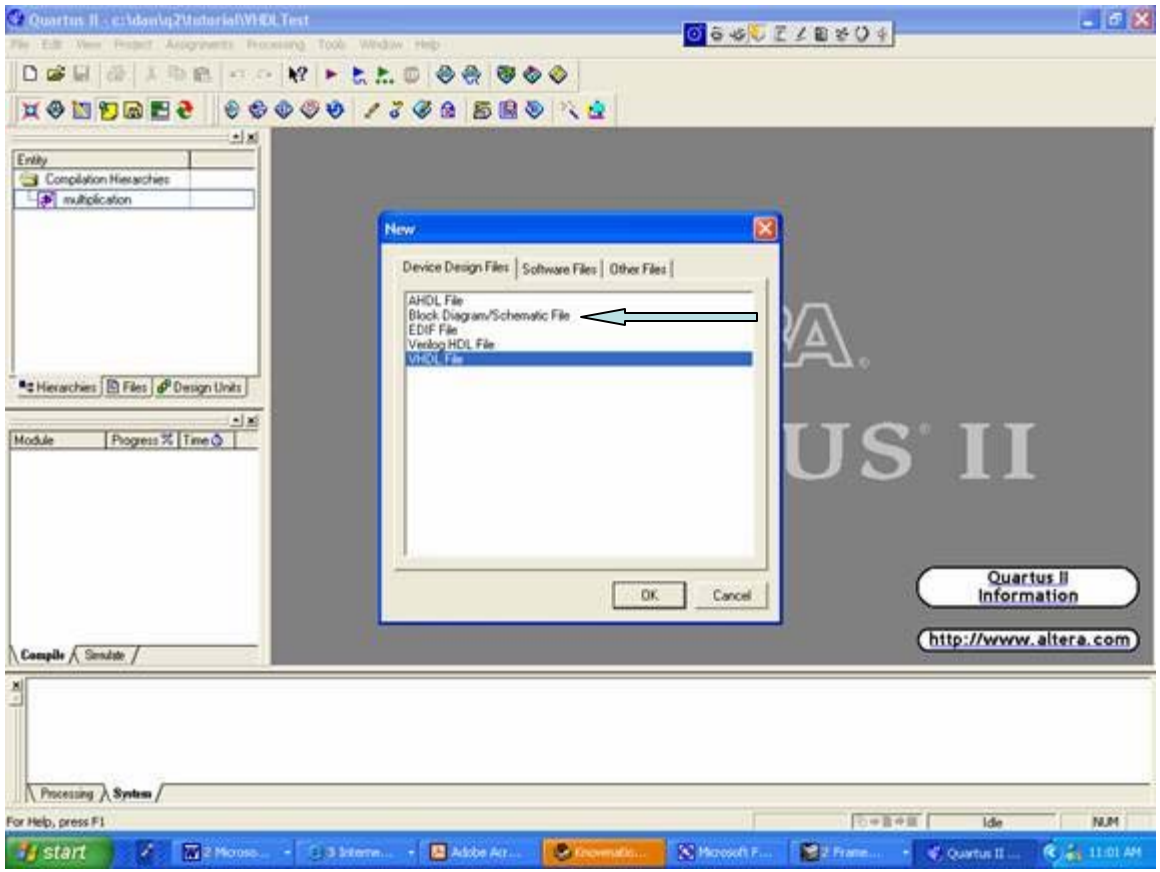
Circuit

X1	X2	X3	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table

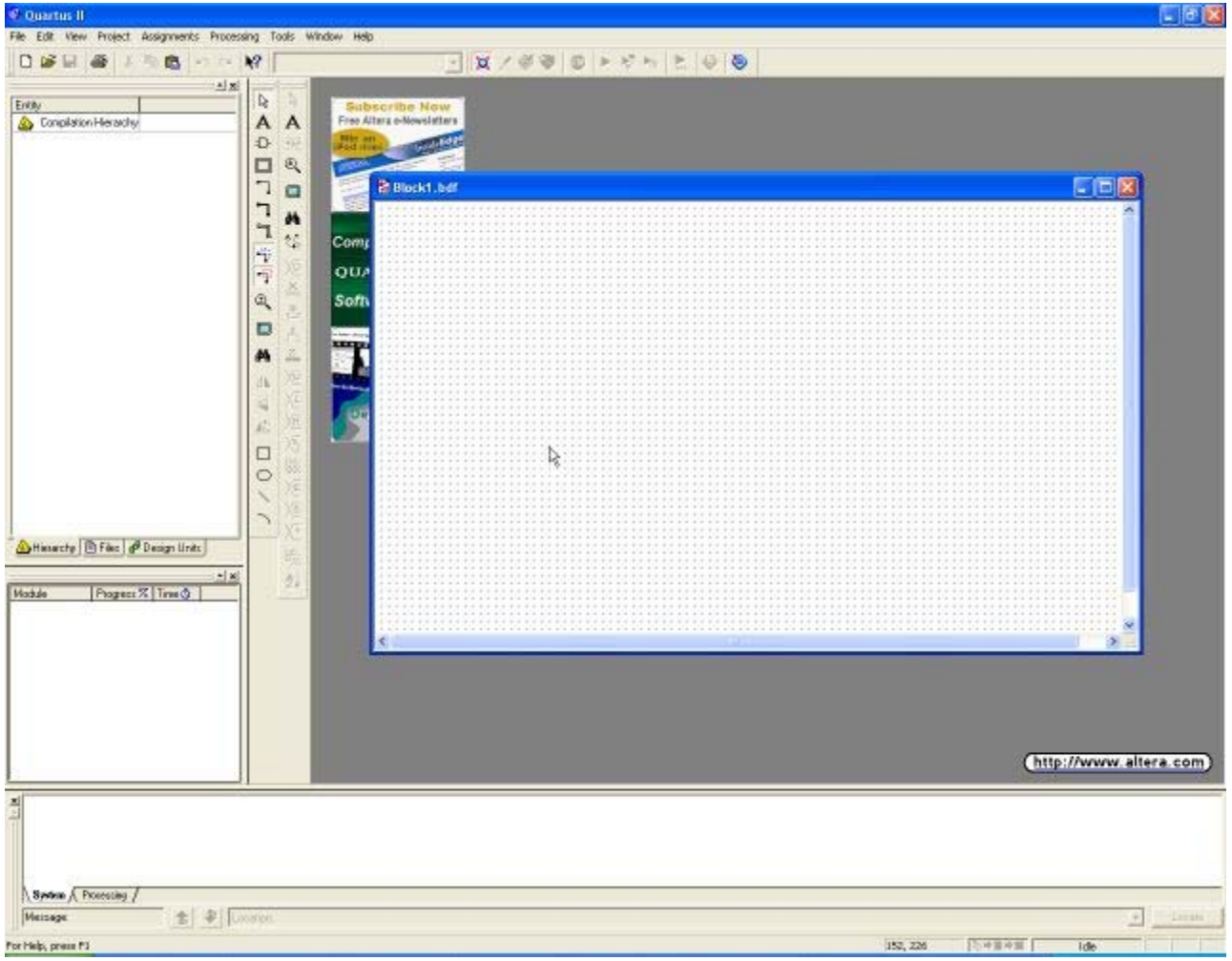
A simple logic function.

Simple Design Example: Chose Schematic



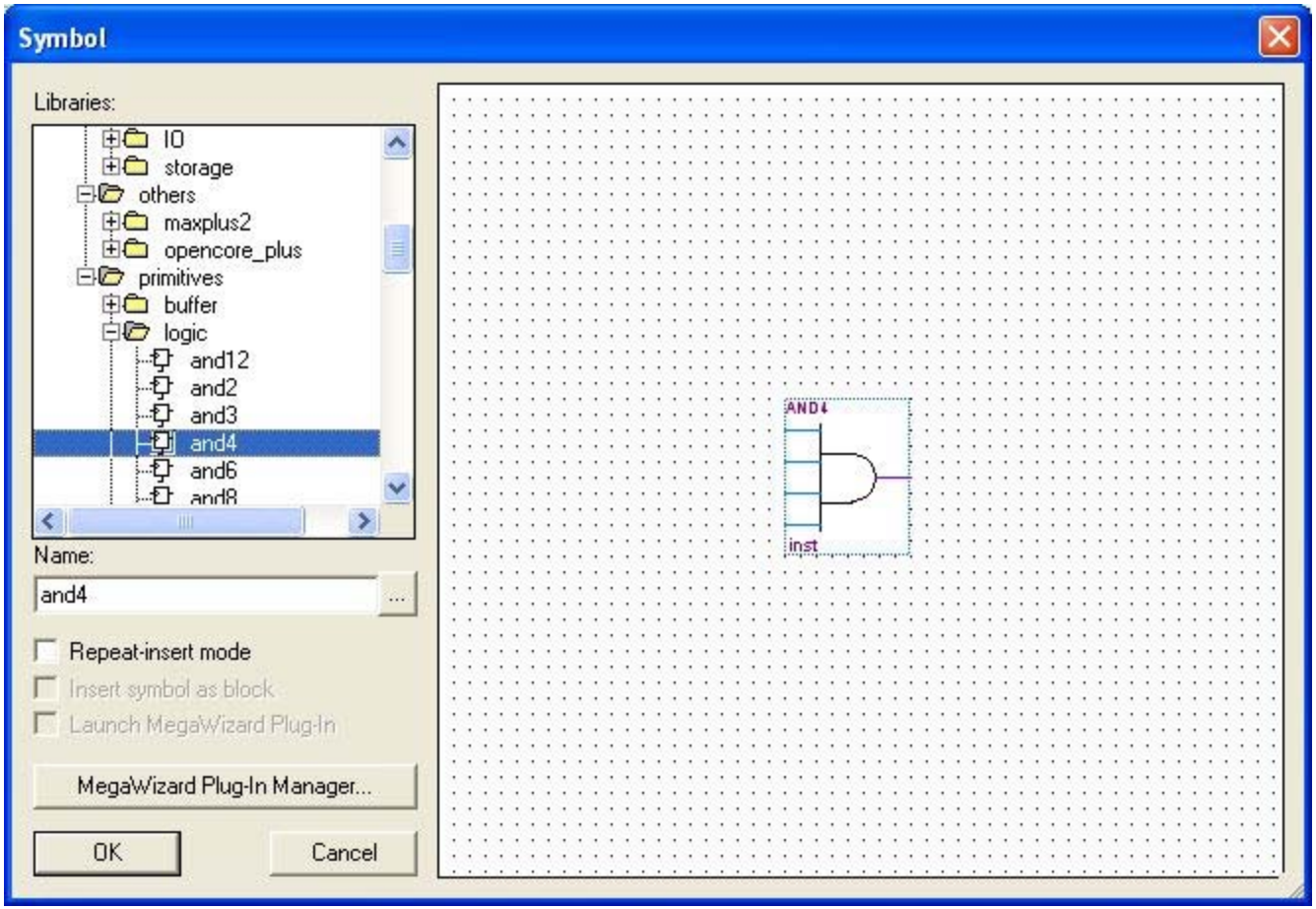
Click [File]->[New] and select “Block Diagram / Schematic File” or “VHDL File” any one of them depending on requirement. Let us select “Block Diagram / Schematic File” and Click [Ok].

Simple Design Example: Block Editor Window



Simple Design Example: Logic Symbol Selection

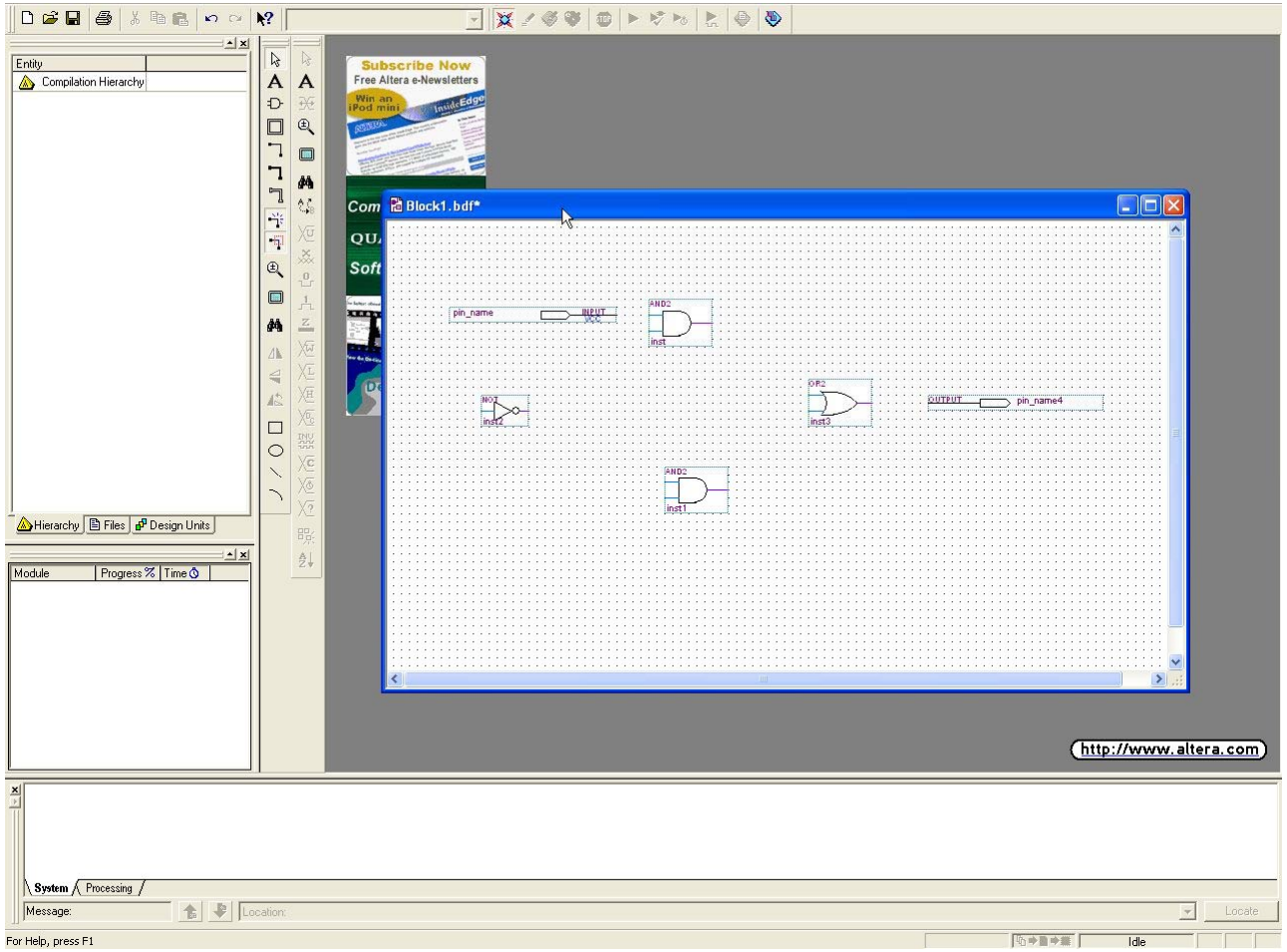
Right Click on the Editor Window, then go to Insert, then go to symbols.



Contains Followings:

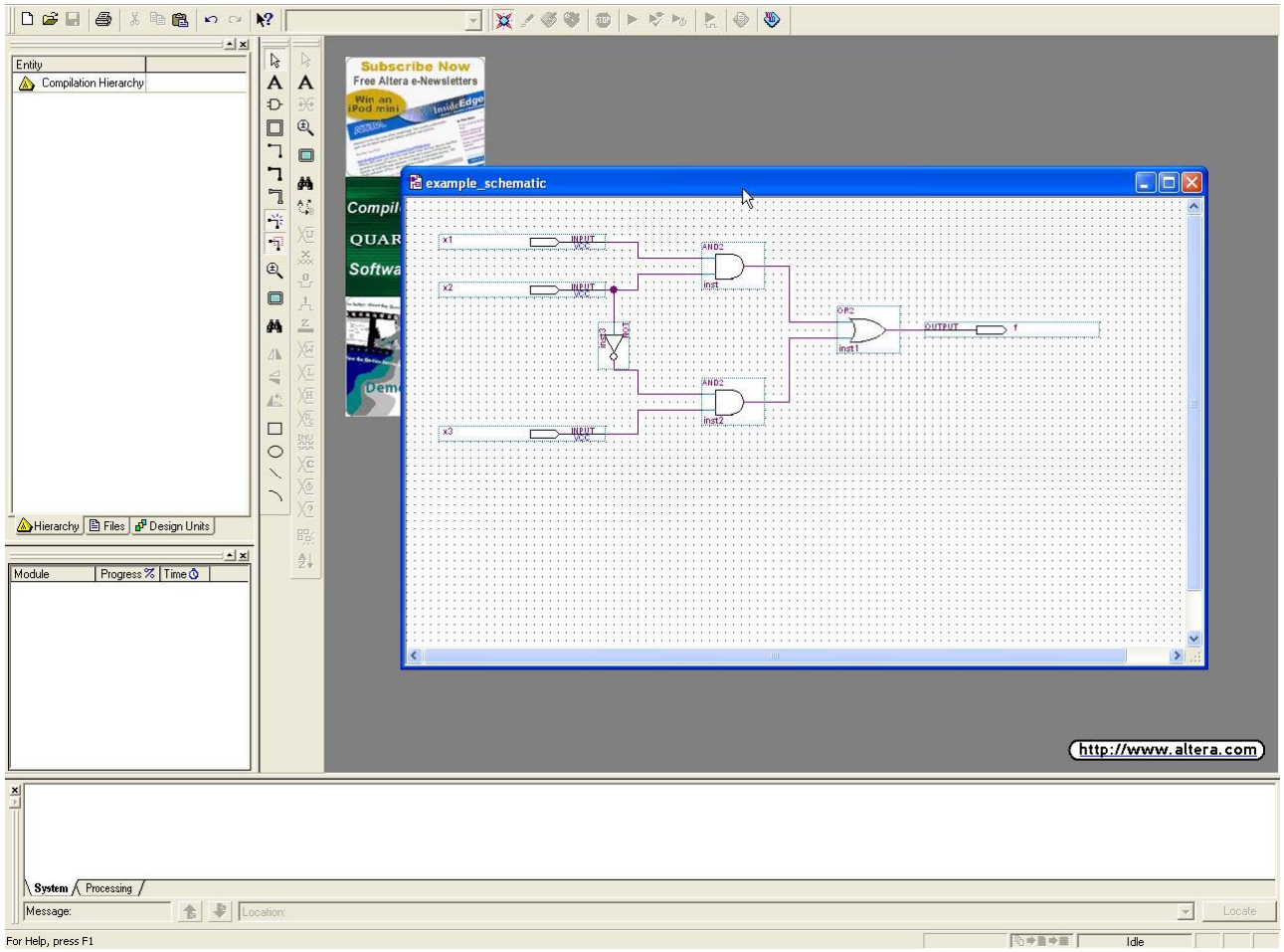
- Megafunctions (arithmetic units, etc.)
- Others (Larger Circuits, Gates, etc.)
- Primitives (Logic, Storage, IO Pins, etc.)

Simple Design Example: Import Logic Symbols



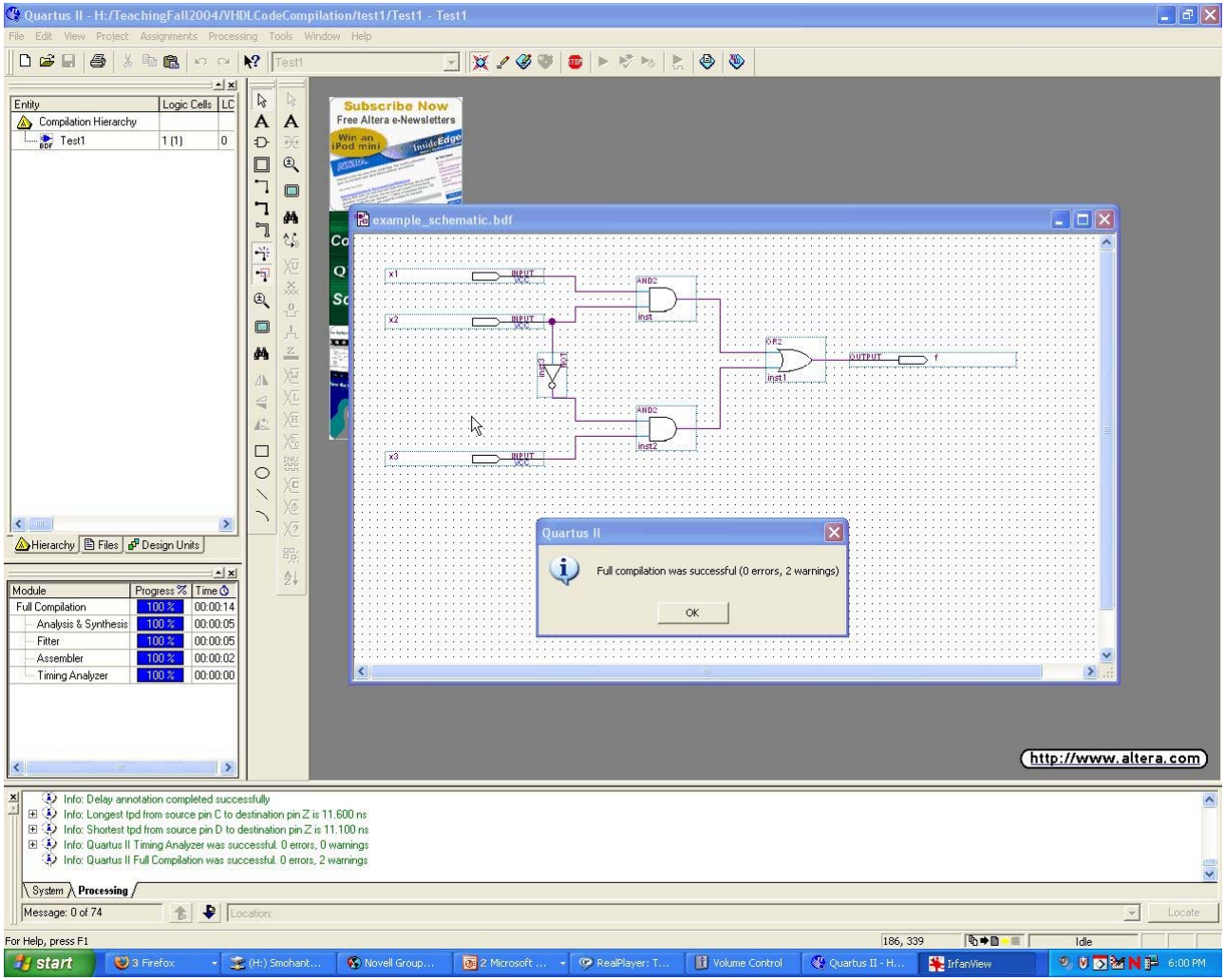
Simple Design Example: Complete Schematic

Arrange and connect various gates to construct the complete schematic diagram.

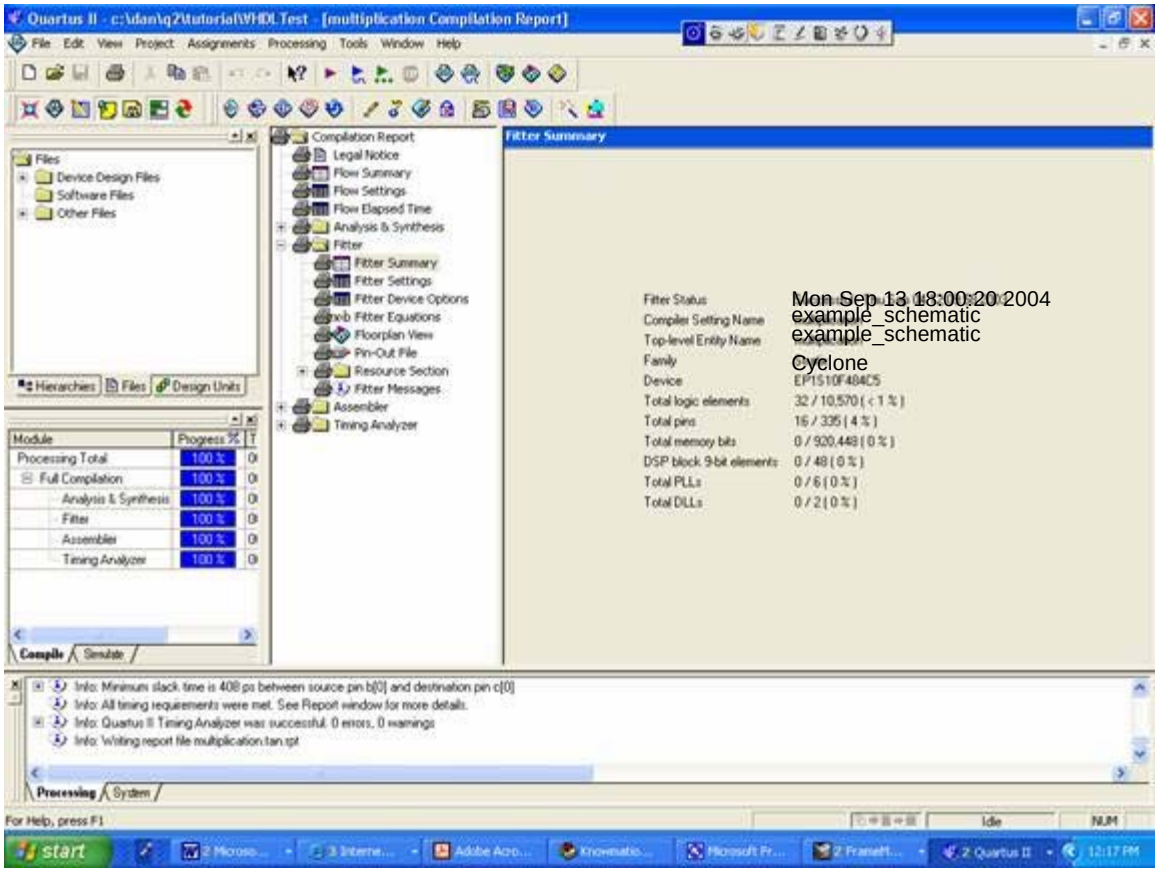


Simple Design Example: Synthesis

Start compilation from process menu or use the compiler from tool menu. Takes some time to compile, high performance computer with larger RAM is better for this tool.



Simple Design Example: Synthesis Report

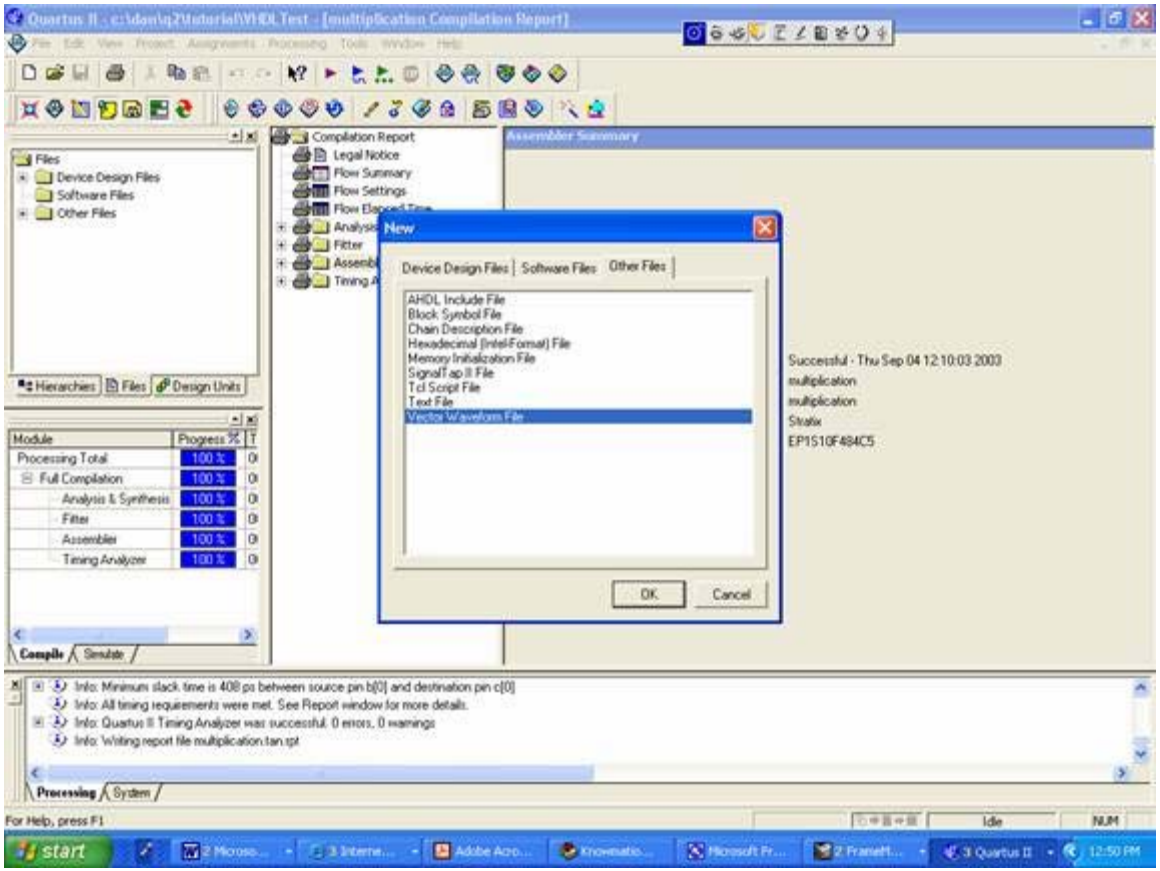


Report:

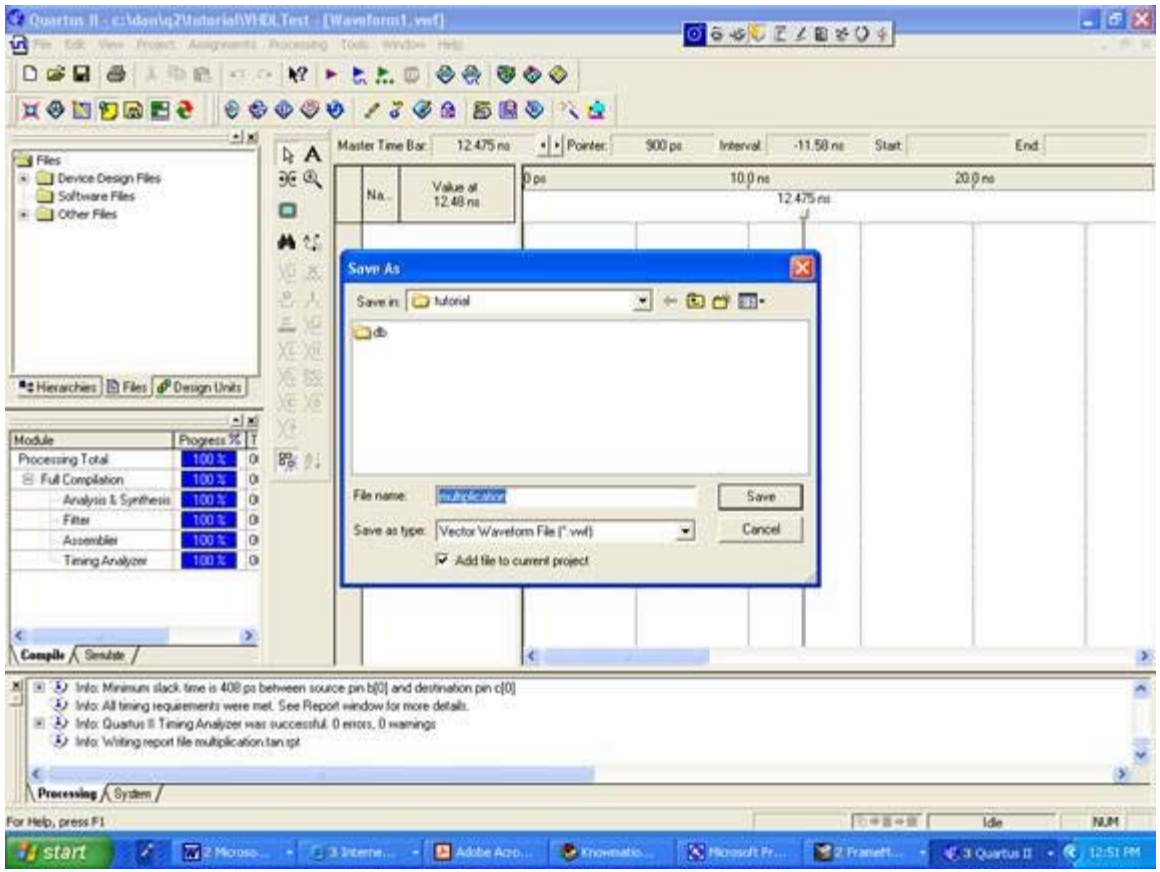
- Family
- Device
- Timing model
- Logic Elements
- Pins
- Memory
- PLLs

Simple Design Example: Simulations

To simulate a design, a vector waveform file has to be created. Go to File-New, Other Files, Vector Waveform Files

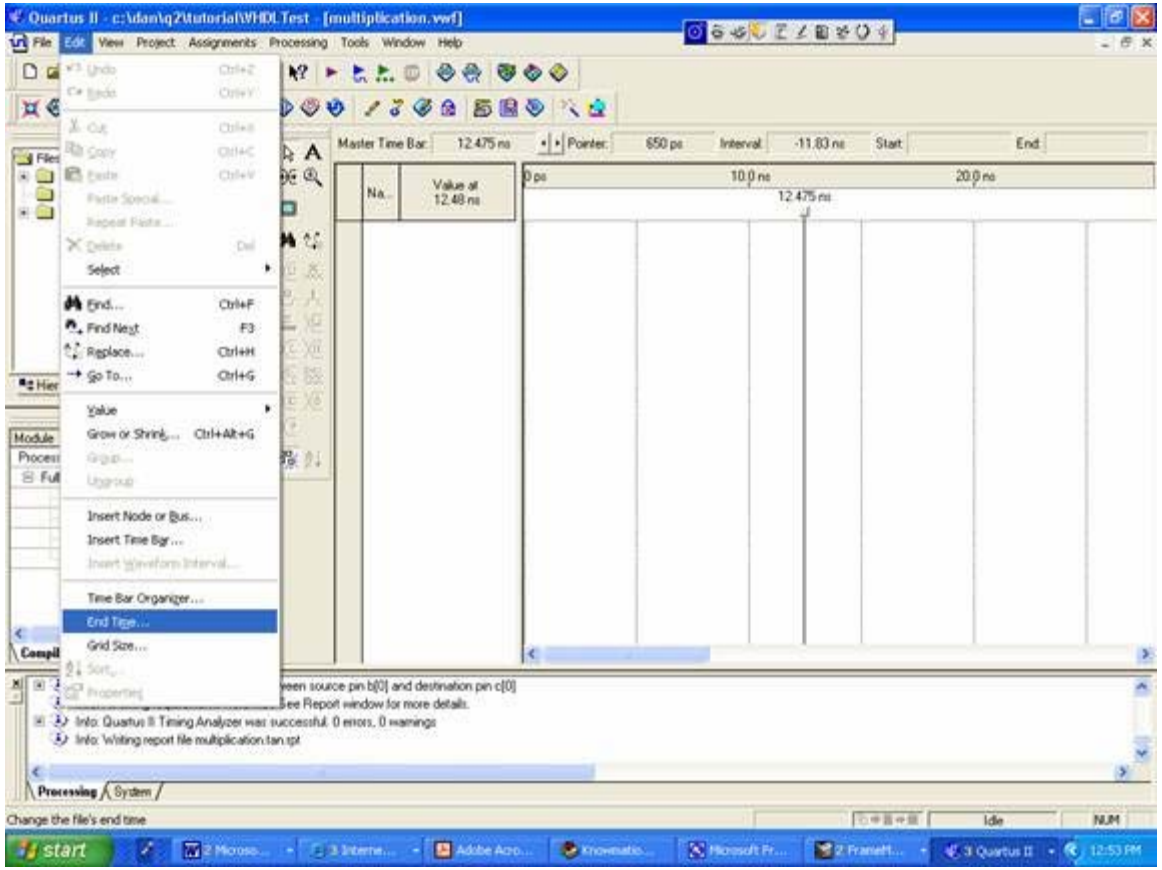


Simple Design Example: Simulation File



[File]->[Save As] Let the file name be the entity name and click [Save].

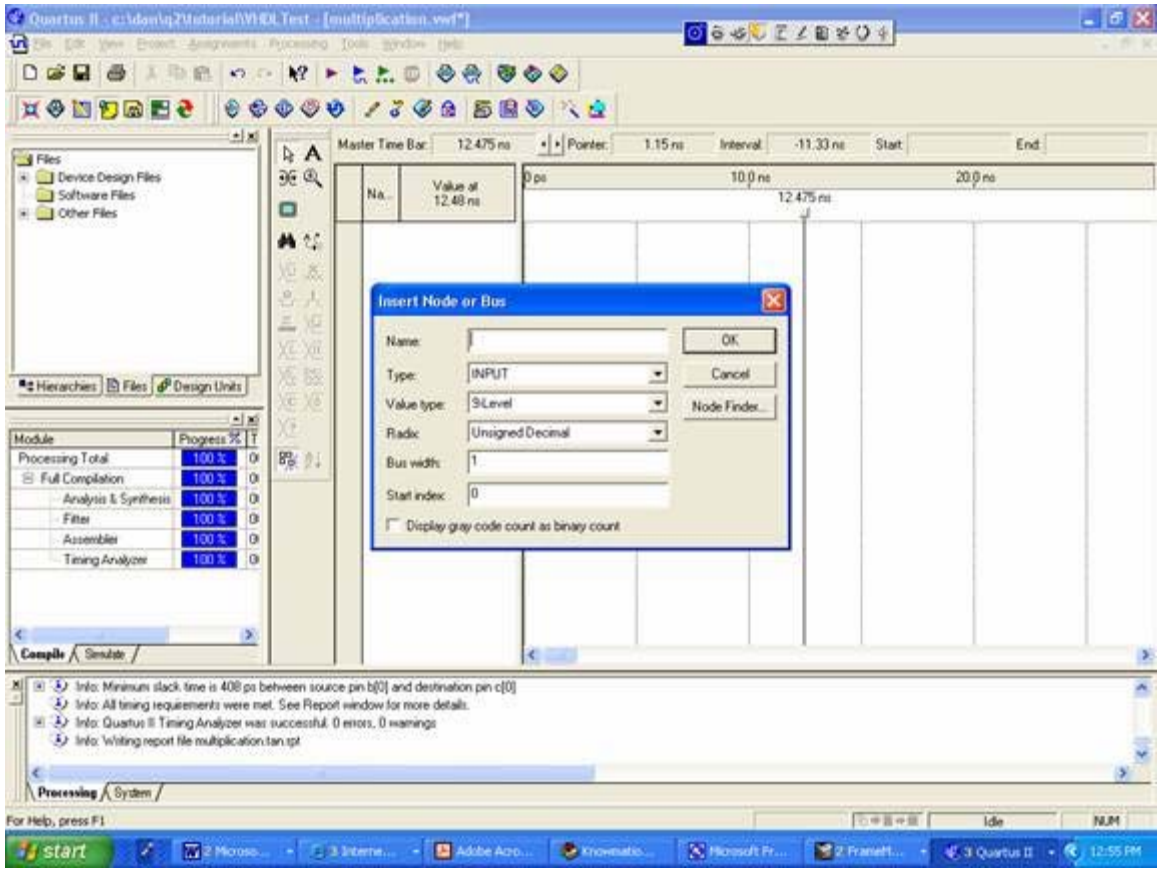
Simple Design Example: Simulations Time



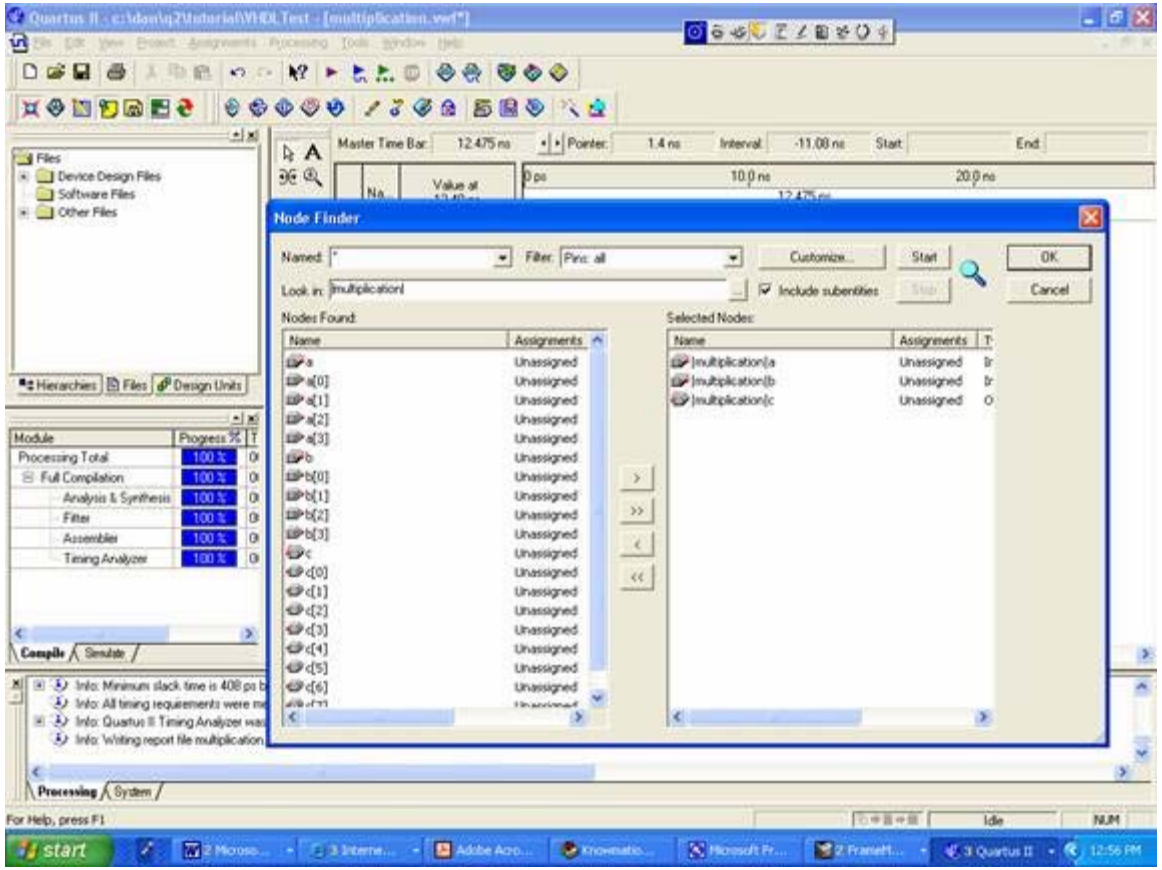
Click [Edit]->[End Time…] and type “500” ns.

Simple Design Example: Add Node for Simulation

Click [Edit]->[Insert Node or Bus]. Then click [Node Finder].

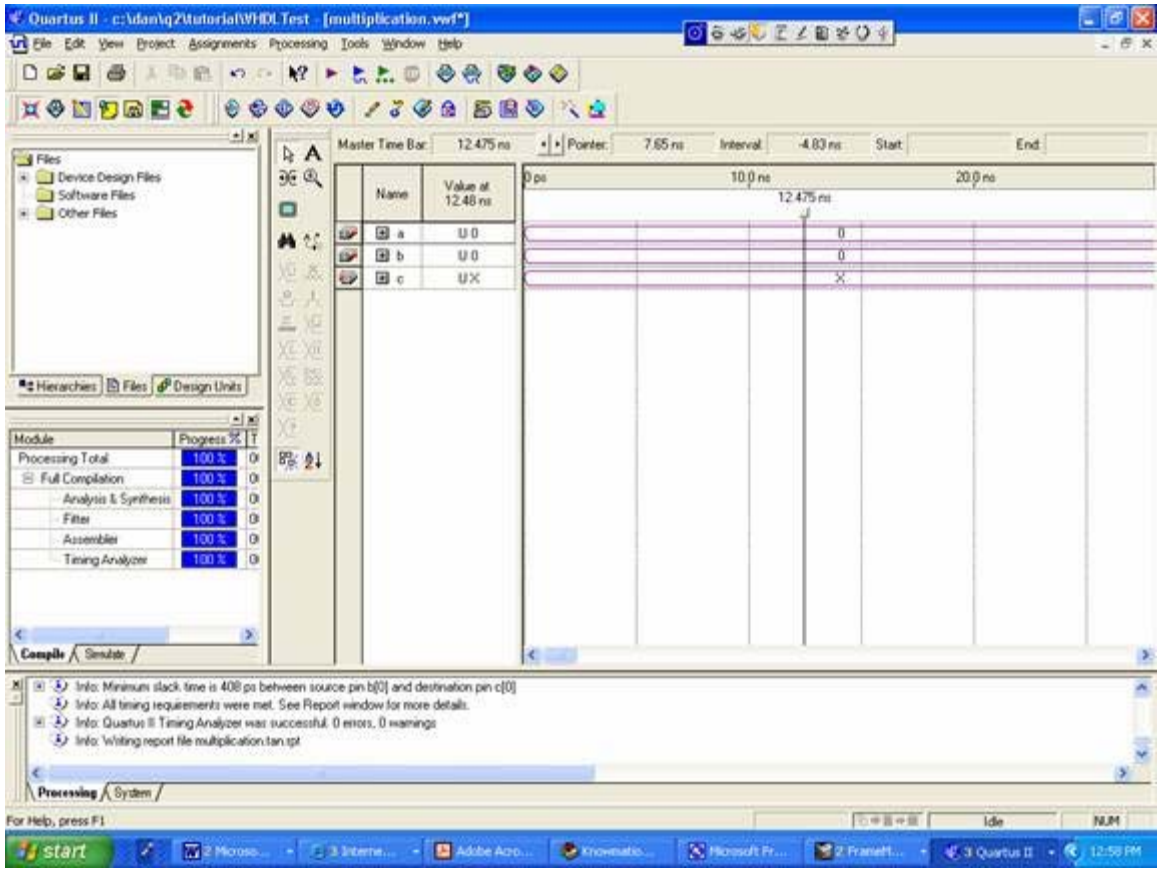


Simple Design Example: Find Node for Simulation



Click [Start] to find all the nodes defined in the entity (Click on List). Choose “x1” and click “>” to insert node “x1” to the vector waveform file. Repeat this procedure for node “x2”, “x3”, etc. Then click two [Ok]’s. Click “>>” to insert all.

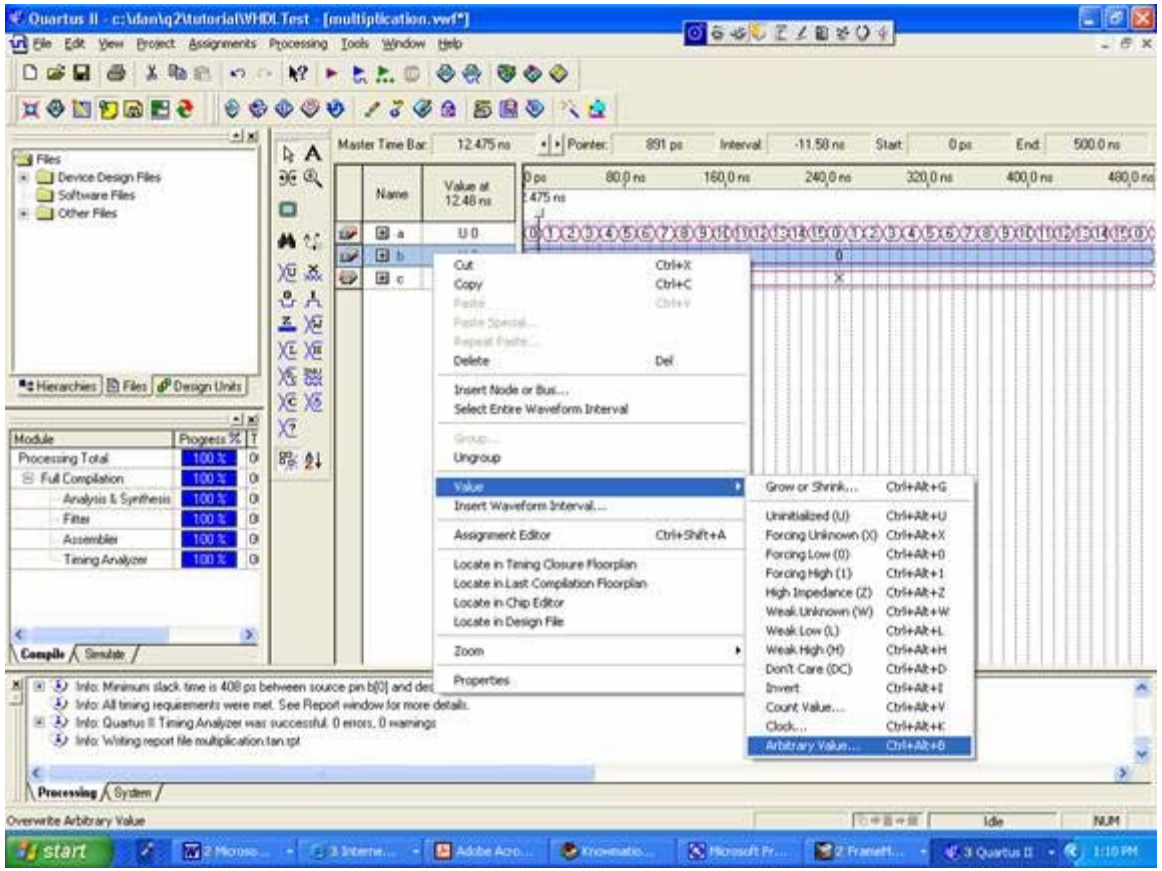
Simple Design Example: Nodes for Simulation



The input nodes and the output node are shown in the waveform.

Simple Design Example: Assign Signal Values

Right click on to select entire waveform. Then, Right Click for “value”



Simple Design Example: Functional Simulation

- Go to process and then start simulation.
- Assumed logic gates and gates are ideal with no delays.
- Just functional correctness of the circuit is verified.