CSCI 5330: Digital CMOS VLSI Design

Assignment 4, Dated: 17th February 2005 (Thu), Instructor: Dr. Saraju P. Mohanty
Due Date: 24th Feb 2005 (Thu)

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1. Problem 4.1 (page-266)
2. Problem 4.4 (page-266)
3. Draw the layout of the following gates using microwind and simulate them for correctness.
    a. Inverter
    b. NAND
    c. AND