CSCI 5330: Digital CMOS VLSI Design

Assignment 5, Dated: 1st Mar 2005 (Tue), Due Date: 8th Mar 2005 (Tue)
Instructor: Dr. Saraju P. Mohanty,

---

1. Problem 4.9 (page-266)
2. Problem 4.11 (page-267)
3. Draw the transistor level design of a full adder using DSCH and simulate it for functionality.
4. Draw the layout of the above using microwind and simulate it for correctness.