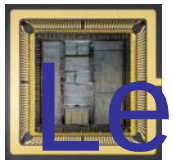
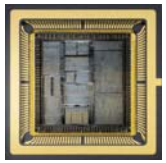


Lecture 11 : Circuit Simulation

CSCI 5330
Digital CMOS VLSI Design

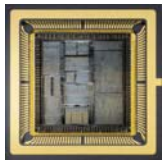
Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.



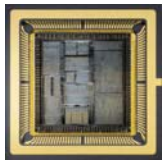
Outline

- Introduction to SPICE
- DC Analysis
- Transient Analysis
- Subcircuits
- Optimization
- Power Measurement
- Logical Effort Characterization



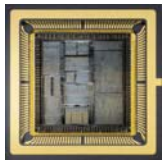
Simulators at Different Levels

- Simulators at different levels of abstraction :
  - Process
  - Circuit
  - Logic
- Process Simulator: Time and temperature effect on physical and electrical characteristics.
- Circuit Simulator: Use device model and netlist to predict current, voltage, and performance.
- Logic Simulator: Functional prediction of digital circuits for logical correctness.



Introduction to SPICE

- **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
  - Developed in 1970's at Berkeley
  - Many commercial versions are available
  - HSPICE is a robust industry standard
    - Has many enhancements that we will use
- The circuits elements are called cards, and complete description is called a SPICE deck.
- The file contains a netlist consisting of components and nodes, simulation options, analysis options, and device models.

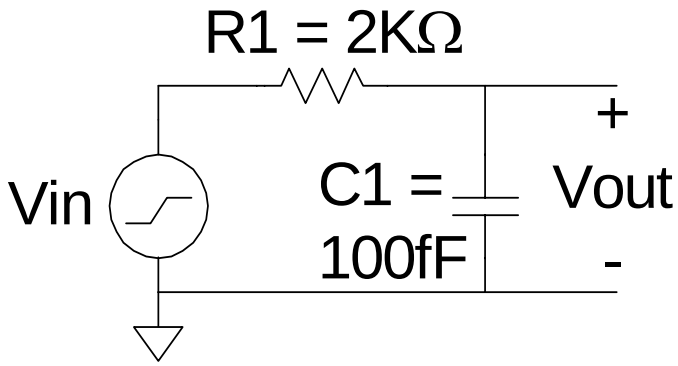


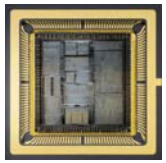
Writing Spice Decks

- Writing a SPICE deck is like writing a good program
  - Plan: sketch schematic on paper or in editor
    - Modify existing decks whenever possible
  - Code: strive for clarity
    - Start with name, email, date, purpose
    - Generously comment
  - Test:
    - Predict what results should be
    - Compare with actual
    - *Garbage In, Garbage Out!*

SPICE : RC Circuit Example

```
* rc.sp
* David_Harris@hmc.edu 2/2/03
* Find the response of RC circuit to rising input
*-----------------------------------------
* Parameters and models
*-----------------------------------------
.option post
*-----------------------------------------
* Simulation netlist
*-----------------------------------------
Vin     in      gnd     pwl     0ps 0 100ps 0 150ps 1.8 800ps 1.8
R1      in      out     2k
C1      out     gnd     100f
*-----------------------------------------
* Stimulus
*-----------------------------------------
.tran 20ps 800ps
.plot v(in) v(out)
.end
```



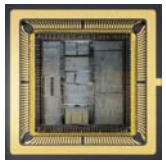


SPICE : RC Circuit Example …

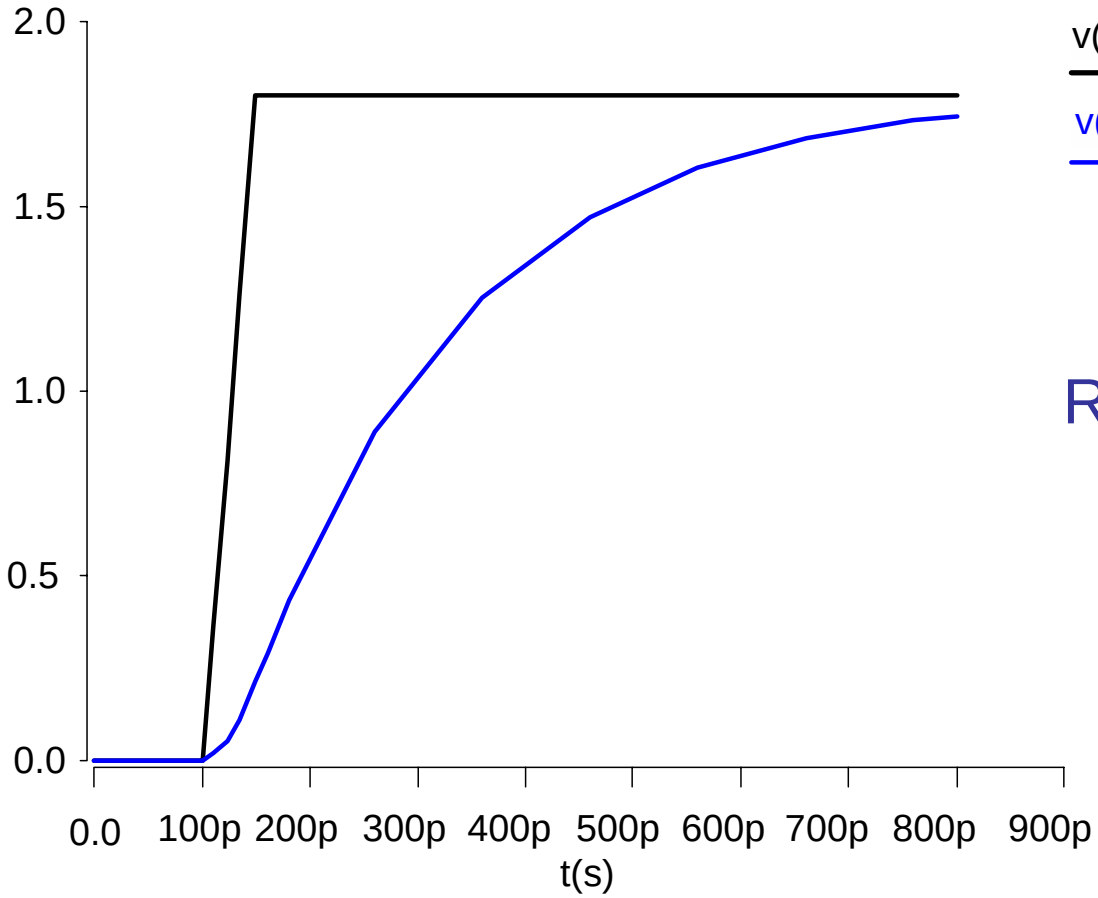
```
legend:
  a: v(in)
  b: v(out)

     time       v(in)
 (ab      )      0.          500.0000m       1.0000          1.5000          2.0000
                  +              +              +               +               +
   0.          0.     -2------+------+------+------+------+------+------+------+-
  20.0000p     0.      2       +      +      +      +      +      +      +      +
  40.0000p     0.      2       +      +      +      +      +      +      +      +
  60.0000p     0.      2       +      +      +      +      +      +      +      +
  80.0000p     0.      2       +      +      +      +      +      +      +      +
 100.0000p     0.      2       +      +      +      +      +      +      +      +
 120.0000p  720.000m +b       +      +     a+      +      +      +      +      +
 140.0000p    1.440   +   b   +      +      +      +      +    a +      +      +
 160.0000p    1.800   +      +b      +      +      +      +      +      +a     +
 180.0000p    1.800   +      +    b +      +      +      +      +      +a     +
 200.0000p    1.800  -+------+------+b-----+------+------+------+------+a-----+-
 220.0000p    1.800   +      +      +    b +      +      +      +      +a     +
 240.0000p    1.800   +      +      +     +b      +      +      +      +a     +
 260.0000p    1.800   +      +      +      +   b  +      +      +      +a     +
 280.0000p    1.800   +      +      +      +     b+      +      +      +a     +
 300.0000p    1.800   +      +      +      +      +b     +      +      +a     +
 320.0000p    1.800   +      +      +      +      +   b  +      +      +a     +
 340.0000p    1.800   +      +      +      +      +      b +      +      +a     +
 360.0000p    1.800   +      +      +      +      +      b      +      +a     +
 380.0000p    1.800   +      +      +      +      +      +b     +      +a     +
 400.0000p    1.800  -+------+------+------+------+------+------+--b---+------+a-----+-
 420.0000p    1.800   +      +      +      +      +      +    b  +      +      +a     +
 440.0000p    1.800   +      +      +      +      +      +     b +      +      +a     +
 460.0000p    1.800   +      +      +      +      +      +      b+      +      +a     +
 480.0000p    1.800   +      +      +      +      +      +       b      +      +a     +
 500.0000p    1.800   +      +      +      +      +      +       +b     +      +a     +
 520.0000p    1.800   +      +      +      +      +      +       +b     +      +a     +
 540.0000p    1.800   +      +      +      +      +      +       + b    +      +a     +
 560.0000p    1.800   +      +      +      +      +      +       +  b   +      +a     +
 580.0000p    1.800   +      +      +      +      +      +       +  b   +      +a     +
 600.0000p    1.800  -+------+------+------+------+------+------+------+---b--+a-----+-
 620.0000p    1.800   +      +      +      +      +      +      +    b  +a     +
 640.0000p    1.800   +      +      +      +      +      +      +     b +a     +
 660.0000p    1.800   +      +      +      +      +      +      +     b +a     +
 680.0000p    1.800   +      +      +      +      +      +      +     b +a     +
 700.0000p    1.800   +      +      +      +      +      +      +      b+a     +
 720.0000p    1.800   +      +      +      +      +      +      +      b+a     +
 740.0000p    1.800   +      +      +      +      +      +      +      b+a     +
 760.0000p    1.800   +      +      +      +      +      +      +      b+a     +
 780.0000p    1.800   +      +      +      +      +      +      +       ba     +
 800.0000p    1.800  -+------+------+------+------+------+------+------+------ba-----+-
                  +              +              +               +               +
```

Textual plot of RC circuit response

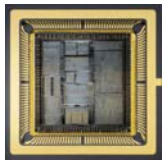
Result (Textual)



SPICE : RC Circuit Example …



Result (Graphical)



SPICE Sources

- DC Source

  Vdd vdd gnd 2.5

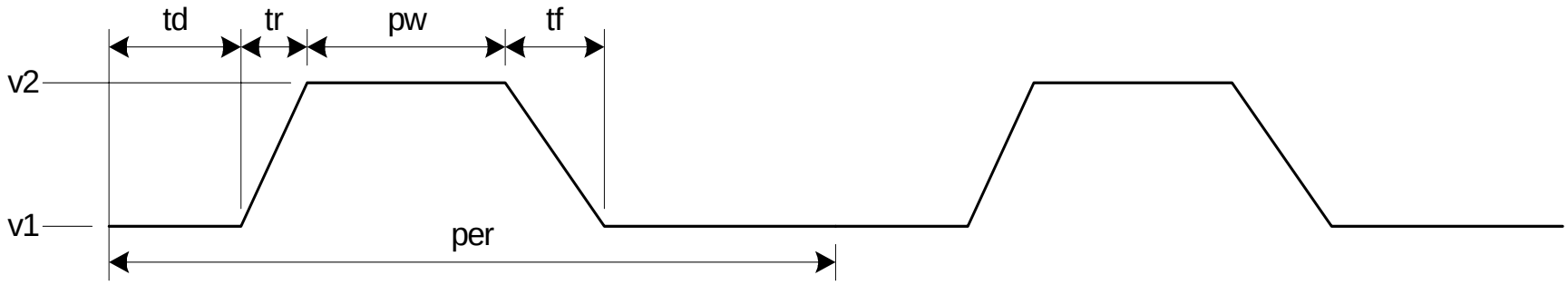
- Piecewise Linear Source

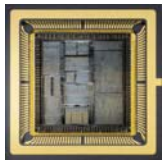
  Vin in gnd pwl 0ps 0 100ps 0 150ps 1.8 800ps 1.8

- Pulsed Source

  Vck clk gnd PULSE 0 1.8 0ps 100ps 100ps 300ps 800ps

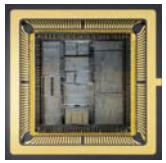
`PULSE v1 v2 td tr tf pw per`





SPICE Elements

Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source



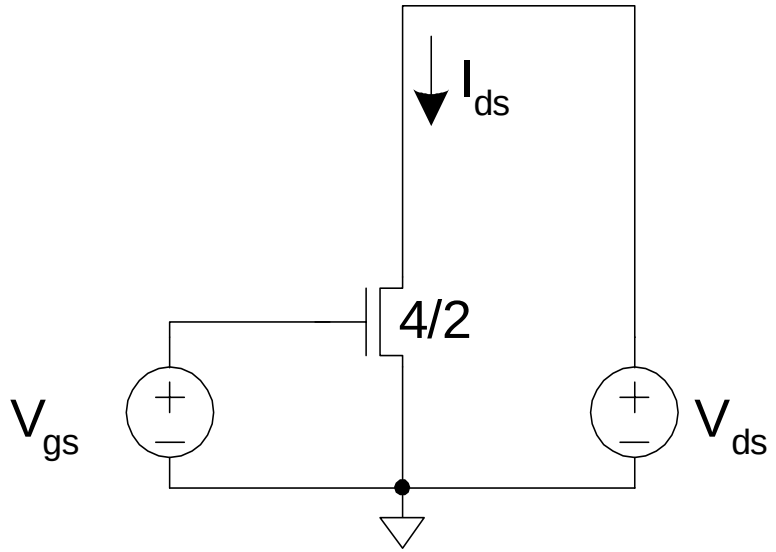
SPICE Units

Letter	Unit	Magnitude
a	atto	10^{-18}
f	fempto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
u	micro	10^{-6}
m	mili	10^{-3}
k	kilo	10^{3}
x	mega	10^{6}
g	giga	10^{9}

Ex: 100 femptofarad capacitor = 100fF, 100f, 100e-15

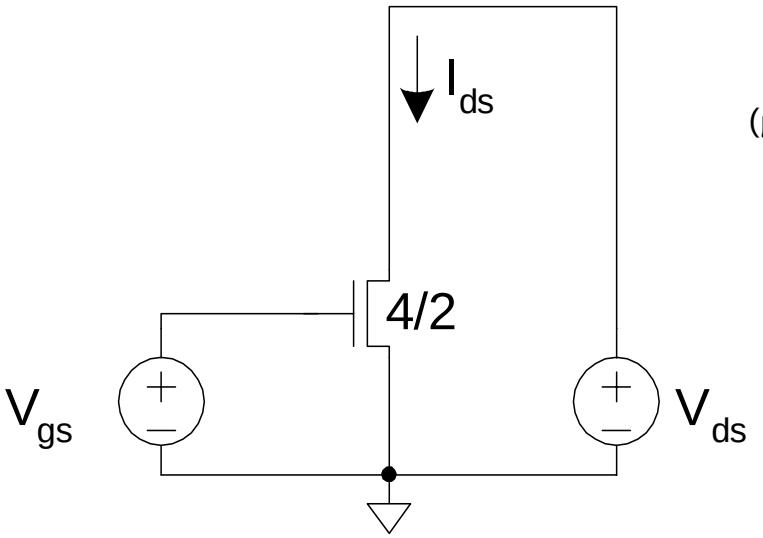
Transistor DC Analysis

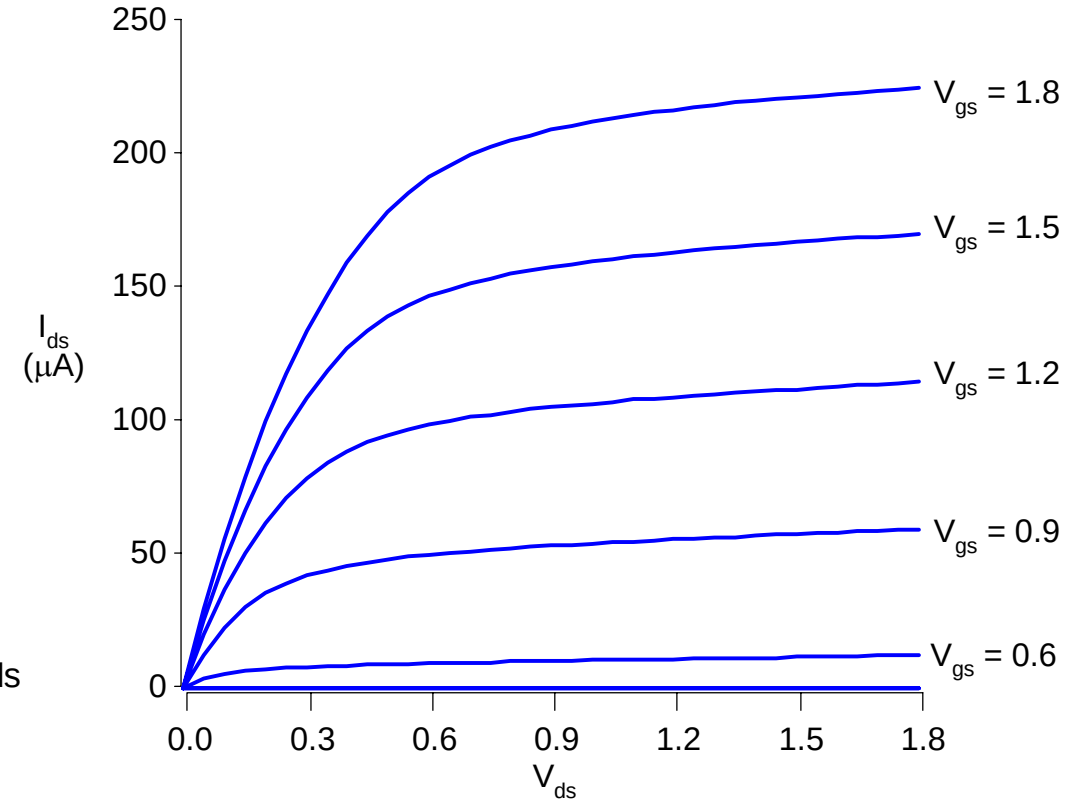
```
* mosiv.sp
*-----------------------------------------
* Parameters and models
*-----------------------------------------
.include '../models/tsmc180/models.sp'
.temp 70
.option post
*-----------------------------------------
* Simulation netlist
*-----------------------------------------
*nmos
Vgs     g       gnd     0
Vds     d       gnd     0
M1      d       g       gnd     gnd     NMOS  W=0.36u
        L=0.18u
*-----------------------------------------
* Stimulus
*-----------------------------------------
.dc Vds 0 1.8 0.05 SWEEP Vgs 0 1.8 0.3
.end
```



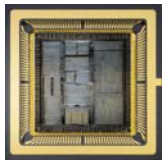
Transistor DC Analysis

- nMOS I-V
  - V_{gs} dependence
  - Saturation





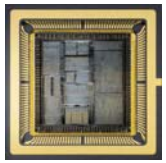
I-V characteristics



MOSFET Elements

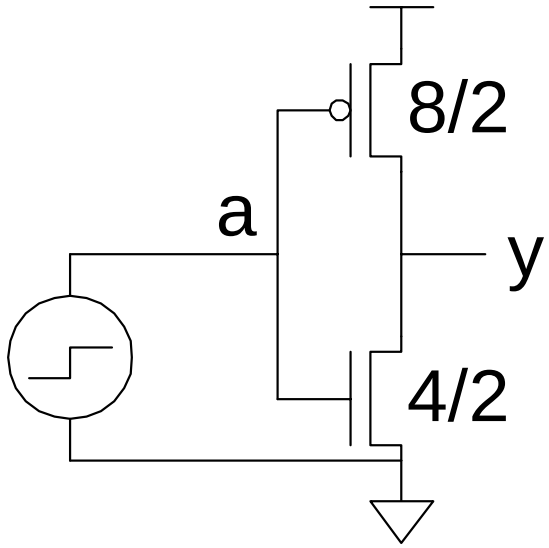
M element for MOSFET

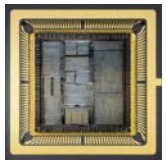
```
Mname drain gate source body type
+ W=<width> L=<length>
+ AS=<area source> AD = <area drain>
+ PS=<perimeter source> PD=<perimeter drain>
```



Inverter Transient Analysis

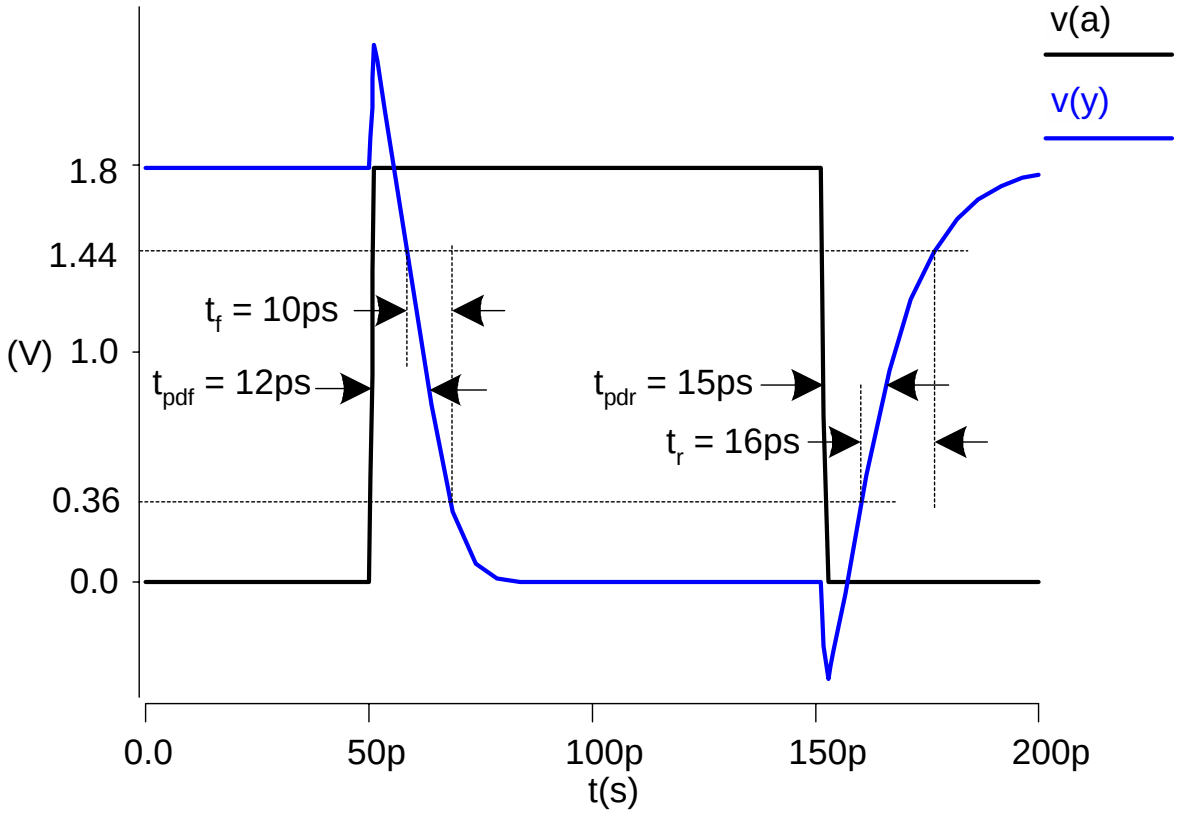
```
* inv.sp
* Parameters and models
*-----------------------------------------
.param SUPPLY=1.8
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post
* Simulation netlist
*-----------------------------------------
Vdd vdd gnd      'SUPPLY'
Vin a    gnd     PULSE 0 'SUPPLY' 50ps 0ps 0ps 100ps 200ps
M1      y        a       gnd     gnd     NMOS  W=4     L=2
+ AS=20 PS=18 AD=20 PD=18
M2      y        a       vdd     vdd     PMOS  W=8     L=2
+ AS=40 PS=26 AD=40 PD=26
* Stimulus
*-----------------------------------------
.tran 1ps 200ps
.end
```

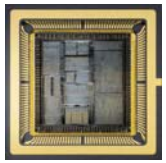




Inverter Transient Analysis ….

- Unloaded inverter
  - Overshoot
  - Very fast edges



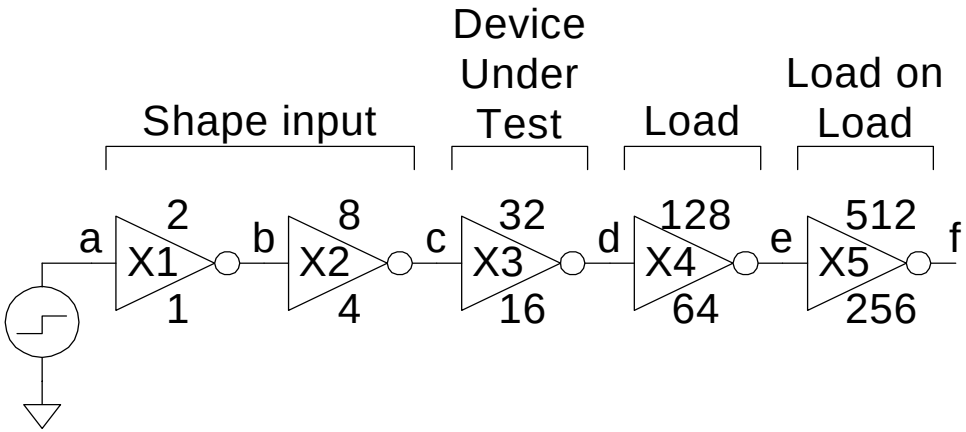


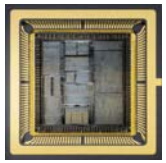
Subcircuits

- Declare common elements as subcircuits

```
.subckt inv a y N=4 P=8
M1 y a gnd gnd NMOS W='N' L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2 y a vdd vdd PMOS W='P' L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
```

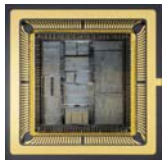
- Ex: Fanout-of-4 Inverter Delay
  - Reuse inv
  - Shaping
  - Loading





FO4 Inverter Delay

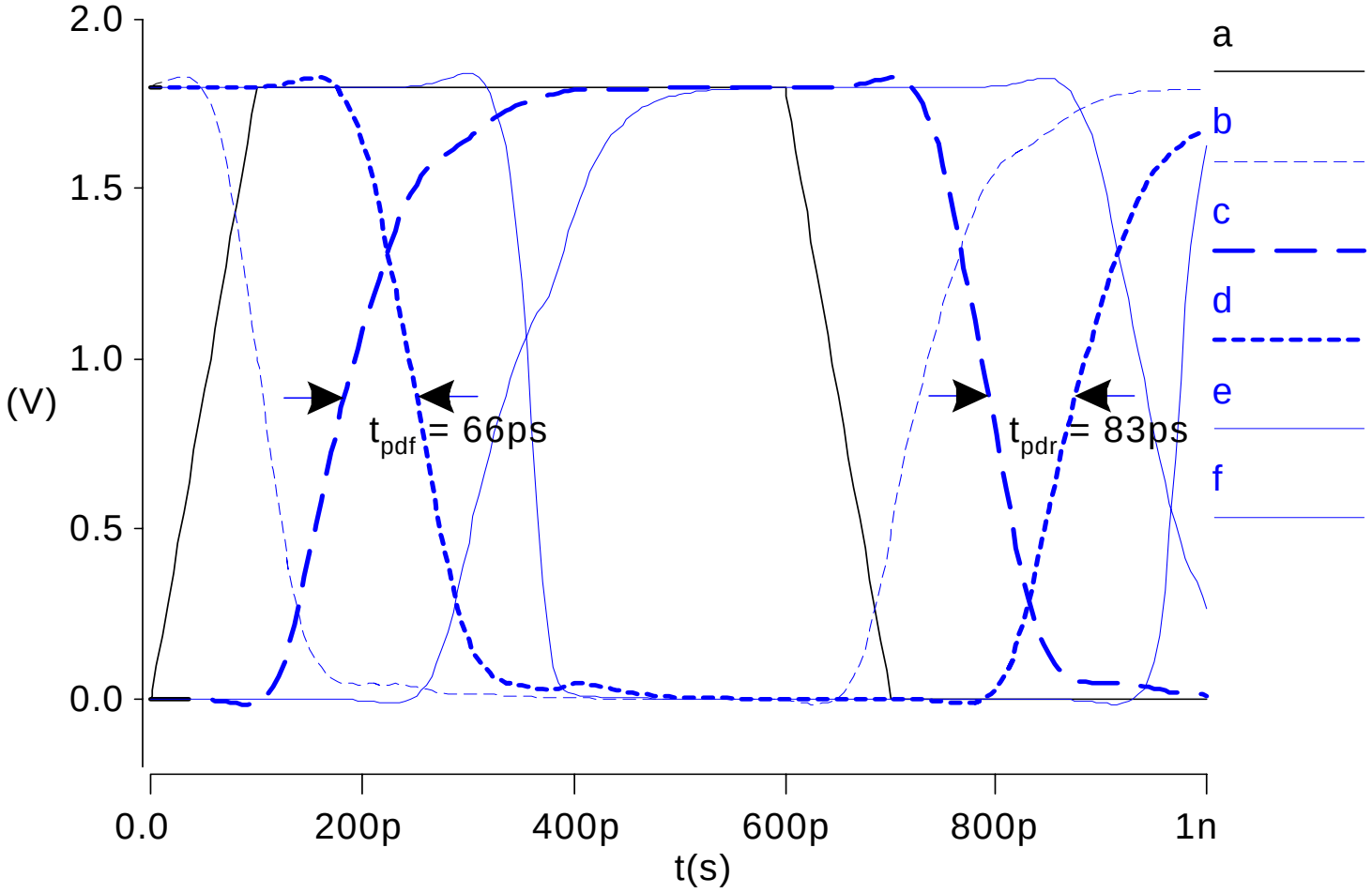
```
* fo4.sp
* Parameters and models
*-----------------------------------------------------------------
.param SUPPLY=1.8
.param H=4
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post
* Subcircuits
*-----------------------------------------------------------------
.global vdd gnd
.include '../lib/inv.sp'
* Simulation netlist
*-----------------------------------------------------------------
Vdd     vdd     gnd     'SUPPLY'
Vin  a  gnd     PULSE 0 'SUPPLY' 0ps 100ps 100ps 500ps 1000ps
X1      a       b       inv             * shape input waveform
X2      b       c       inv     M='H'   * reshape input waveform
.end
```

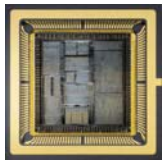


FO4 Inverter Delay ….

```
X3      c       d       inv     M='H**2' * device under test
X4      d       e       inv     M='H**3' * load
x5      e       f       inv     M='H**4' * load on load
* Stimulus
*-----------------------------------------------------------------
.tran 1ps 1000ps
.measure tpdr                                   * rising prop delay
+    TRIG v(c)   VAL='SUPPLY/2' FALL=1
+    TARG v(d)          VAL='SUPPLY/2' RISE=1
.measure tpdf                                   * falling prop delay
+    TRIG v(c)   VAL='SUPPLY/2' RISE=1
+    TARG v(d)          VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2'                      * average prop delay
.measure trise                                          * rise time
+       TRIG v(d)       VAL='0.2*SUPPLY' RISE=1
+       TARG v(d)       VAL='0.8*SUPPLY' RISE=1
.measure tfall                                          * fall time
+       TRIG v(d)       VAL='0.8*SUPPLY' FALL=1
+       TARG v(d)       VAL='0.2*SUPPLY' FALL=1
.end
```

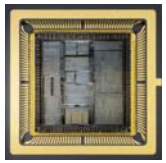
FO4 Inverter Delay ….





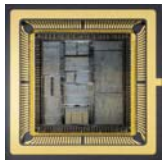
Optimization

- HSPICE can automatically adjust parameters
  - Seek value that optimizes some measurement
- Example: Best P/N ratio
  - We've assumed 2:1 gives equal rise/fall delays
  - But we see rise is actually slower than fall
  - What P/N ratio gives equal delays?
- Strategies
  - (1) run a bunch of sims with different P size
  - (2) let HSPICE optimizer do it for us



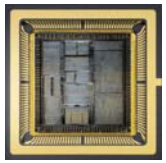
P/N Optimization

```
* fo4opt.sp
* Parameters and models
*-----------------------------------------------------------------
.param SUPPLY=1.8
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post
* Subcircuits
*-----------------------------------------------------------------
.global vdd gnd
.include '../lib/inv.sp'
* Simulation netlist
*-----------------------------------------------------------------
Vdd     vdd     gnd     'SUPPLY'
Vin     a       gnd     PULSE 0 'SUPPLY' 0ps 100ps 100ps 500ps
1000ps
X1      a       b       inv     P='P1'          * shape input
waveform
X2      b       c       inv     P='P1'  M=4     * reshape input
X3      c       d       inv     P='P1'  M=16    * device under test
```



P/N Optimization ….

```
X4      d       e       inv     P='P1'  M=64    * load
X5      e       f       inv     P='P1'  M=256   * load on load
* Optimization setup
*-----------------------------------------------------------------
.param P1=optrange(8,4,16)                  * search from 4 to 16, guess 8
.model optmod opt itropt=30                 * maximum of 30 iterations
.measure bestratio param='P1/4'                     * compute best P/N
ratio
* Stimulus
*-----------------------------------------------------------------
.tran 1ps 1000ps SWEEP OPTIMIZE=optrange RESULTS=diff
MODEL=optmod
.measure tpdr                                       * rising propagation delay
+       TRIG v(c) VAL='SUPPLY/2' FALL=1
+       TARG v(d)         VAL='SUPPLY/2' RISE=1
.measure tpdf                                       * falling propagation delay
+       TRIG v(c)         VAL='SUPPLY/2' RISE=1
+       TARG v(d)         VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2' goal=0           * average prop delay
.measure diff param='tpdr-tpdf' goal = 0  * diff between delays
.end
```

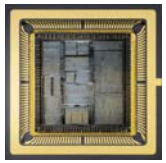


P/N Optimization ….

- P/N ratio for equal delay is 3.6:1
  - $t_{pd} = t_{pdr} = t_{pdf} = 84$ ps (slower than 2:1 ratio)
  - Big pMOS transistors waste power too
  - Seldom design for exactly equal delays
- What ratio gives lowest average delay?

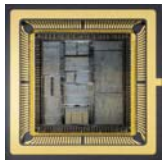
```
.tran 1ps 1000ps SWEEP OPTIMIZE=optrange RESULTS=tpd
   MODEL=optmod
```

  - P/N ratio of 1.4:1
  - $t_{pdr} = 87$ ps, $t_{pdf} = 59$ ps, $t_{pd} = 73$ ps



Device Models

- SPICE uses wide variety of transistor models with different trade-offs between complexity and accuracy.
- Different models:
  - Level 1 (simple)
  - Level 2 (simple)
  - Level 3 (simple)
  - BSIM 1 (Berkley Short-Channel IGFET Model)
  - BSIM 2 (very elaborate)
  - BSIM 3 (very elaborate)
  - BSIM 4 (current, most elaborate)

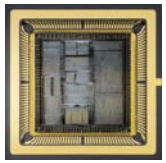


Device Models : Level 1

- Closely related to the Shockley model
- Enhanced with channel length modulation and the body effect.
- The parameters from the SPICE model are in CAPS.
- The threshold voltage is modulation by the source-to-body voltage (V_{sb}) due to body effect is taken into account.
- Gate capacitance is calculated from the oxide thickness TOX.

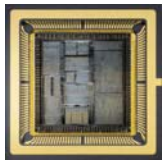
```
.model NMOS NMOS (LEVEL=1 TOX=40e-10 KP=155E-6 LAMBDA=0.2
+                 VTO=0.4 PHI=0.93 GAMMA=0.6
+                 CJ=9.8E-5 PB=0.72 MJ=0.36
+                 CJSW=2.2E-10 PHP=7.5 MJSW=0.1)
```

Sample Level 1 MODEL card



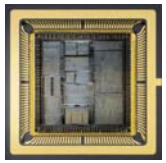
Device Models : Level 2 and Level 3

- Account effects of :
  - Velocity Saturation
  - Mobility Degradation
  - Subthrehold Conduction
  - Drain-Induced Barrier Lowering
- Still not good enough to mimic the characteristics of the modern devices.



Device Models : BSIM

- Features of version 3v3:
  - Continuous and differentiable I-V characteristics for different regions of operation for good convergence.
  - Sensitivity of V_t, etc to length and width
  - V_t model include body effect and DIBL.
  - Velocity saturation, mobility degradation, etc.
  - Multiple gate capacitance
  - Diffusion capacitance and resistance models
- Features of version 4:
  - Tunneling current
  - High-K dielectric

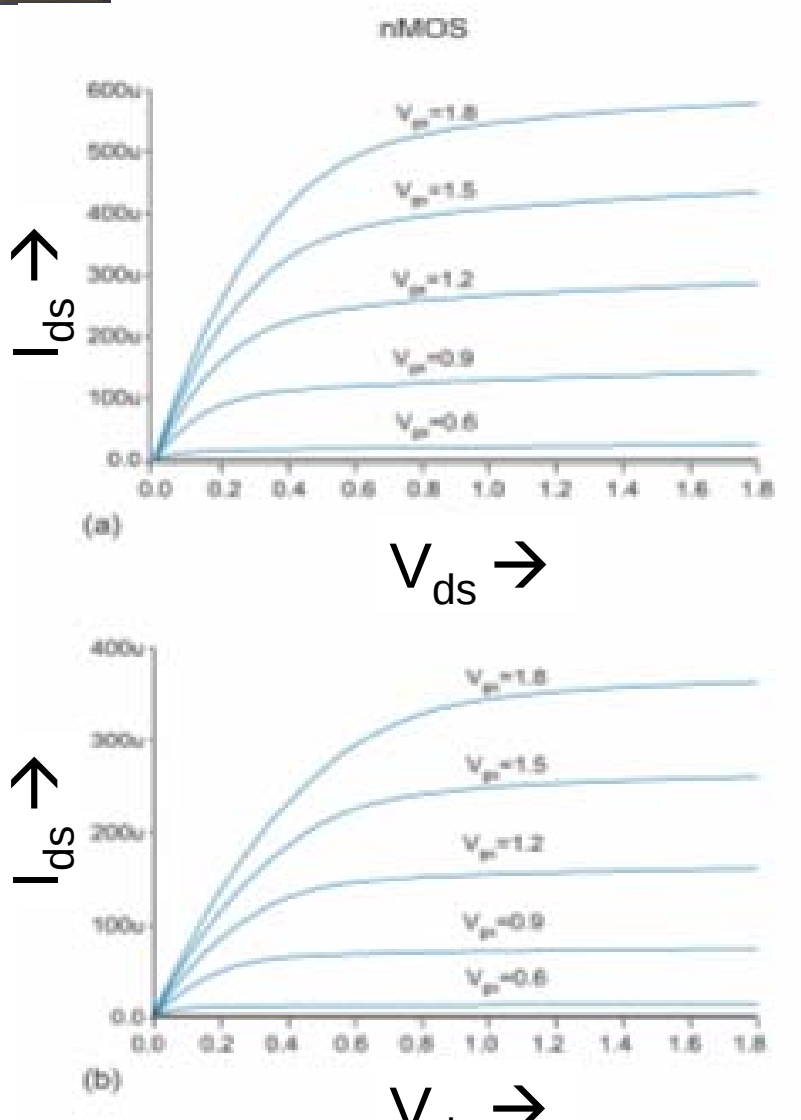


Design Corners

```
* corner.sp
* Step response of unloaded inverter across process corners

*---------------------------------------------------------------------------
* Parameters and models
*---------------------------------------------------------------------------
.option scale=90n
.param SUP=1.8 * Must set before calling .lib
.lib '../models/tsmc180/opconditions.lib' TT
.option post

*---------------------------------------------------------------------------
* Simulation netlist
*---------------------------------------------------------------------------
Vdd   vdd   gnd   'SUPPLY'
Vin   a     gnd   PULSE    0 'SUPPLY' 200ps 0ps 0ps 500ps 1000ps
M1    y     a     gnd      gnd     NMOS   W=4   L=2
+ AS=20 PS=18 AD=20 PD=18
M2    y     a     vdd      vdd     PMOS   W=8   L=2
+ AS=40 PS=26 AD=40 PD=26

*---------------------------------------------------------------------------
* Stimulus
*---------------------------------------------------------------------------
.tran 1ps 1000ps
.alter
.lib '../models/tsmc180/opconditions.lib' FF
.alter
.lib '../models/tsmc180/opconditions.lib' SS
.end
```

CORNER SPICE deck

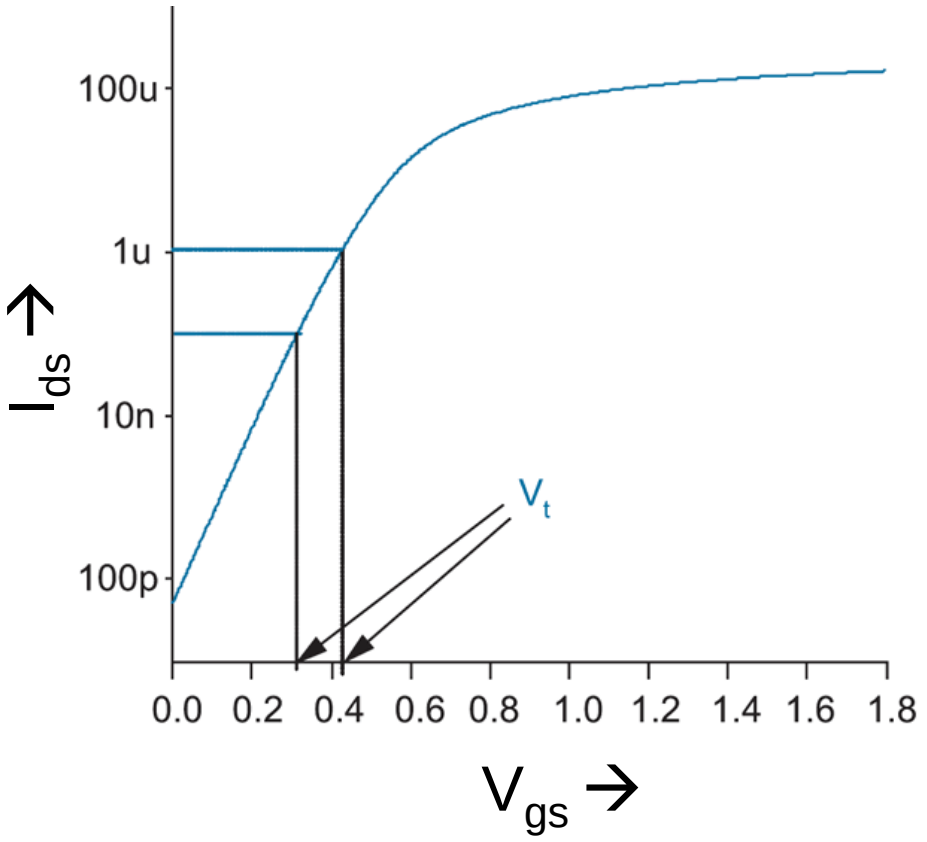
Device Characterization : I-V characteristics



180nm process, V_{dd} = 1.8V, W = 1000nm, 70°C

360nm process, V_{dd} = 1.8V, W = 1000nm, 70°C

Device Characterization : V_t



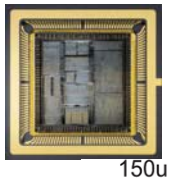
Constant current threshold voltage extraction method

Two methods to determine V_t from I_{ds}-V_{gs} characteristics:

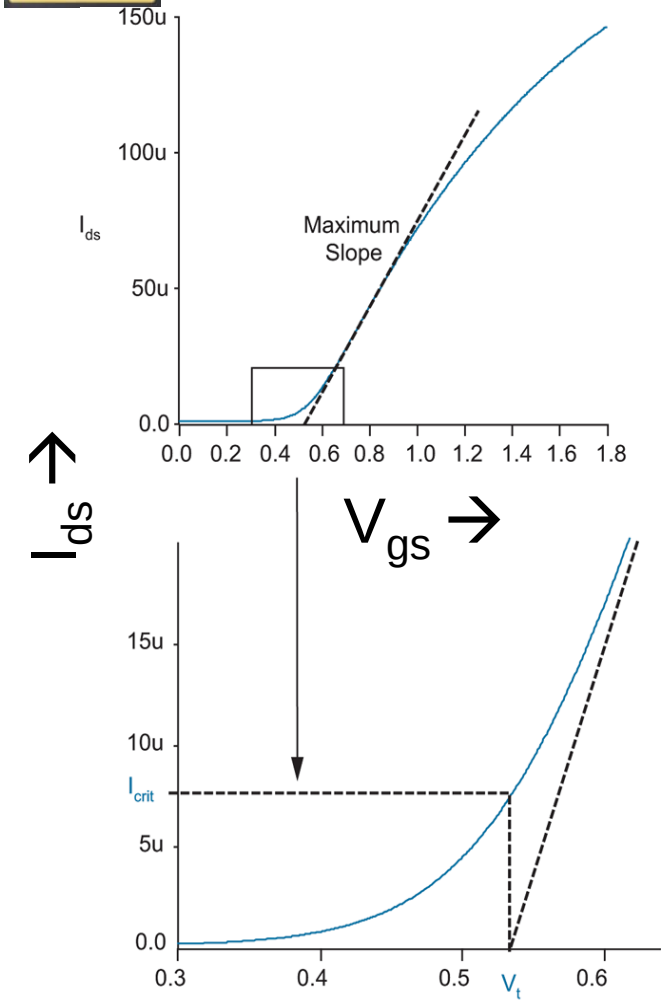
- Constant Current
- Linear Extrapolation

Constant Current:

- V_t is defined as the gate voltage at a given drain current.
- Depends on an arbitrary choice of a drain current.



Device Characterization : V_t



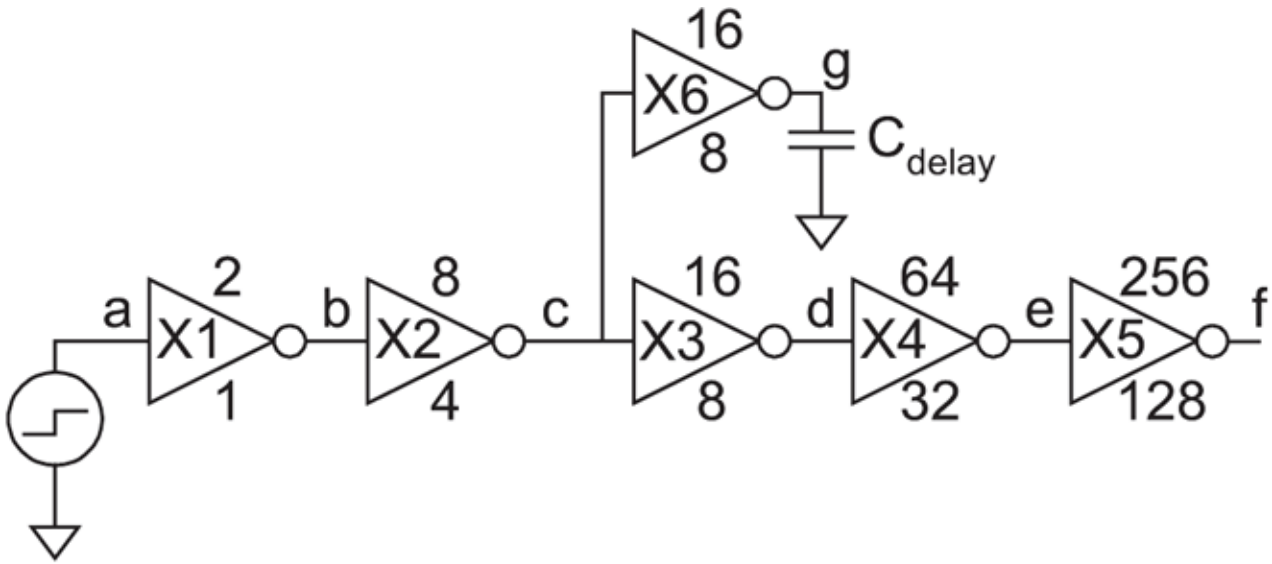
Linear extrapolation threshold voltage extraction method

Linear Extrapolation:

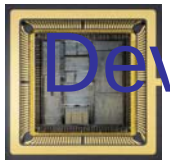
- Extrapolates the gate voltage from the point of maximum slope on I_{ds}-V_{gs} characteristics.
- Valid for linear region of operation only.

Device Characterization : Gate Capacitance

- Effective gate capacitance is needed to estimate the delay (RC).



Circuit for extracting effective gate capacitance for delay estimation

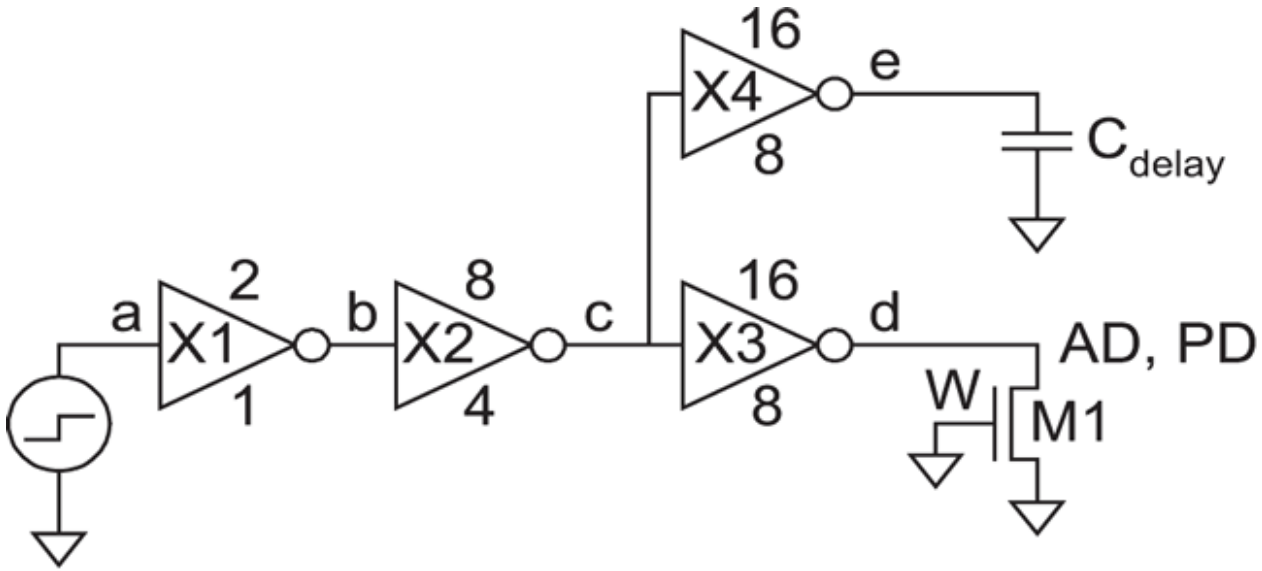


Device Characterization : Gate Capacitance

```
* capdelay.hsp
* Extract effective gate capacitance for delay estimation.
*-------------------------------------------------------------------------
* Parameters and models
*-------------------------------------------------------------------------
.option scale=90n
.param SUP=1.8 * Must set before calling .lib
.lib '../models/tsmc180/opconditions.lib' TT
.option post
*-------------------------------------------------------------------------
* Subcircuits
*-------------------------------------------------------------------------
.global  vdd   gnd
.subckt  inv   a     y
M1       y     a     gnd   gnd   NMOS   W=16 L=2 AD=0 AS=0 PD=0 PS=0
M2       y     a     vdd   vdd   PMOS   W=32 L=2 AD=0 AS=0 PD=0 PS=0
.ends
*-------------------------------------------------------------------------
* Simulation netlist
*-------------------------------------------------------------------------
Vdd      vdd   gnd   'SUPPLY'      * SUPPLY is set by .lib call
Vin      a     gnd   pulse 0 'SUPPLY' 1ns 0.5ns 0.5ns 4ns 10ns
X1       a     b     inv           * set appropriate slope
X2       b     c     inv   M=4     * set appropriate slope
X3       c     d     inv   M=8     * drive real load
X4       d     e     inv   M=32    * real load
X5       e     f     inv   M=128   * load on load (important!)
X6       c     g     inv   M=8     * drive linear capacitor
cdelay   g     gnd   'CperMicron*32*(16+32)*90n/1u' * linear capacitor
*-------------------------------------------------------------------------
* Optimization setup
*-------------------------------------------------------------------------
.measure errorR param='invR - capR' goal=0
.measure errorF param='invF - capF' goal=0
.param CperMicron=optrange(2f, 1f, 3.0f)
.model optmod opt itropt=30
.measure CperMic param = 'CperMicron'
*-------------------------------------------------------------------------
* Stimulus
*-------------------------------------------------------------------------
.tran .1ns 12ns SWEEP OPTIMIZE = optrange RESULTS=errorR,errorF MODEL=optmod
.measure invR
+       TRIG v(c)  VAL='SUPPLY/2' FALL=1
+       TARG v(d)  VAL='SUPPLY/2' RISE=1
.measure  capR
+       TRIG v(c)  VAL='SUPPLY/2' FALL=1
+       TARG v(g)  VAL='SUPPLY/2' RISE=1
.measure invF
+       TRIG v(c)  VAL='SUPPLY/2' RISE=1
+       TARG v(d)  VAL='SUPPLY/2' FALL=1
.measure  capF
+       TRIG v(c)  VAL='SUPPLY/2' RISE=1
+       TARG v(g)  VAL='SUPPLY/2' FALL=1
.end
```

CAPDELAY SPICE deck

Device Characterization : Parasitic Capacitance

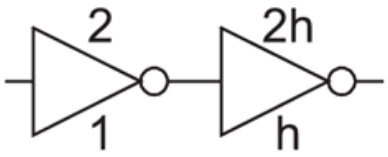


Circuit for extracting effective parasitic capacitance for delay estimation

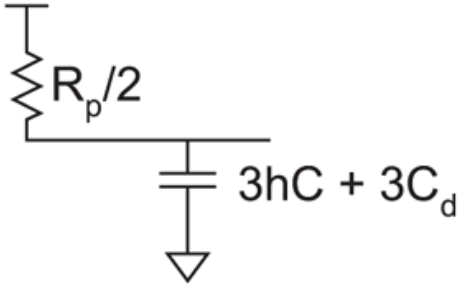
- Diffusion capacitance is voltage dependent
- Effective gate capacitance is obtained as average over switching transition.

Device Characterization : Effective Resistance

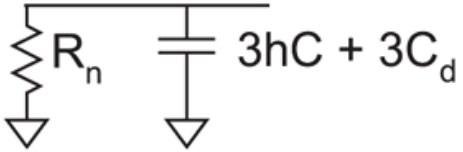
$$t_{pdr} = \frac{R_p}{2}(3hC + 3C_d) \qquad t_{pdf} = R_n(3hC + 3C_d)$$



(a) Fanout-of-h inverter

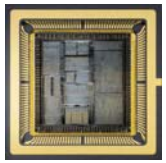


(b) Rising delay



(c) Falling delay

- RC delay model: Unit transistor has capacitance C, parasitic resistance C_d, resistance R_n for NMOS, resistance R_p for PMOS.
- As C is known from effective capacitance extraction, R_n the and R_p values can be know once delays are measured.



Circuit Characterization : Power

- HSPICE can measure power
  - Instantaneous P(t)
  - Or average P over some interval

  .print $P(v_{dd})$

  .measure pwr AVG $P(v_{dd})$ FROM=0ns TO=10ns

- Power in single gate
  - Connect to separate V_{DD} supply
  - Be careful about input power

Circuit Characterization : Monte Carlo Simulation

- Used to find the effect of random variations on a circuit.
- Consists of running simulation repeatedly with different randomly chosen parameters.
- Transistor models must include the offset parameters.

```
 .model NMOS NMOS (LEVEL=1 TOX=40e-10 KP=155E-6 LAMBDA=0.2
+                 VTO='0.4+dvthn' PHI=0.93 GAMMA=0.6
+                 CJ=9.8E-5 PB=0.72 MJ=0.36
+                 CJSW=2.2E-10 PHP=7.5 MJSW=0.1
+                 XL='dxl' XW='dxw')
```

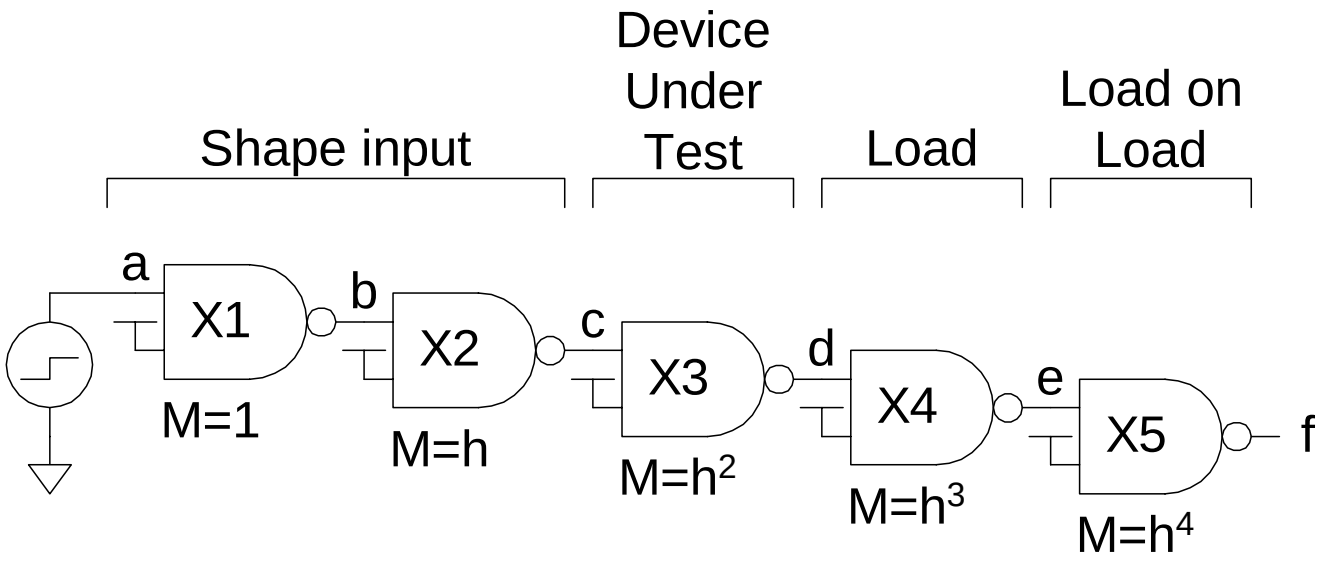
Sample Level 1 MODEL card with offsets

```
.param dxl=aunif(0,12.5nm) dvthn=agauss(0,16.8m,1) dvthp=agauss(0,14.6m,1)
.tran 1ps 1000ps SWEEP MONTE=30
```

Monte Carlo transient analysis

Circuit Characterization : Logical Effort

- Logical effort can be measured from simulation
  - As with FO4 inverter, shape input, load output



Circuit Characterization : Logical Effort

- Plot t_{pd} vs. h
  - Normalize by τ
  - y-intercept is parasitic delay
  - Slope is logical effort
- Delay fits straight line very well in any process as long as input slope is consistent

τ = 15 ps