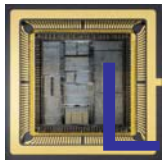
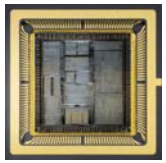


Lecture 12 : Circuit Families

CSCI 5330
Digital CMOS VLSI Design

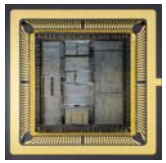
Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.



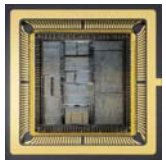
Outline

- Pseudo-nMOS Logic
- Dynamic Logic
- Pass Transistor Logic



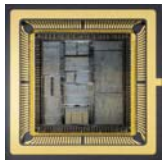
Introduction

- Usual case: Static CMOS gates using complementary NMOS and PMOS
- Alternative CMOS logic configurations are called logic families.
- What family to be used? Depending on the application, use the family that needs least design effort and least logical effort.
- Most common alternatives of SCMOS:
  - ratioed circuits
  - Dynamic circuits
  - Pass-transistor circuits



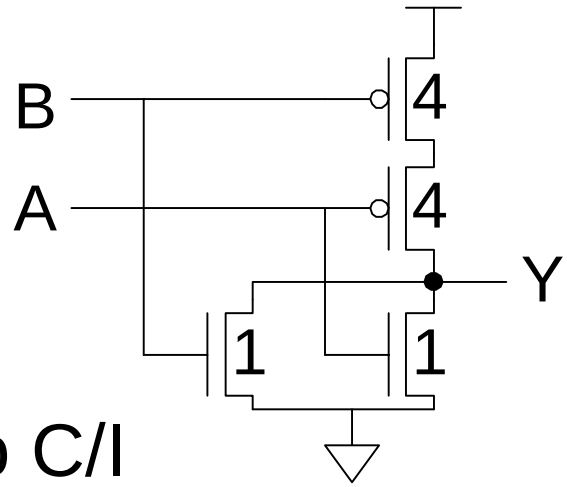
Static CMOS Circuit

- Advantages of static CMOS circuit:
  - Good noise margin
  - Fast operation
  - Low power
  - Insensitive to device variation
  - Easy to design
  - Widely supported by existing CAD tools
  - Readily available as various cell libraries



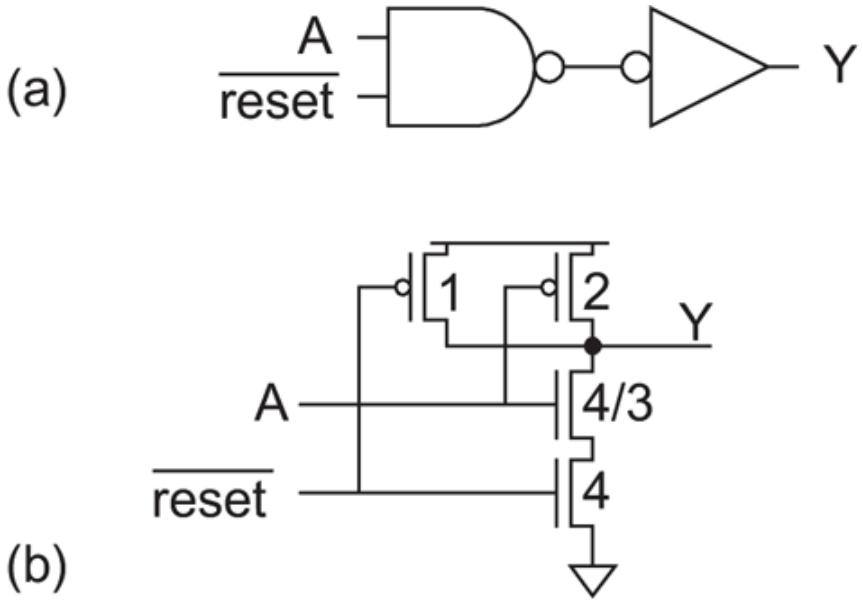
Static CMOS Circuit

- What makes a circuit fast?
  - $I = C\,dV/dt \rightarrow t_{pd} \propto (C/I)\,\Delta V$
  - low capacitance
  - high current
  - small swing



- Logical effort is proportional to C/I
- Static CMOS have large logical effort and high voltage swing $0 \leftrightarrow V_{dd}$.
- PMOS are the enemy!
  - High capacitance for a given current
- Can we take the PMOS capacitance off the input? Various circuit families try to do this…

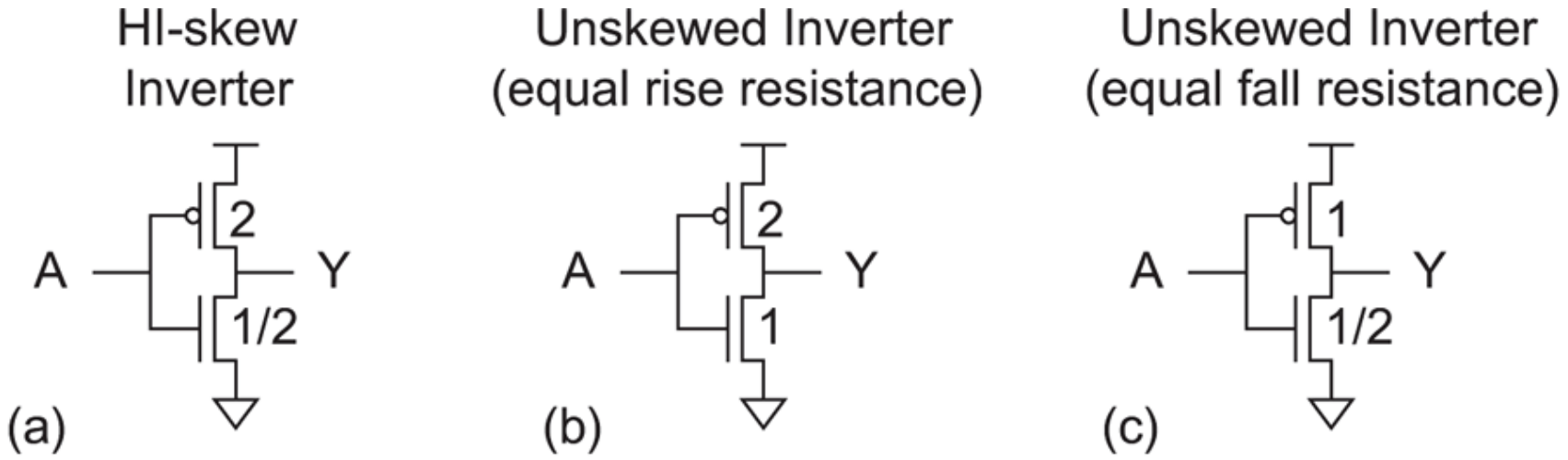
Static CMOS Circuit : Asymmetric Gates



Resettable buffer optimized for data input

- When one I/P is less critical than another.
- Circuit should be optimized for I/P-O/P delay at the expensed of reset.
- This reduces the diffusion capacitance and parasitic delay at the expense of slower response to reset.

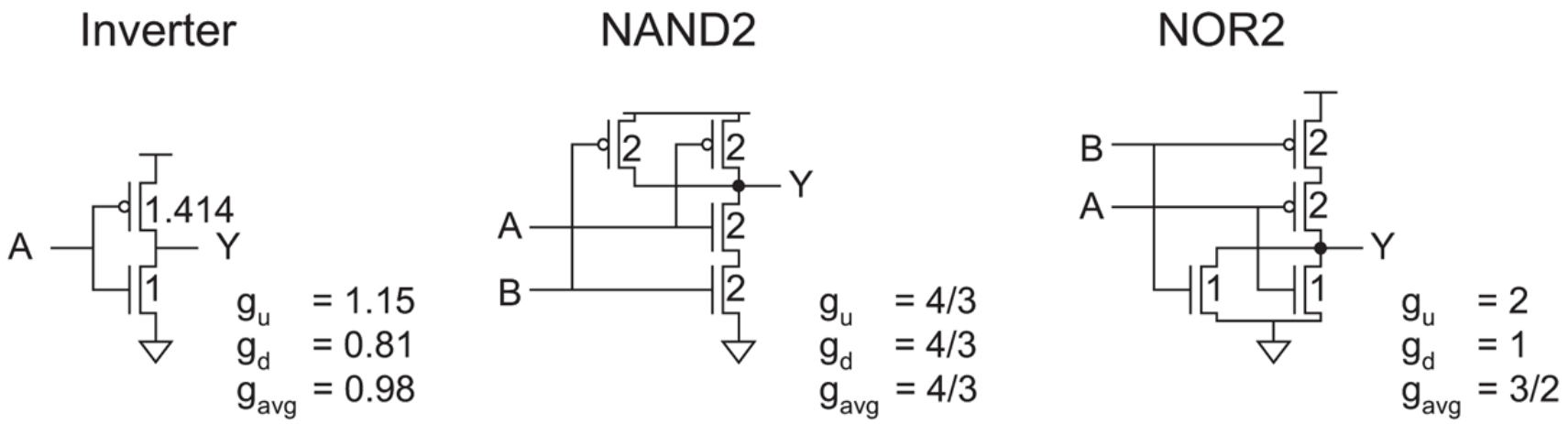
Static CMOS Circuit : Skewed Gates



Logical effort calculation for HI-skew inverter

- When one I/P transitions is more important than other
- HI-skew: favor the rising output transitions
- LO-skew: favor the falling output transitions

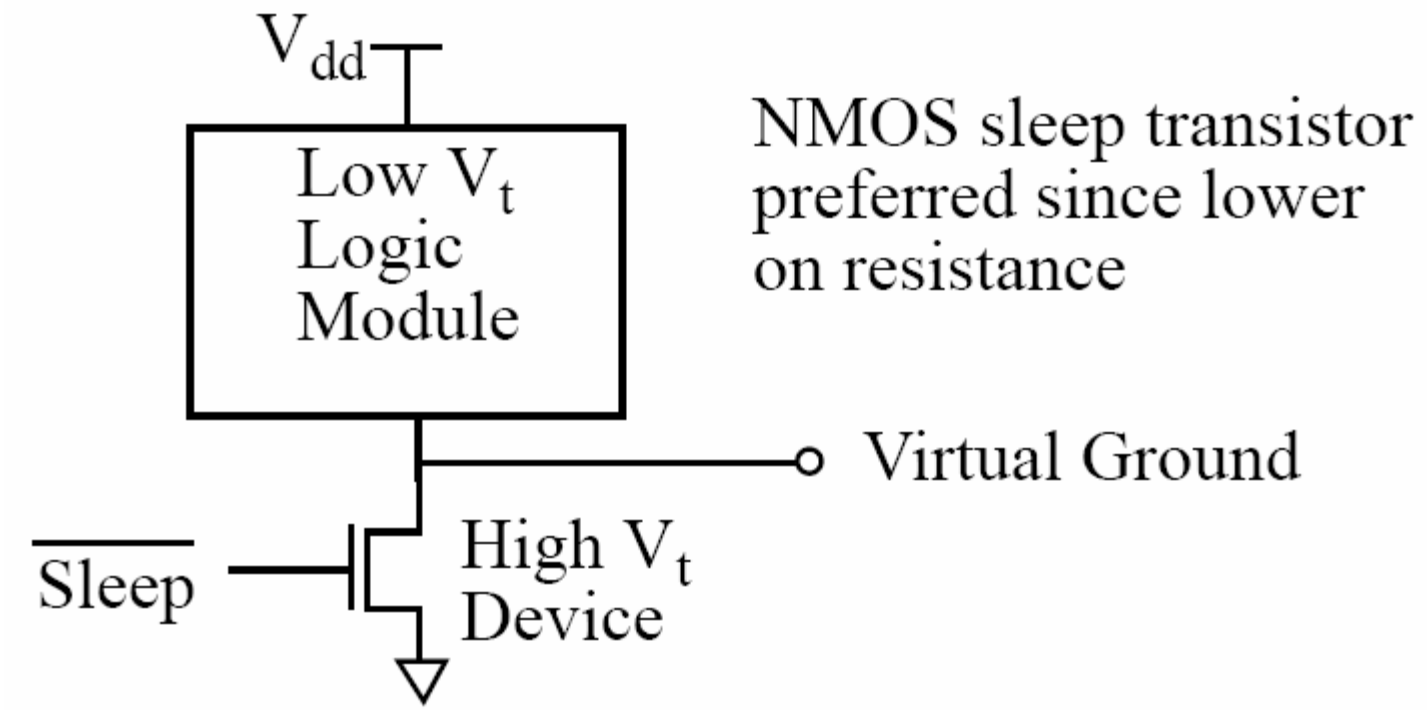
Static CMOS Circuit : P/N Ratios



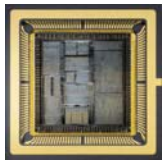
Gates with *P/N* ratios giving least delay

- P/N ratio of library cells should be chosen on the basis of area, power, and reliability, not average delay.
- For a NOR gate, reducing size of the PMOS significantly improves both the delay and area.

Static CMOS Circuit : MTCMOS



- MOS with lower V_T produces more ON current but also leaky exponentially more OFF current.
- Low VT are faster and may be used in critical path of a circuit.

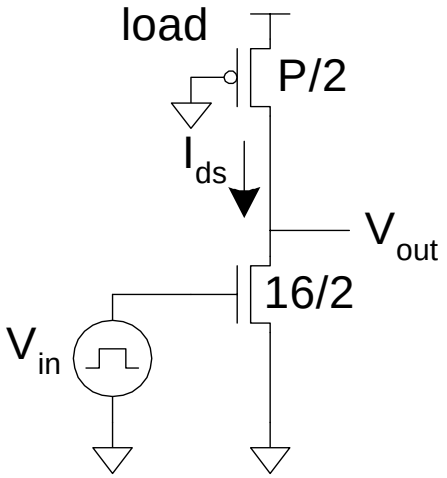


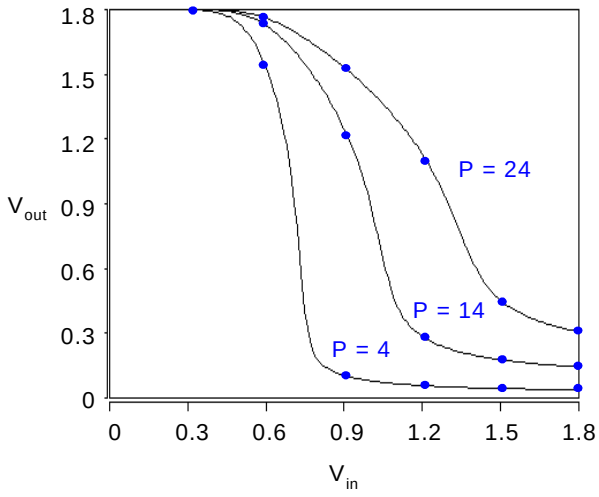
Ratioed Circuits

- Use weak pull-up devices and stronger pull-down devices.
- I/P capacitance improves, and logical effort improves, but depends on ratio of pull-up and pull-down strength.
- Strong pull-up : V_{OLmax} is too high
- Weak pull-up : slow rising delay
- Dissipate more static power.

Ratioed Circuits : Pseudo-NMOS

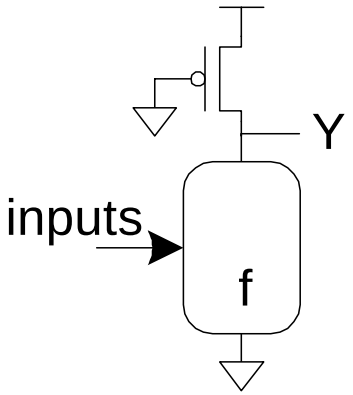
- In the old days, NMOS processes had no PMOS
  - Instead, use pull-up transistor that is always ON
- In CMOS, use a PMOS that is always ON
  - Ratio issue
  - Make PMOS about ¼ effective strength of pulldown network



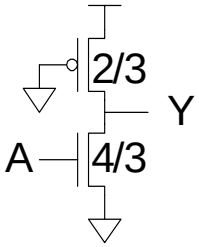


Ratioed Circuits : Pseudo-NMOS Gates

- Design for unit current on output to compare with unit inverter.
- pMOS fights nMOS

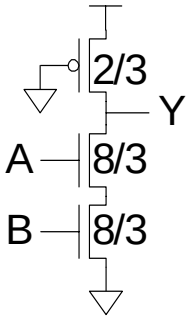


Inverter



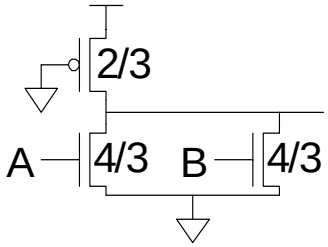
$g_u = 4/3$
$g_d = 4/9$
$g_{avg} = 8/9$
$p_u = 6/3$
$p_d = 6/9$
$p_{avg} = 12/9$

NAND2



$g_u = 8/3$
$g_d = 8/9$
$g_{avg} = 16/9$
$p_u = 10/3$
$p_d = 10/9$
$p_{avg} = 20/9$

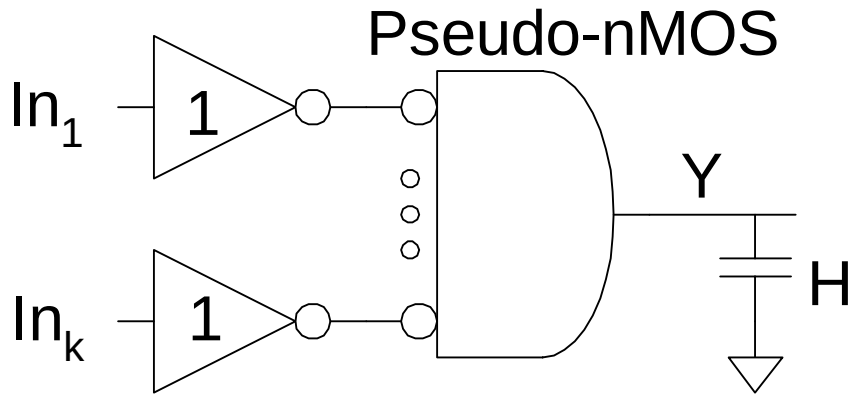
NOR2



$g_u = 4/3$
$g_d = 4/9$
$g_{avg} = 8/9$
$p_u = 10/3$
$p_d = 10/9$
$p_{avg} = 20/9$

Ratioed Circuits : Pseudo-NMOS Design

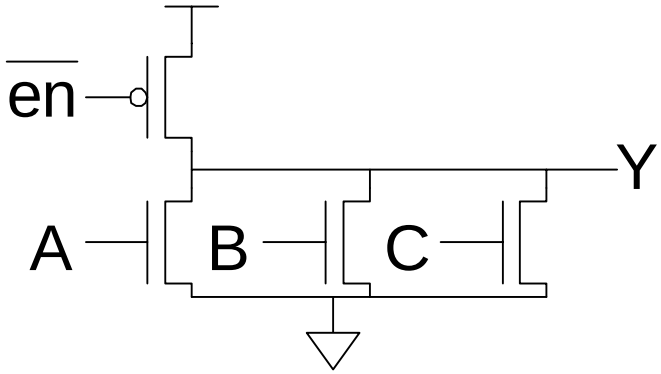
- Ex: Design a k-input AND gate using pseudo-nMOS. Estimate the delay driving a fanout of H



- G = 1 * 8/9 = 8/9
- F = GBH = 8H/9
- P = 1 + (4+8k)/9 = (8k+13)/9
- N = 2
- $D = NF^{1/N} + P = \frac{4\sqrt{2H}}{3} + \frac{8k+13}{9}$

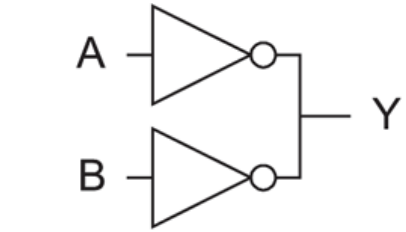
Ratioed Circuits : Pseudo-NMOS Power

- Pseudo-NMOS draws power whenever Y = 0
  - Called static power $P = I \bullet V_{DD}$
  - A few mA / gate * 1M gates would be a problem
  - This is why NMOS went extinct!
- Use pseudo-NMOS sparingly for wide NORs
- Turn off PMOS when not in use

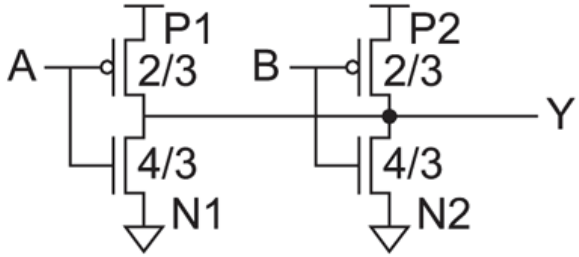


Ratioed Circuits : Ganged CMOS

- Pair of inverters ganged together and the pair computes NOR function.
- When 01 or 10 : acts pseudo-NMOS circuit
- When 00 : both PMOS are ON in parallel pulling the O/P high much faster
- When 11 : both PMOS are OFF reducing static power consumption



(a)



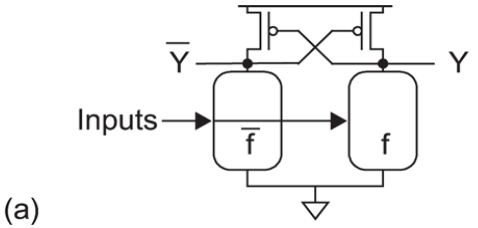
(b)

$g_u = 1$
$g_d = 2/3$
$g_{avg} = 5/6$

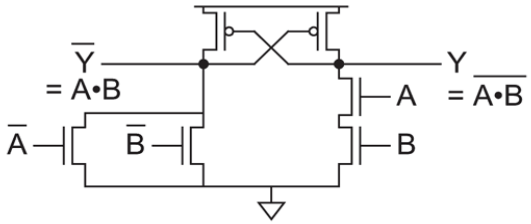
Symmetric 2-input NOR gate

Cascode Voltage Switch Logic (CVSL)

- Performance as good as ratioed circuits, but reduced static power consumption.
- Uses both true and complementary I/P signals and computes both true and complementary.
- For any given pattern: One of the pull-down network will be ON and other will be OFF.

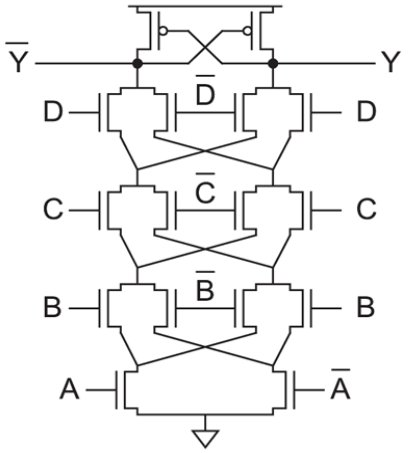


(a)



(b)

AND/NAND gate

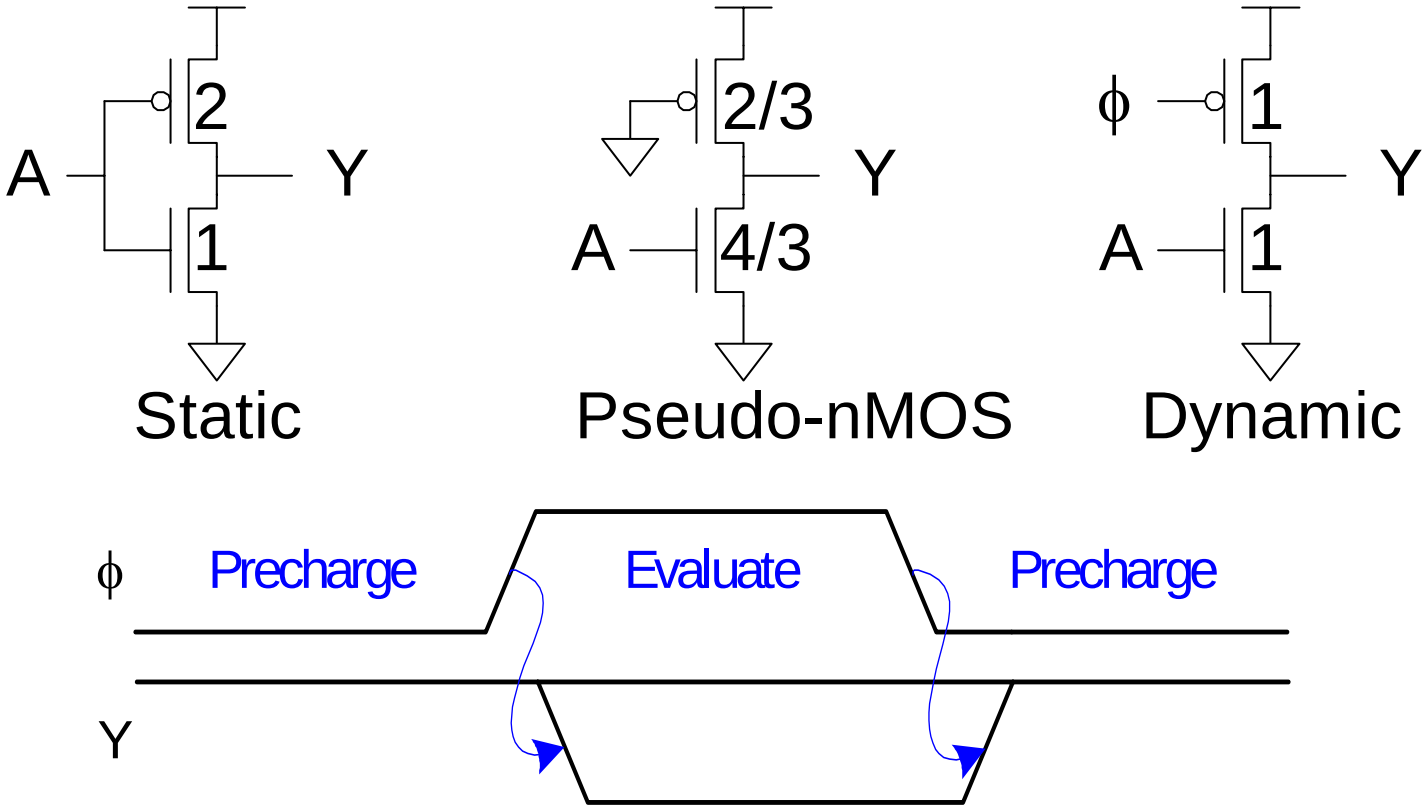


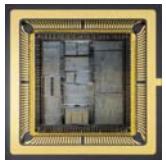
(c)

4-input XOR gate

Dynamic Circuit

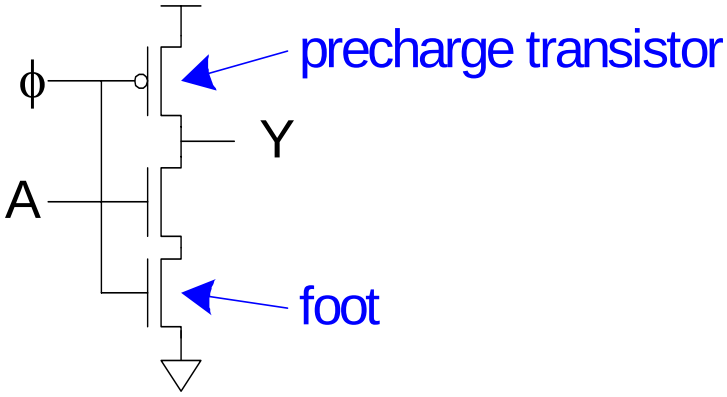
- Dynamic gates uses a clocked pMOS pullup
- Two modes: precharge and evaluate



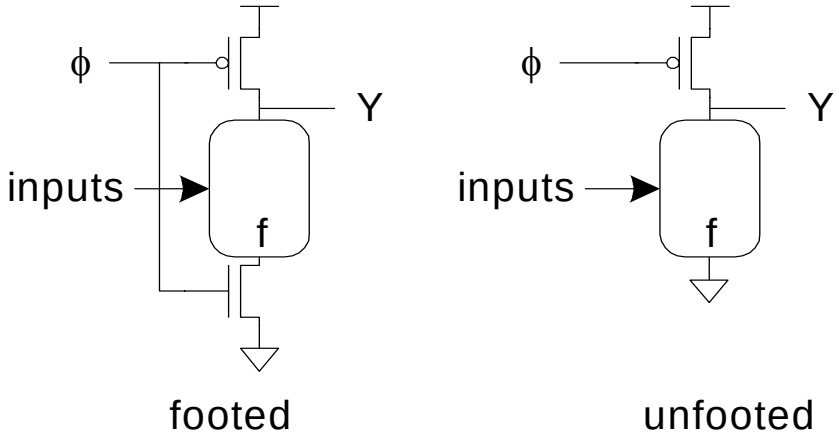


Dynamic Circuit : Footed

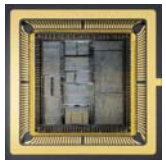
- What if pulldown network is ON during precharge?
- Use series evaluation transistor to prevent fight.



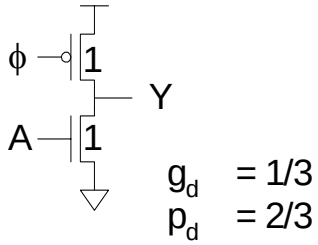
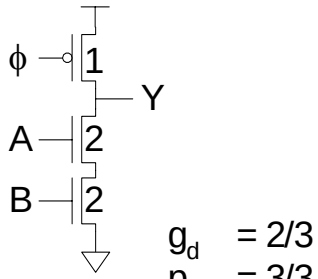
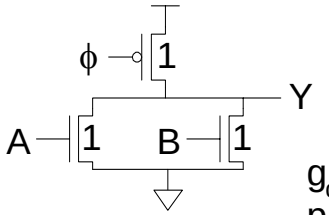
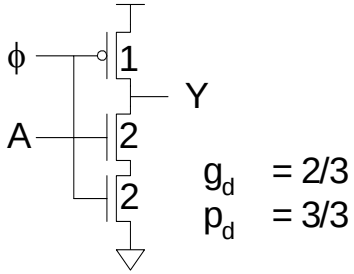
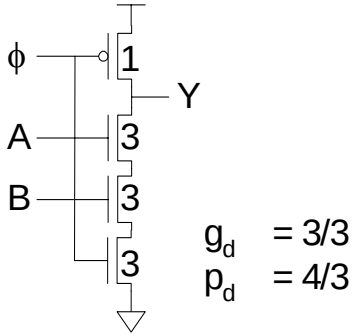
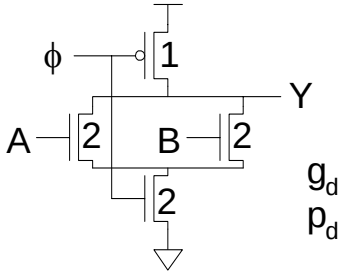
Footed dynamic inverter



Generalized Footed/Unfooted dynamic gates



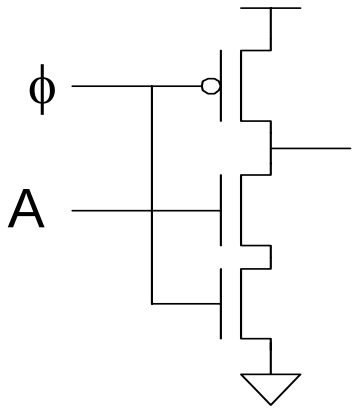
Dynamic Circuit : Logical Effort

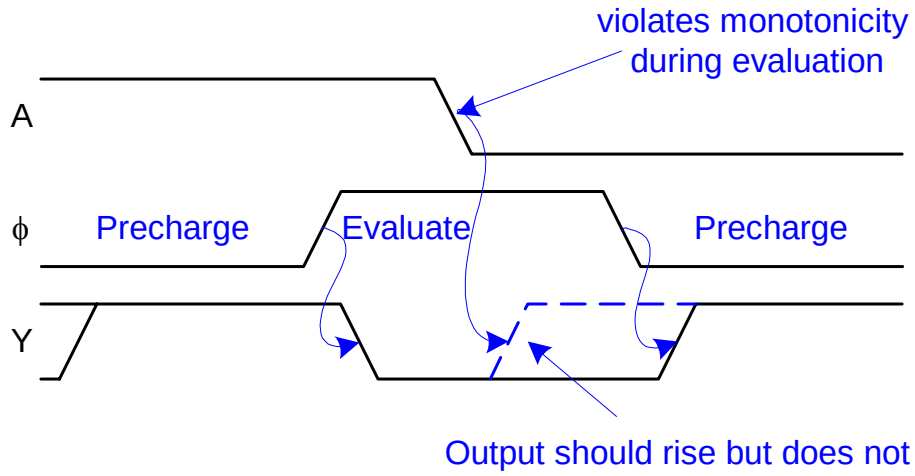
	Inverter	NAND2	NOR2
unfooted	 $g_d = 1/3$ $p_d = 2/3$	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 1/3$ $p_d = 3/3$
footed	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 3/3$ $p_d = 4/3$	 $g_d = 2/3$ $p_d = 5/3$

- Pull-down MOS width are chosen to give unit resistance.
- Precharge occurs when gate is idle which is often slow.
- Footed gates have higher logical effort.

Dynamic Circuit : Monotonicity problem

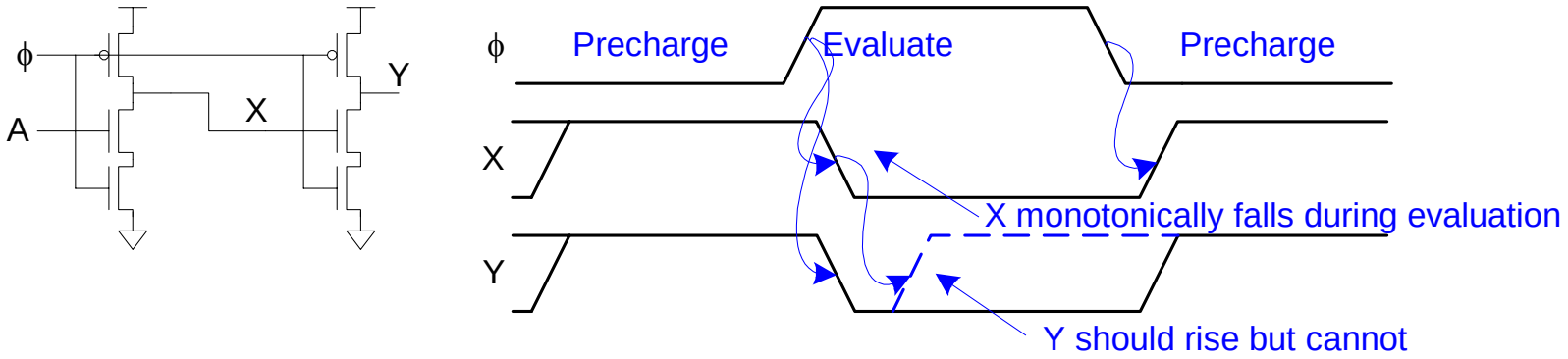
- Dynamic gates require monotonically rising inputs during evaluation
  - 0 -> 0
  - 0 -> 1
  - 1 -> 1
  - But not 1 -> 0





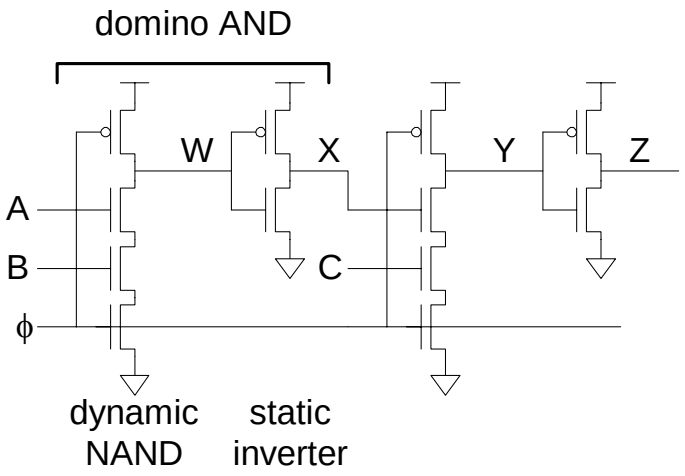
Dynamic Circuit : Monotonicity Woes

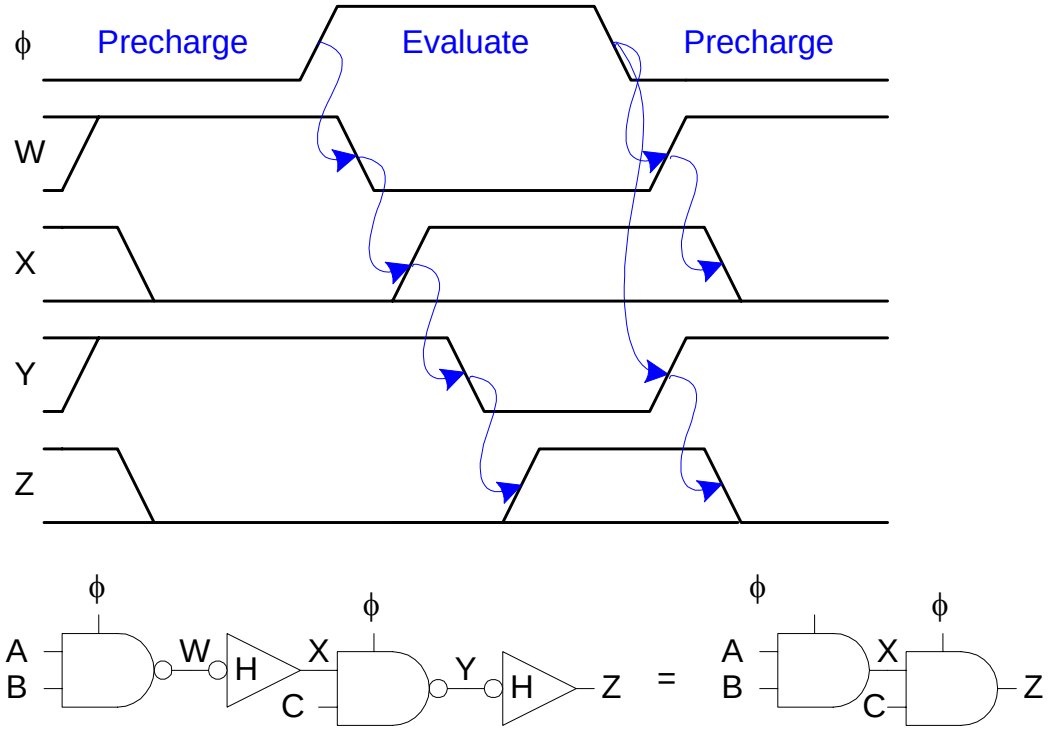
- But dynamic gates produce monotonically falling outputs during evaluation
- Illegal for one dynamic gate to drive another!



Dynamic Circuit : Domino Gates

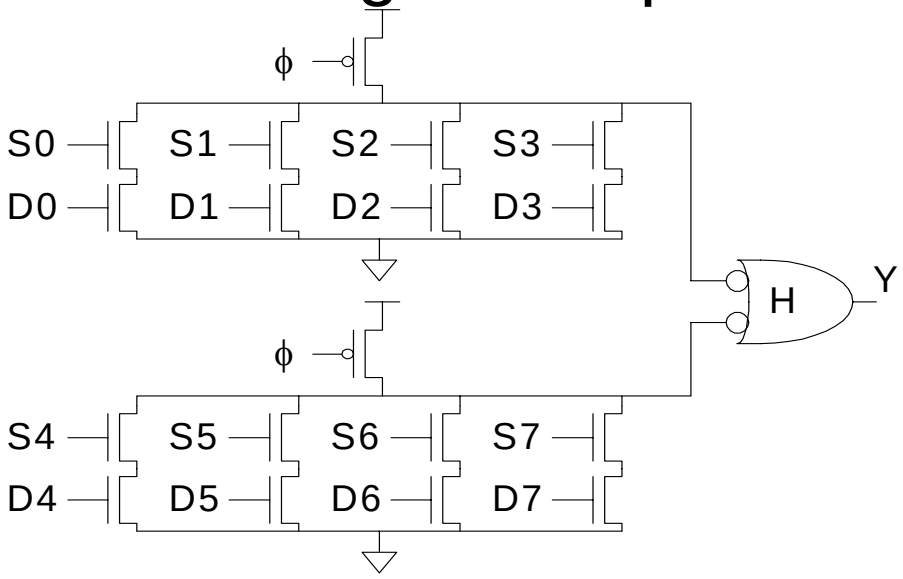
- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs





Dynamic Circuit : Domino Optimizations

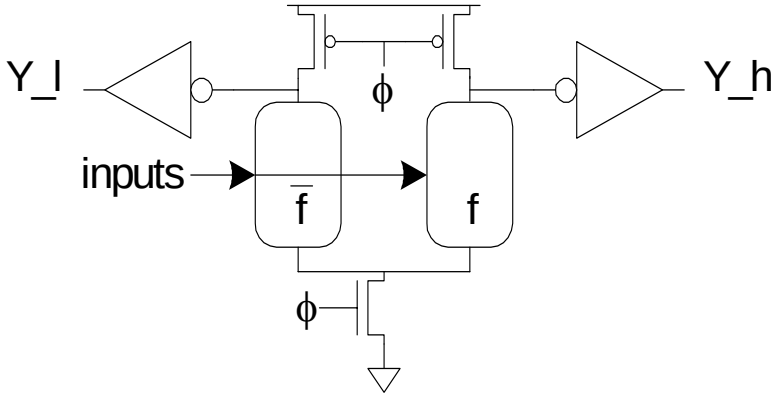
- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- HI-skewed static stages can perform logic



Dynamic Circuit : Dual-Rail Domino

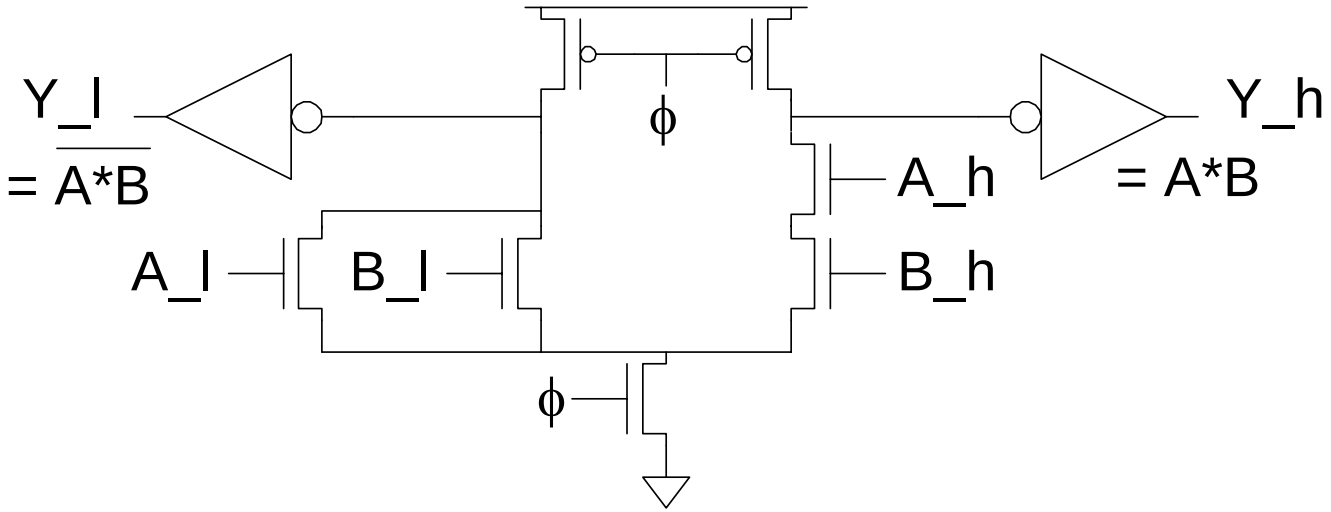
- Domino only performs noninverting functions:
  - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  - Takes true and complementary inputs
  - Produces true and complementary outputs

sig_h	sig_l	Meaning
0	0	Precharged
0	1	‘0’
1	0	‘1’
1	1	invalid



Dynamic Circuit : Dual-Rail Domino

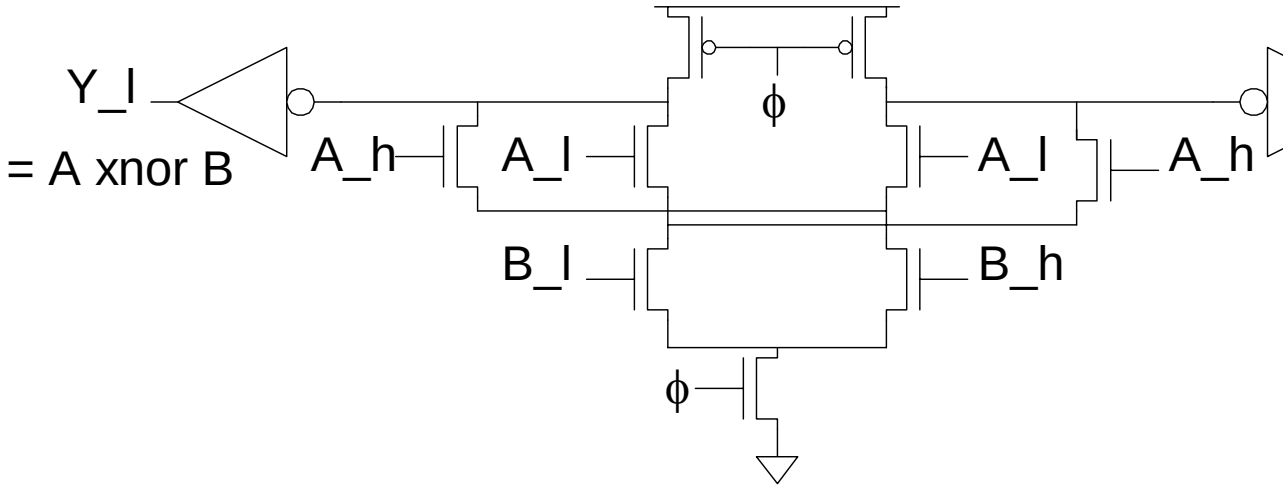
- Given A_h, A_l, B_h, B_l
- Compute Y_h = A * B, Y_l = ~(A * B)
- Pulldown networks are conduction complements



Example: AND/NAND

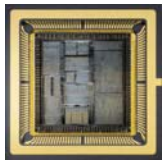
Dynamic Circuit : Dual-Rail Domino

- Sometimes possible to share transistors



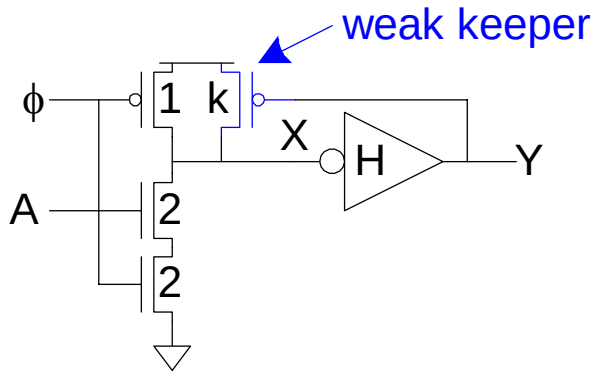
Example: XOR/XNOR

- Dual-rail domino can be viewed as a dynamic form of CVSL, sometimes called DCVS.



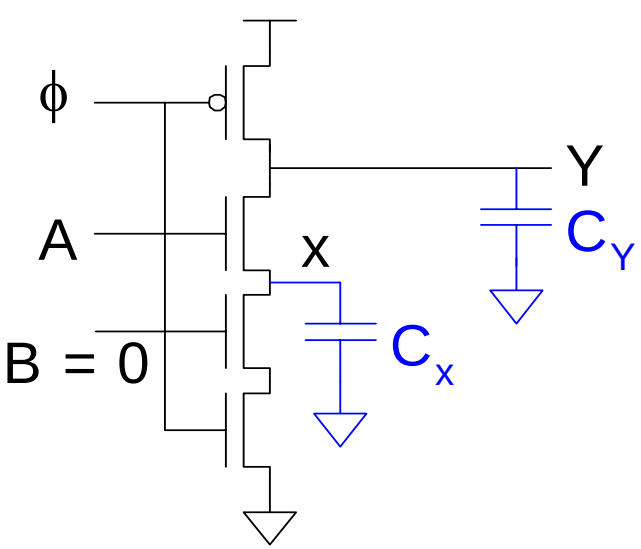
Dynamic Circuit : Leakage

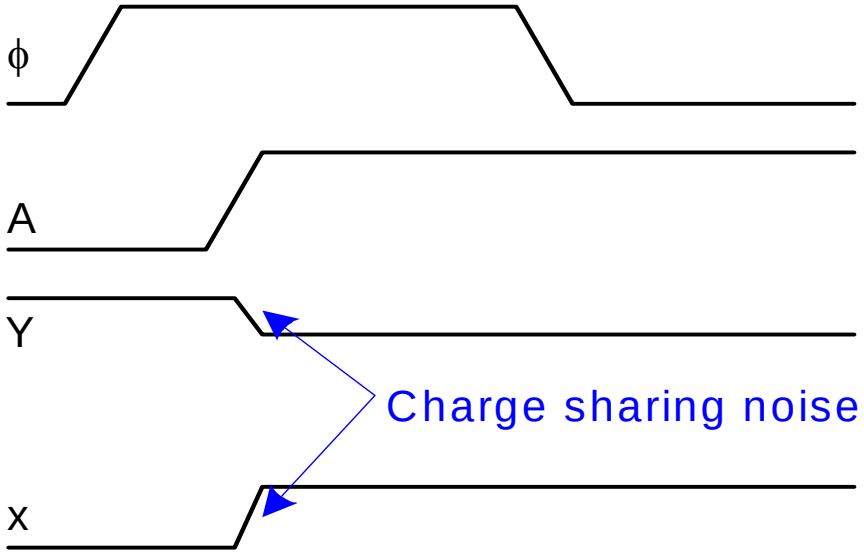
- Dynamic node floats high during evaluation
  - Transistors are leaky ($I_{OFF} \neq 0$)
  - Dynamic value will leak away over time
  - Formerly miliseconds, now nanoseconds!
- Use keeper to hold dynamic node
  - Must be weak enough not to fight evaluation



Dynamic Circuit : Charge Sharing

- Dynamic gates suffer from charge sharing noise.

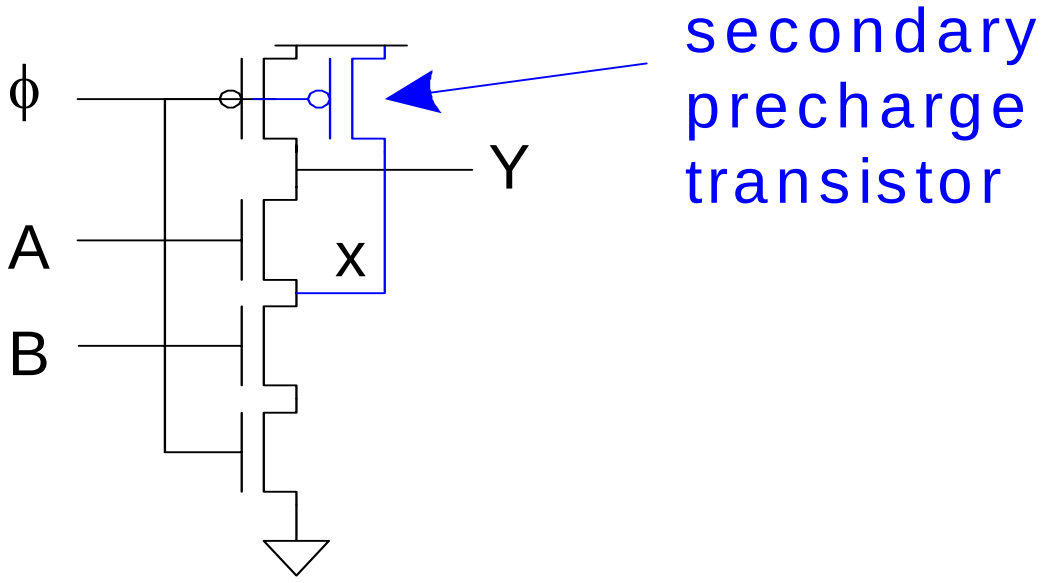


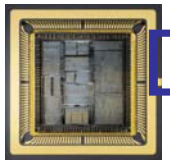


$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

Dynamic Circuit : Secondary Precharge

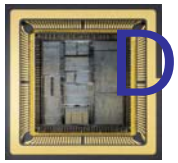
- Solution: add secondary precharge transistors
  - Typically need to precharge every other node
- Big load capacitance C_Y helps as well





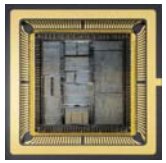
Dynamic Circuit : Noise Sensitivity

- Dynamic gates are very sensitive to noise
  - Inputs: $V_{IH} \approx V_{tn}$
  - Outputs: floating output susceptible noise
- Noise sources
  - Capacitive crosstalk
  - Charge sharing
  - Power supply noise
  - Feedthrough noise
  - And more!



Dynamic Circuit : Domino Summary

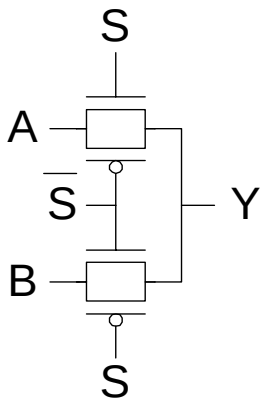
- Domino logic is attractive for high-speed circuits
  - 1.5 – 2x faster than static CMOS
  - But many challenges:
    - Monotonicity
    - Leakage
    - Charge sharing
    - Noise
- Widely used in high-performance microprocessors

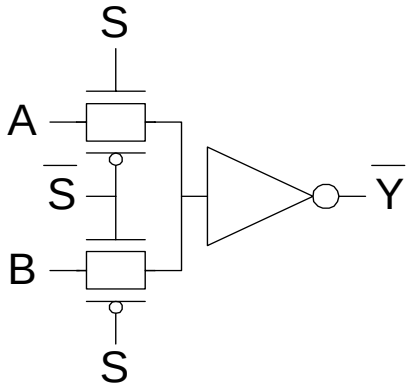


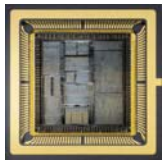
Pass Transistor Circuits

- Use pass transistors like switches to do logic
- Inputs drive diffusion terminals as well as gates

- CMOS + Transmission Gates:
  - 2-input multiplexer
  - Gates should be restoring

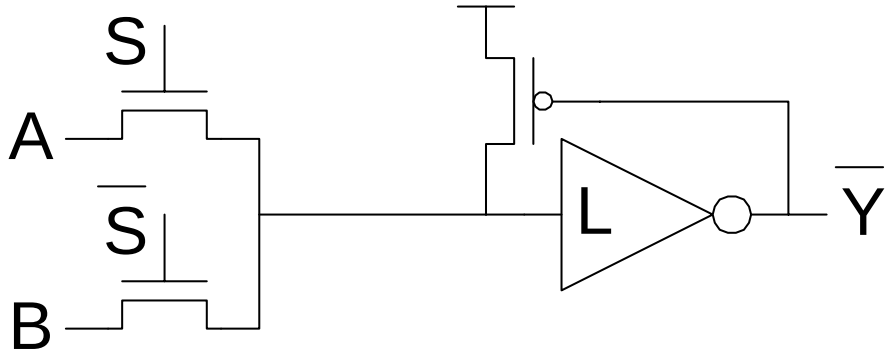


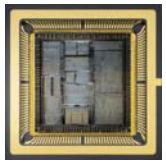




Pass Transistor Circuits : LEAP

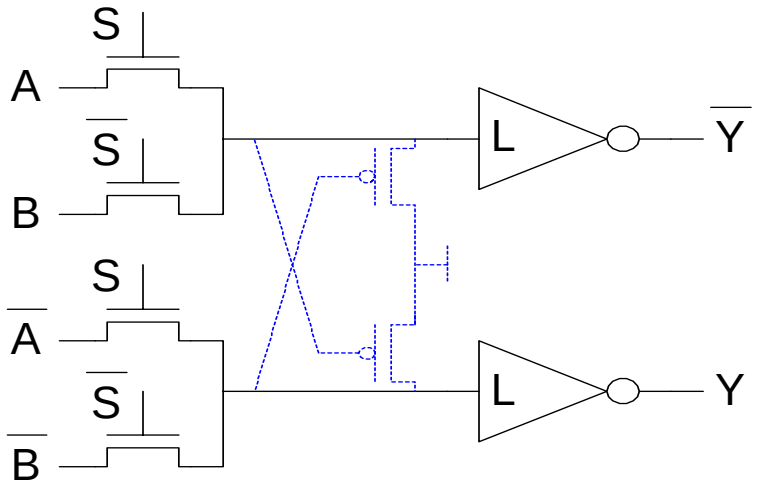
- **LEA**n integration with **P**ass transistors
- Get rid of PMOS transistors
  - Use weak PMOS feedback to pull fully high
  - Ratio constraint

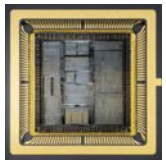




Pass Transistor Circuits : CPL

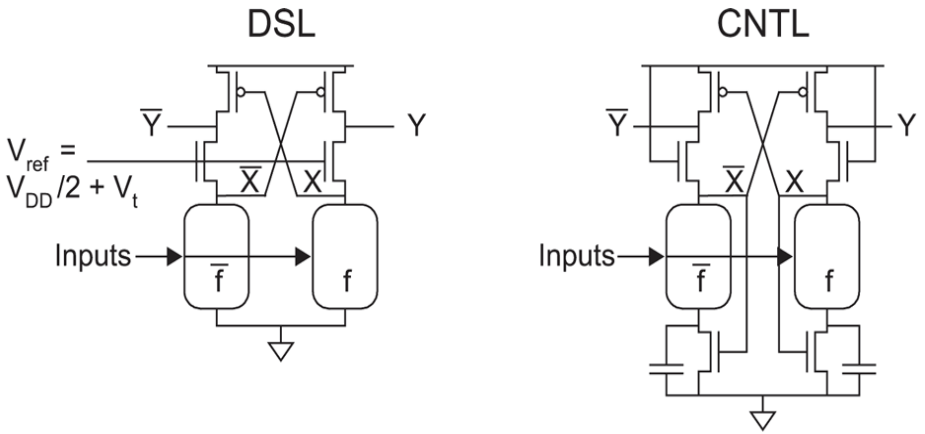
- **C**omplementary **P**ass-transistor **L**ogic
  - Dual-rail form of pass transistor logic
  - Avoids need for ratioed feedback
  - Optional cross-coupling for rail-to-rail swing



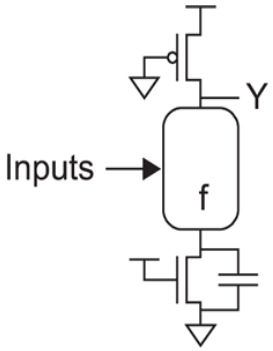


Differential Circuits

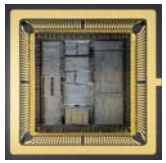
- Derived from basic CVSL using NMOS pull-down network.
- Differential Split Level (DSL) : DSL places NMOS transistors in series with basic CVSL pull-down networks.
- Cascode Nonthreshold Logic (CNTL) : A transistor and a shunting capacitor added to the bottom of each pull-down



Differential circuit families

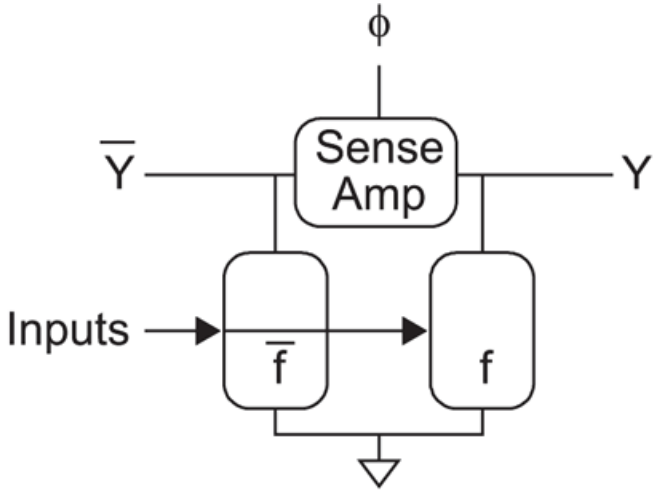


Nonthreshold Logic



Sense-Amplifier Circuit

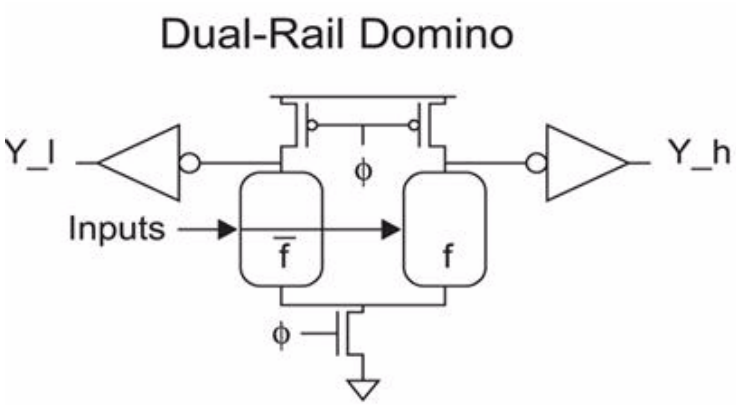
- Sense amplifiers magnify small differential I/P voltage into larger O/P voltage.
- These circuits are also derived from CVSL.
- Used in memories in which differential bitlines have high capacitive load.
- Offer potential for reducing delay in heavily loaded logic circuit as well.

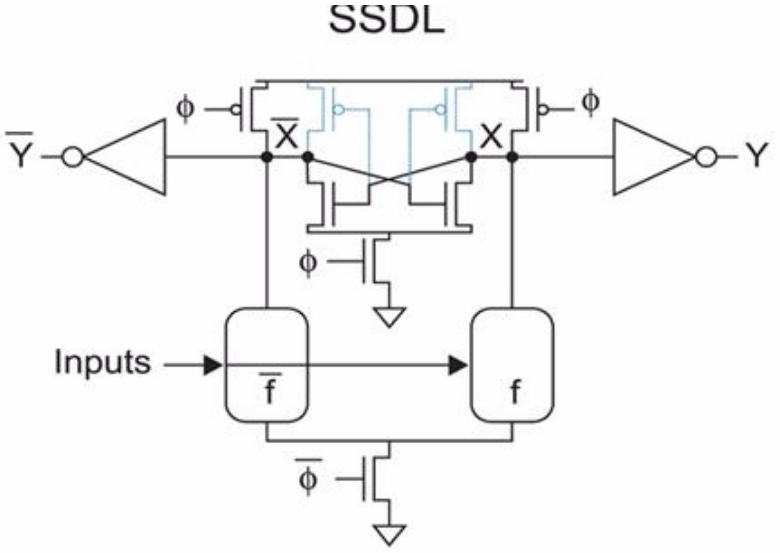


Generic sense-amplifier circuit

Sense-Amplifier Circuit : SSDL

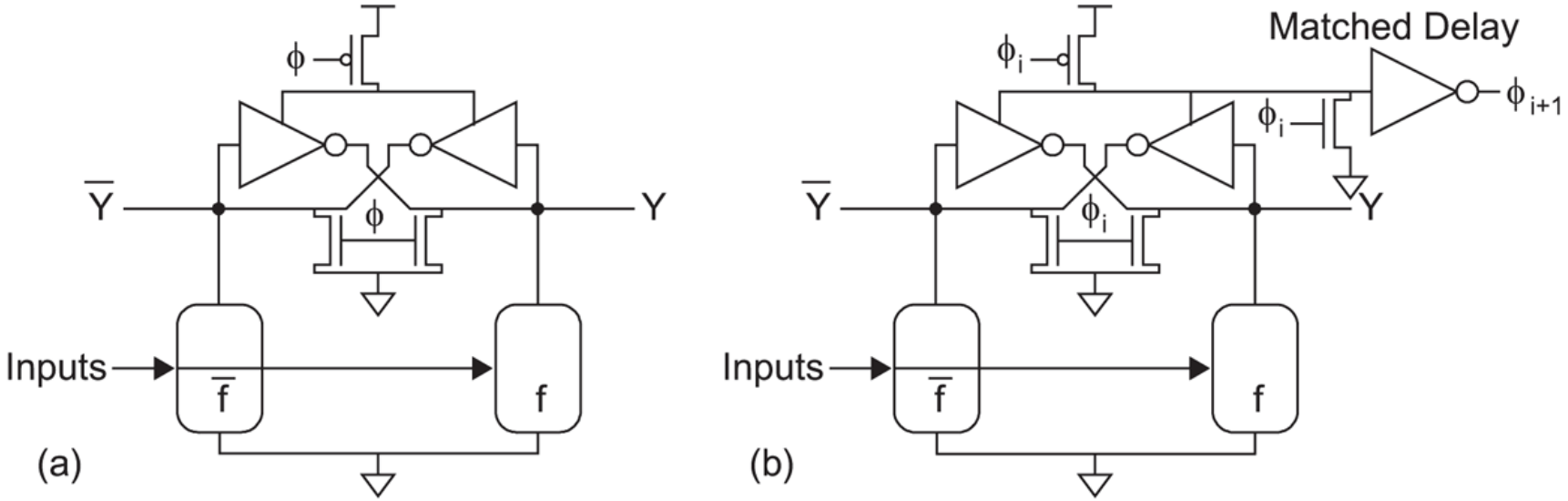
- Sample Set Differential Logic (SSDL) modifies dual-rail domino logic by adding a clocked sense amplifier and modifying the clocking.
- SSDL uses sample and set instead of precharge and evaluation phases.
- Keeper is helpful to restore the high level.



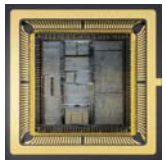


Sense-Amplifier Circuit : ECDL

- Improves on SSDL to eliminate static power dissipation.
- The sense amplifier is made from a pair of cross-coupled clocked inverters.
- Cycle is of two phases : enable and disable



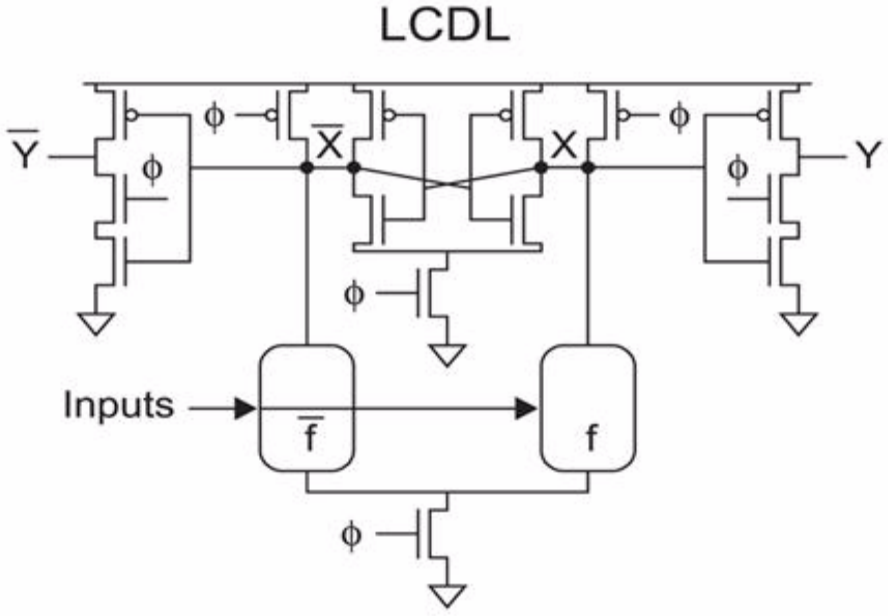
Enable/Disable CMOS Differential Logic



Sense-Amplifier Circuit : LCDL

Latched CMOS Differential Logic (LCDL):

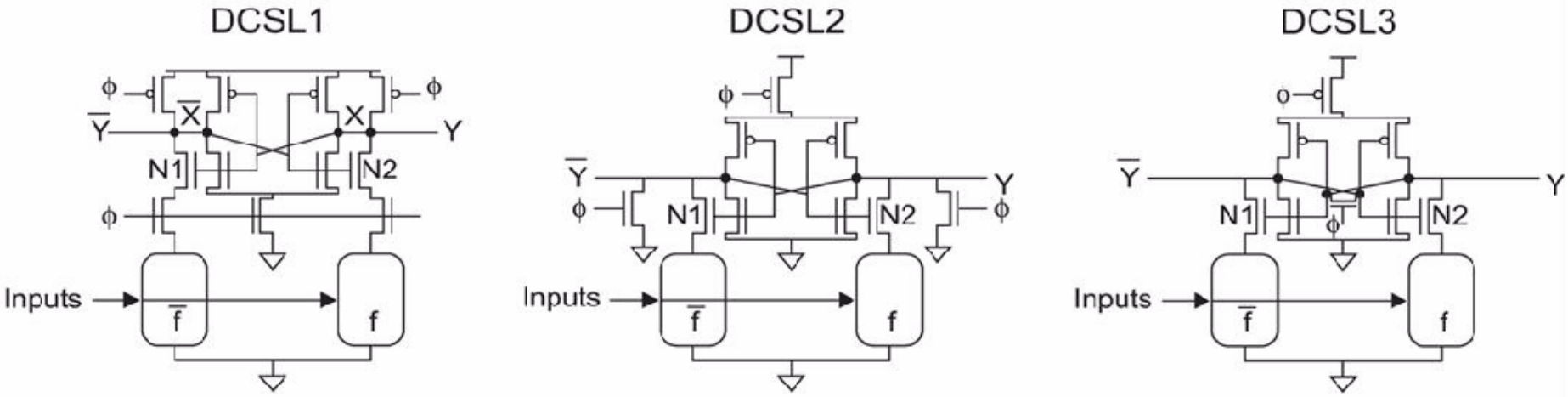
- Adds a sense amplifier directly to the output nodes of a dual-rail domino gate
- Includes n-latches on the outputs
- Risk of amplifying noise as sense-amplifier and dual-rail gate fire at same time.

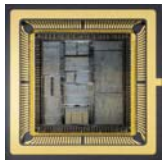


Sense-Amplifier Circuit : DCSL

Differential Current Switch Logic (DCSL):

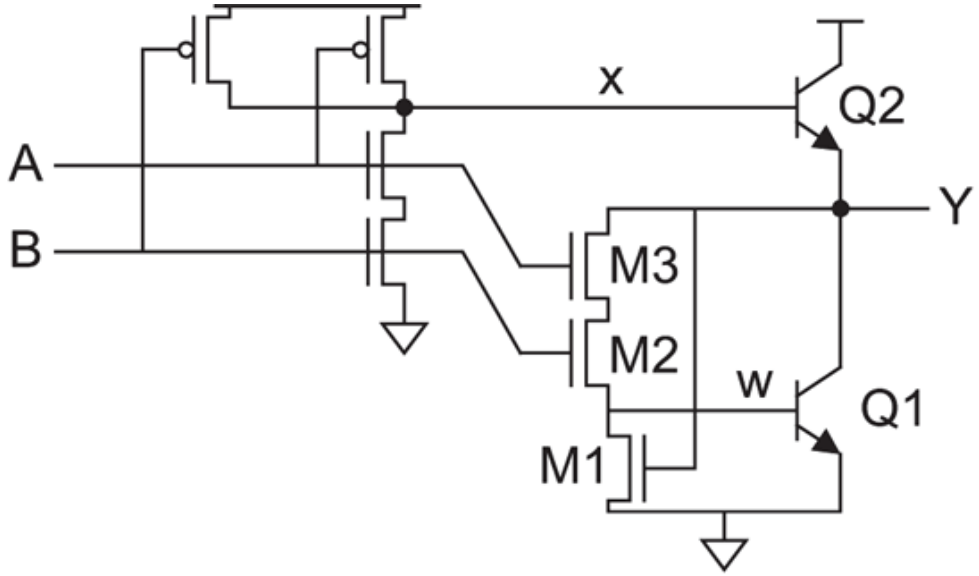
- Due to O/P transitions in every cycle the differential circuit can consume more dynamic power.
- DCSL reduces the power consumption of internal nodes and offer high speed by swinging the pull-down networks through a small voltage.

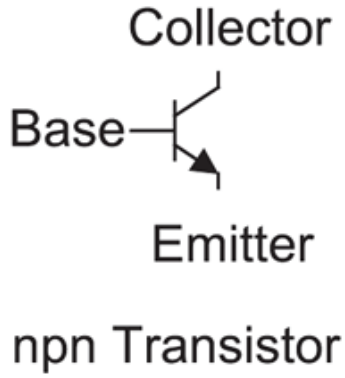




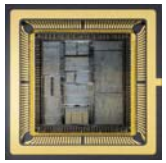
BiCMOS Circuit

- For equal capacitance BJT can deliver much higher output current than a CMOS.
- Can be used to build gates with low logical effort and are good for driving large capacitive loads.





BiCMOS NAND gate



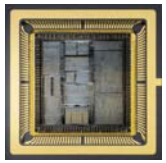
Comparison of Circuit Families

Table 6.4 Comparison of circuit families

Family	nMOS	pMOS	Differ-ential	Static Power	Rail-to-rail Out-put	Dynamic Nodes	Restor-ing	Ratioed	Cascade-able	Robust-ness
Static CMOS	k	k	NO	NO	YES	NO	YES	NO	YES	HIGH
Pseudo-nMOS	k	1	NO	YES	NO	NO	YES	YES	YES	MEDIUM
SFPL	2k + 2	1	NO	YES	NO	NO	YES	YES	YES	MEDIUM
CVSL	2k	2	YES	NO	YES	NO	YES	NO	YES	HIGH
Dynamic	k + 1	1	NO	NO	YES	YES	YES	NO	NO	LOW
Domino	k + 2	2	NO	NO	YES	YES	YES	NO	YES	LOW
Dual-rail Domino	2k + 3	4	YES	NO	YES	YES	YES	NO	YES	LOW
CMOSTG	k	k	NO	NO	YES	NO	YES	NO	YES	HIGH
LEAP	k	2	NO	NO	YES	NO	YES	YES	YES	MEDIUM
DPL	2k	2k	YES	NO	YES	NO	YES	NO	YES	HIGH
CPL	2k	4	YES	NO	YES	NO	YES	NO	YES	MEDIUM
EEPL	2k	4	YES	NO	YES	NO	YES	NO	YES	MEDIUM
SRPL	2k	2	YES	NO	YES	NO	YES	YES	YES	LOW
DCVSPG	2k – 2	2	YES	NO	YES	NO	NO	NO	YES	MEDIUM
PPL	k	k	YES	NO	YES	NO	NO	NO	YES	LOW
DSL	2k + 2	2	YES	YES	NO	NO	YES	NO	YES	MEDIUM
CNTL	2k + 4	2	YES	YES	NO	NO	YES	NO	YES	MEDIUM
NTL	k + 1	1	NO	YES	NO	NO	YES	YES	YES	MEDIUM
SSDL	2k + 6	6	YES	YES	YES	NO	YES	NO	NO	VERY LOW
EDCL	2k + 4	3	YES	NO	YES	NO	YES	NO	NO	VERY LOW
LCDL	2k + 8	6	YES	NO	YES	NO	YES	NO	NO	VERY LOW
DCSL1	2k + 7	4	YES	NO	YES	NO	YES	NO	NO	VERY LOW
BiCMOS	2k + 1	k	NO	YES	NO	NO	YES	NO	YES	MEDIUM

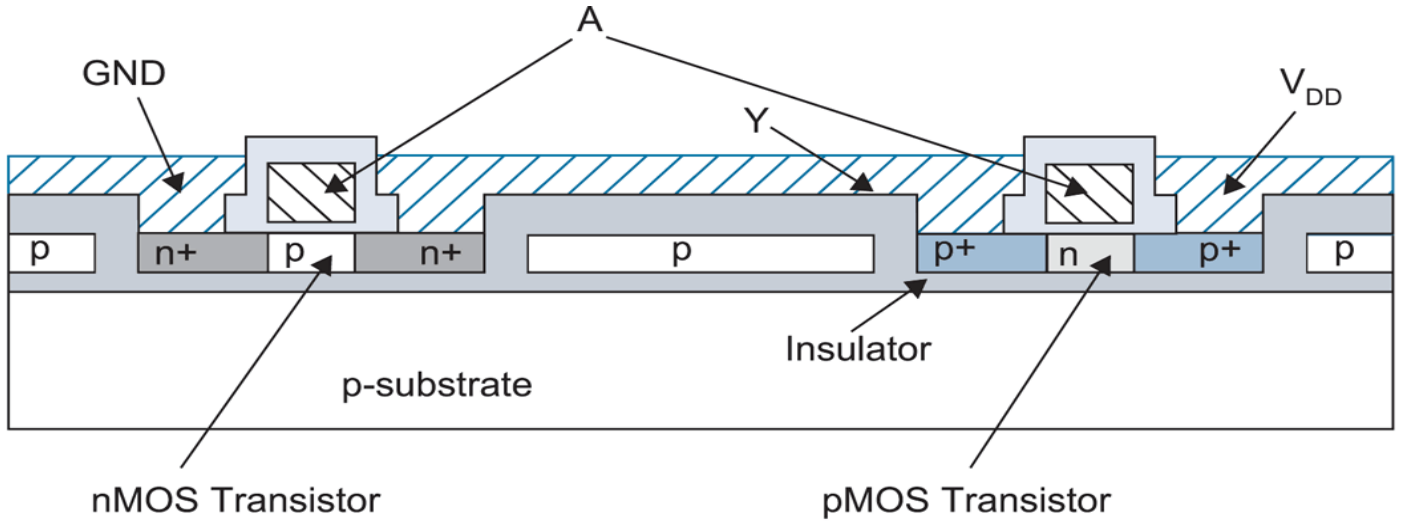
Silicon-on-Insulator (SOI) Circuit Design

- Low power high performance circuit design possible.
- SOI has higher manufacturing costs
- SIO transistors have some unusual behavior
- SIO Vs conventional bulk technology : source, drain and body are surrounded by insulating oxide rather than the conductive substrate, well or bulk.
- Insulator eliminates most of the parasitic diffusion capacitance.
- Any change in body voltage modulates V_t as body can not be connected to V_{dd} or GND.



SOI Circuit Design

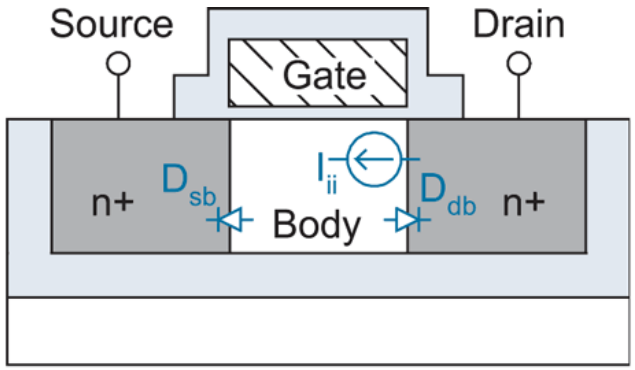
- SOI : partially depleted (PD) or fully depleted (FD)
- FD SOI : body is thinner than channel depletion width, thus body charge is fixed and its voltage remains constant
- PD SOI : body is thicker and its voltage can vary depending on amount of charge (vary through body effect)
- FD SOI are difficult to manufacture due to thin body



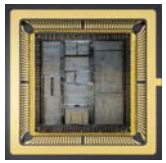
SOI inverter cross-sections

SOI Circuit Design : Floating Body Voltage

- Paths for flow into the body:
  - Reverse biased junctions, D_{db} and D_{sb} carry small diode leakage
  - The impact of ionization current is modeled as I_{ii}
- Paths for exit from the body:
  - As D_{sb} junction become forward biased due to increase in body voltage
  - Same thing happens due to capacitive coupling of gate-body and drain-body.



Charge paths to/from floating body (PD SOI)

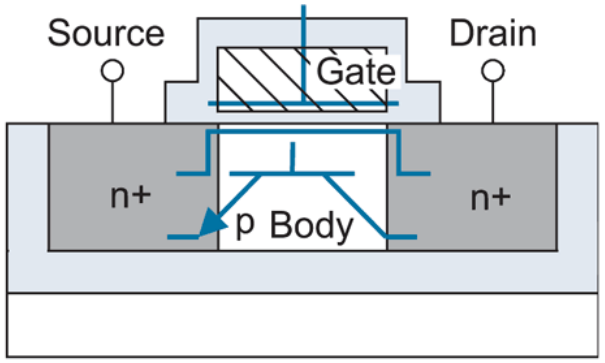


SOI Circuit Design : Advantages

- Source and drain abut against oxide on bottom and side walls not facing the channel, thus eliminating parasitic capacitances of these sides.
- Thus, smaller parasitic delay and lower dynamic power consumption.
- Potential for lower threshold voltages → faster transistor especially for low V_{dd} operations
- Immune to latch-up effect

SOI Circuit Design : Disadvantages

- PD SOI suffer from history effect i.e. change in body voltage modulates the V_t and adjusts the delay.
- Presence of parasitic bipolar transistor within each transistor.
- BJT can cause pass-gate leakage : Pulse current flows from drain to source when the source is pulled low even though transistor is OFF.
- Self heating as oxide is a thermal insulator as well.



Parasitic bipolar transistor in PD SOI