

# **Test 1 Syllabus**

## **CSCI 5330: Digital CMOS VLSI Design**

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#### **NOTE:**

- This is closed book, closed text examination.
- Calculators are NOT allowed in the examination.

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NOTE: All material covered from 18<sup>th</sup> Jan 05 to 22<sup>nd</sup> Feb 05 is the syllabus of the test1.

1. Five classic components of a computer
2. Microprocessor
3. IC design abstraction level
4. Developmental trends of ICs
5. Moore's Law
6. MOS Transistors
7. CMOS Logic
8. CMOS Fabrication
9. Design Partitioning
10. Logic Design
11. Circuit Design
12. Physical Design
13. Fabrication, Packaging, and Testing
14. MOS modes of operation
15. MOS regions of operation
16. Ideal I-V Characteristics
17. C-V Characteristics
18. Non-ideal I-V Effects
19. DC Transfer Characteristics
20. Delay Definitions
21. Switch-level RC Delay Models
22. Effective Resistance and Capacitance
23. Diffusion Capacitance and Layout Effects
24. Elmore Delay Model
25. Linear Delay Model
26. Parasitic Delay
27. Logical Efforts