Test 2 Syllabus

CSCI 5330: Digital CMOS VLSI Design

Instructor: Dr. Saraju P. Mohanty

NOTE:

- This is closed book, closed text examination.
- Calculators are NOT allowed in the examination.

NOTE: All material covered from 24th Feb 05 to 22nd Mar 05 is the syllabus of the test2.

1. Delay in a Logic Gate
2. Multistage Logic Networks
3. Choosing the Best Number of Stages
4. Limitations of Logical Effort
5. Power and Energy
6. Dynamic Power
7. Static Power
8. Low Power Design
9. Wire Resistance
10. Wire Capacitance
11. Wire RC Delay
12. Crosstalk
13. Wire Engineering
14. Repeaters
15. Design Margin
16. Reliability
17. Scaling
18. DC Analysis
19. Transient Analysis
20. Subcircuits
21. Optimization
22. Power Measurement
23. Logical Effort Characterization