CSCE 5730: Digital CMOS VLSI Design

Instructor: Dr. Saraju P. Mohanty

Assignment 3

Assigned Dated: 15th Feb 2006 (Wed)

Due Date: 22nd February 2006 (Wed)

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1. Design and verify the circuits of MUX, D-latch, D-FF, and a SRAM cell using DSCH tool as discussed in the class. Provide printouts for the schematic designs and simulation results.