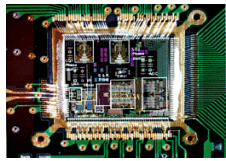
Lecture 7: The Inverter

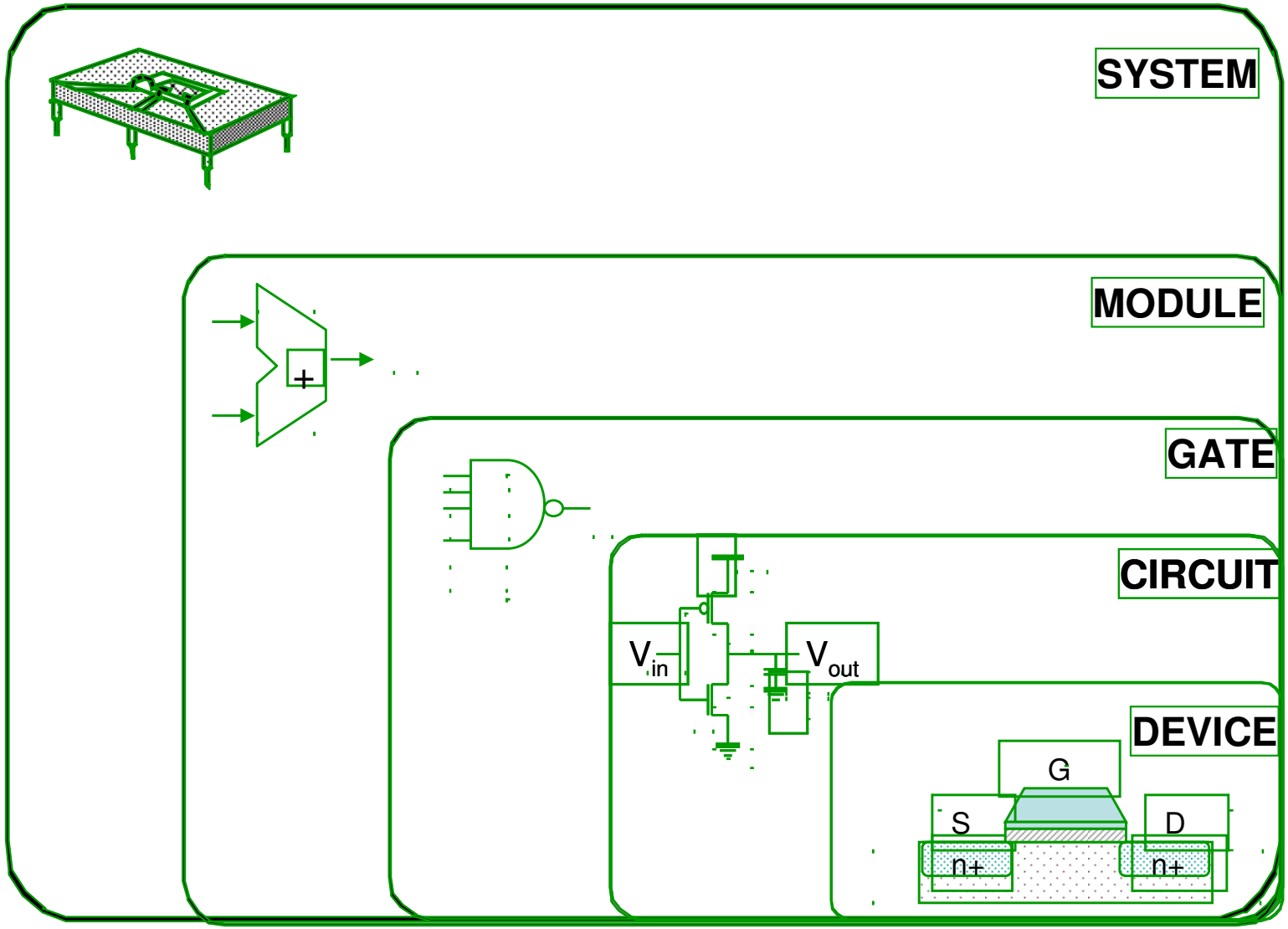
CSCE 5730
Digital CMOS VLSI Design

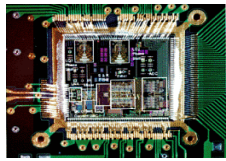
Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.

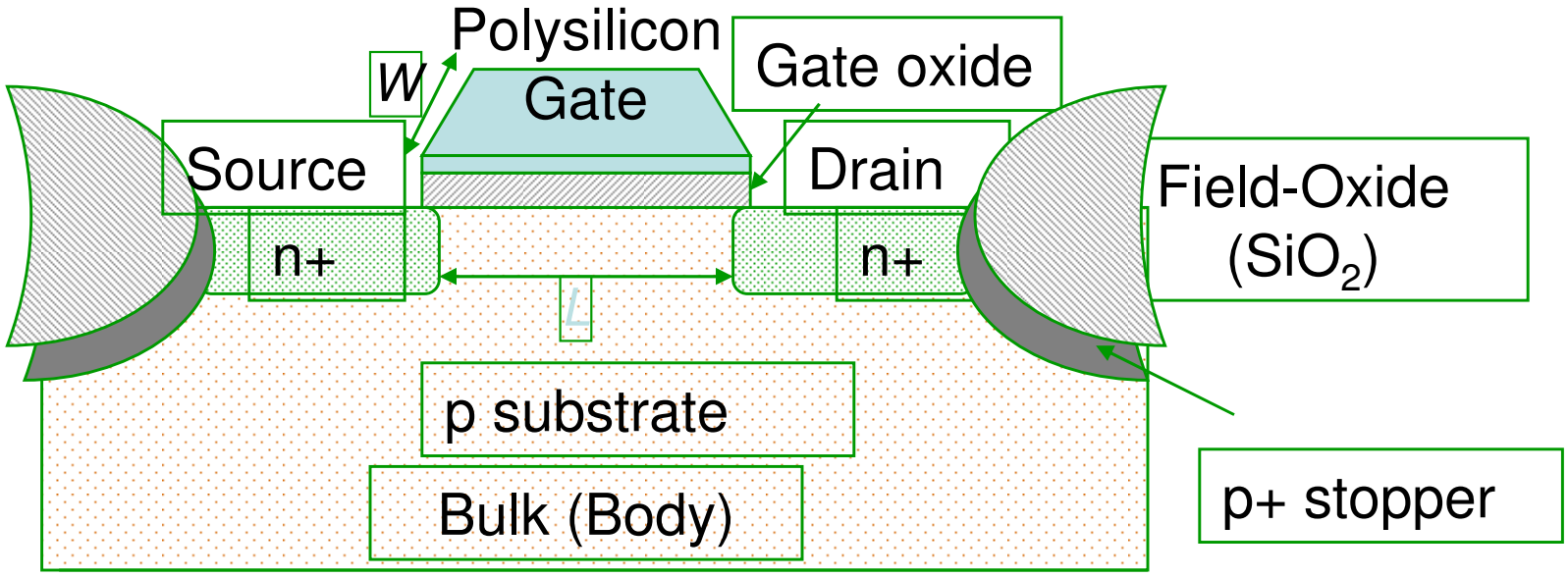


Review: Design Abstraction Levels



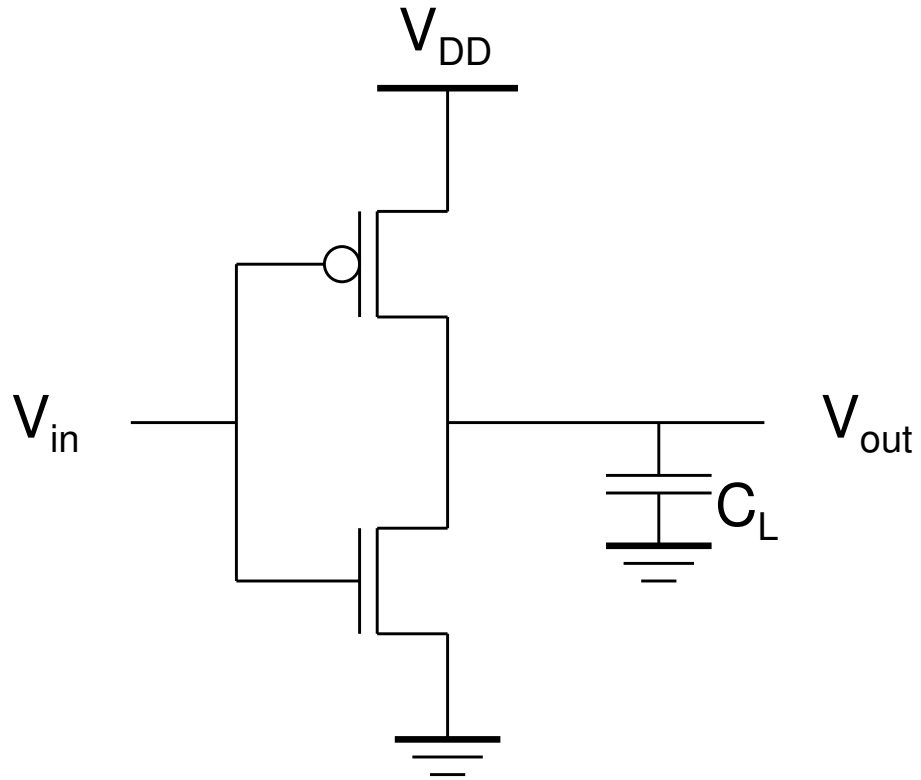


Review: The MOS Transistor

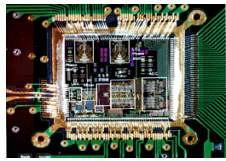


- Starting at the bottom of the design abstraction chart
- Gate Oxide – insulator, NMOS – since carriers are electrons (n type carriers), M – metal; O – oxide; S – semiconductor
- Field oxide isolates one device from neighboring devices
- View transistor as a switch with an infinite off-resistance and a finite on-resistance

CMOS Inverter: A First Look

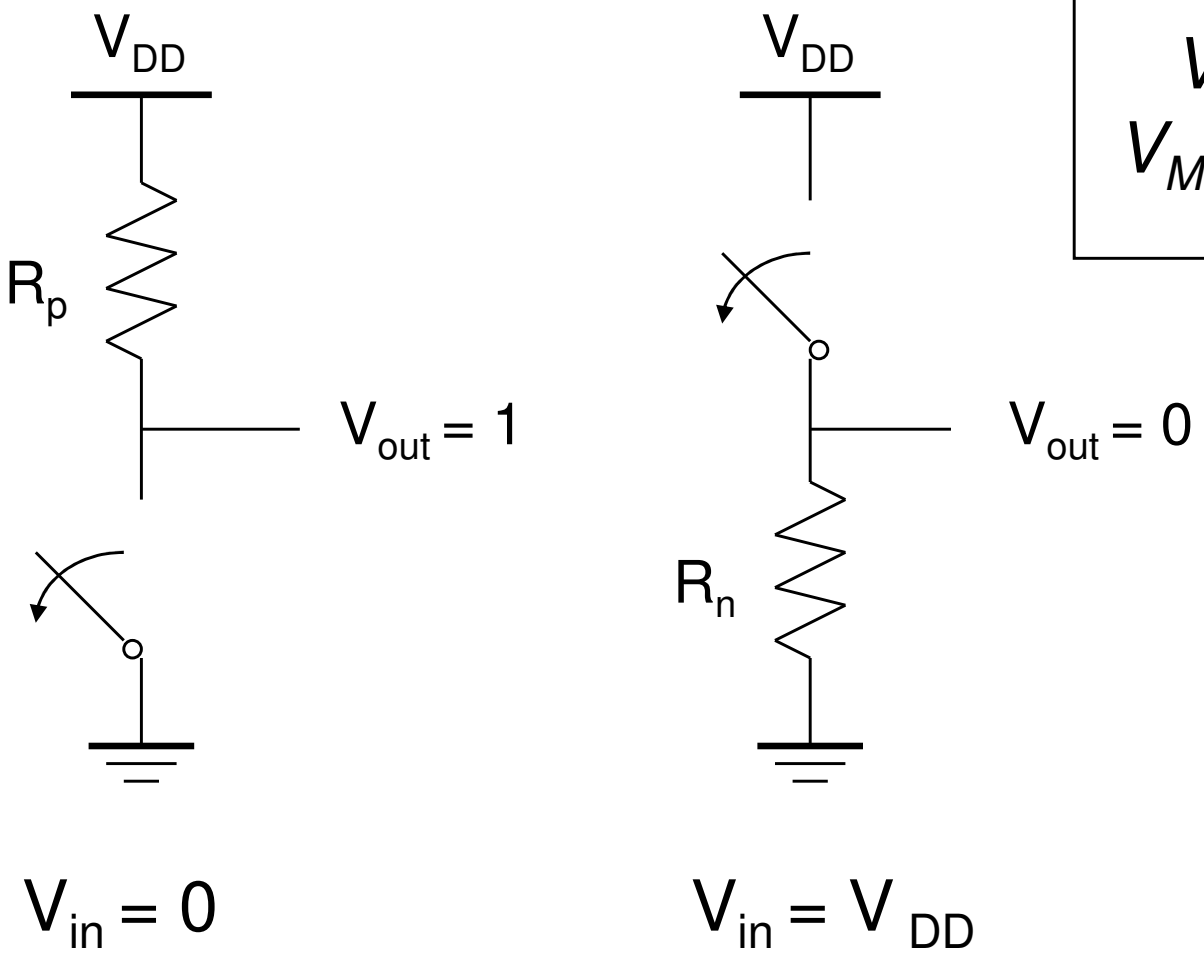


- Inverter – the nucleus of all digital designs; foundation of more intricate gates
- Design metrics – cost (area); integrity and robustness (static – steady-state behavior); performance (dynamic or transient behavior); energy efficiency



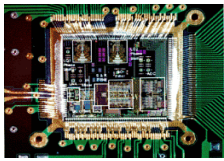
CMOS Inverter: Steady State Response

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$



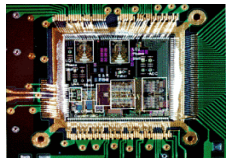
CMOS Properties

- Full rail-to-rail swing ⇒ high noise margins
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ ratioless
- Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ nearly zero steady-state input current
- No direct path steady-state between power and ground ⇒ no static power dissipation

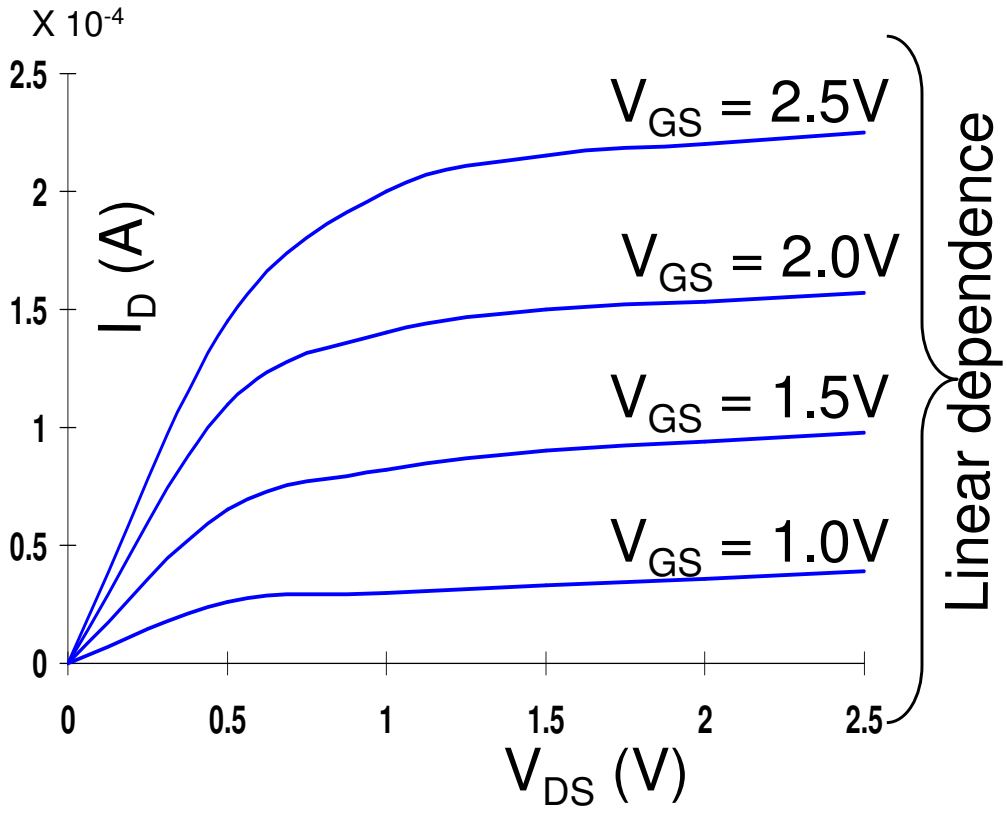


CMOS Properties …..

- Propagation delay function of load capacitance and resistance of transistors
- rail-to-rail - Vdd to 0V giving good noise margins
- power dissipation - no path between Vdd and Gnd in steady state (ignores leakage current)
- ratioless - logic levels are not dependent upon relative device sizes (as in NMOS), so transistors can be minimum size
- single inverter can theoretically drive an infinite number of gates and still be functionally operational; fan-out increases propagation delay
- steady state path to Vdd or GND - low output impedance, so less sensitive to noise

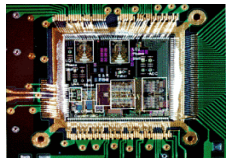


Review: Short Channel I-V Plot (NMOS)



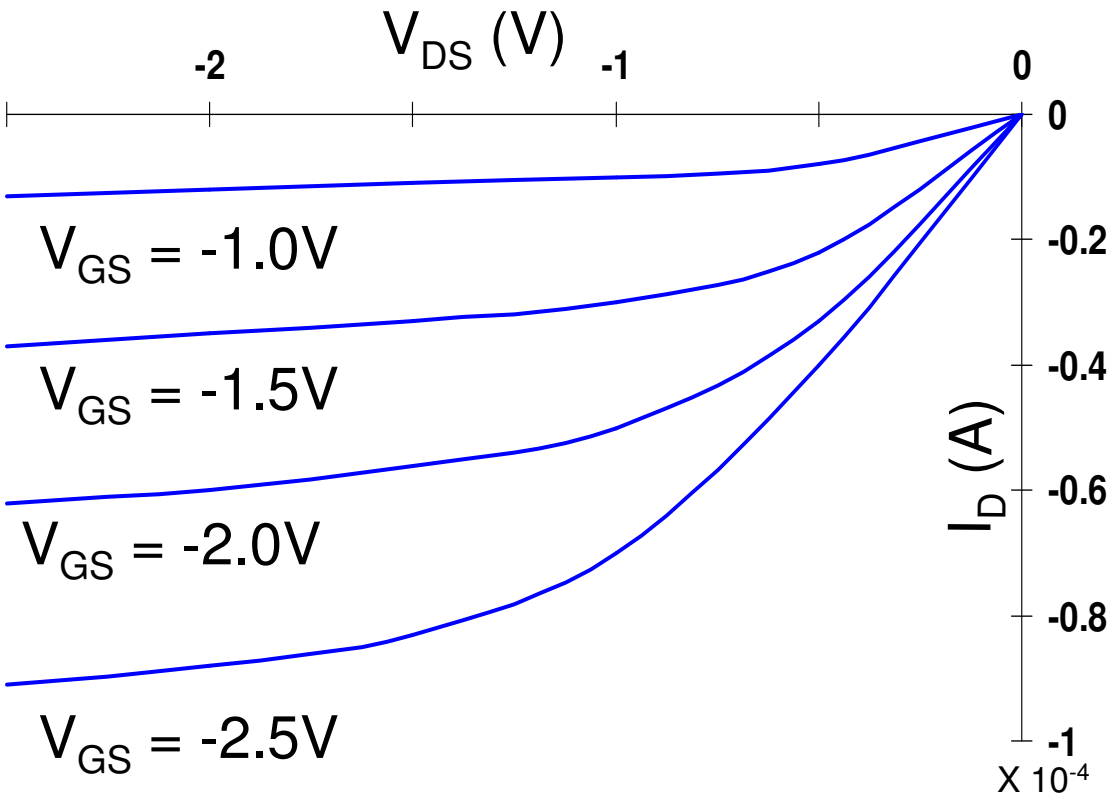
NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

- Ld is drawn length
- Linear dependence of saturation current wrt VGS
- Velocity saturation causes device to saturate for substantially smaller values of VDS.
- Results in a substantial drop in current drive for high voltage levels.
- The drain current of the short channel device is only 40% of the corresponding value of the long channel device (220 uA versus 540 uA)



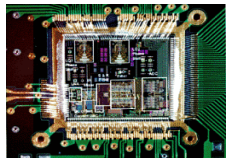
Review: Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

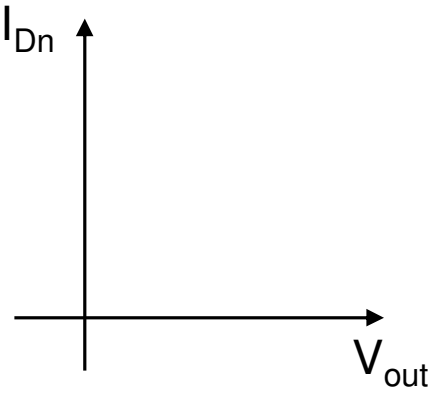
- All the derived equations hold for PMOS – for PMOS devices the polarities of all voltages and currents are reversed
- Due to lower mobility, the maximum current is only 42% of what is achieved by a similar NMOS transistor
- Effects of velocity saturation are less pronounced than in NMOS (smaller mobility of holes act electrons)

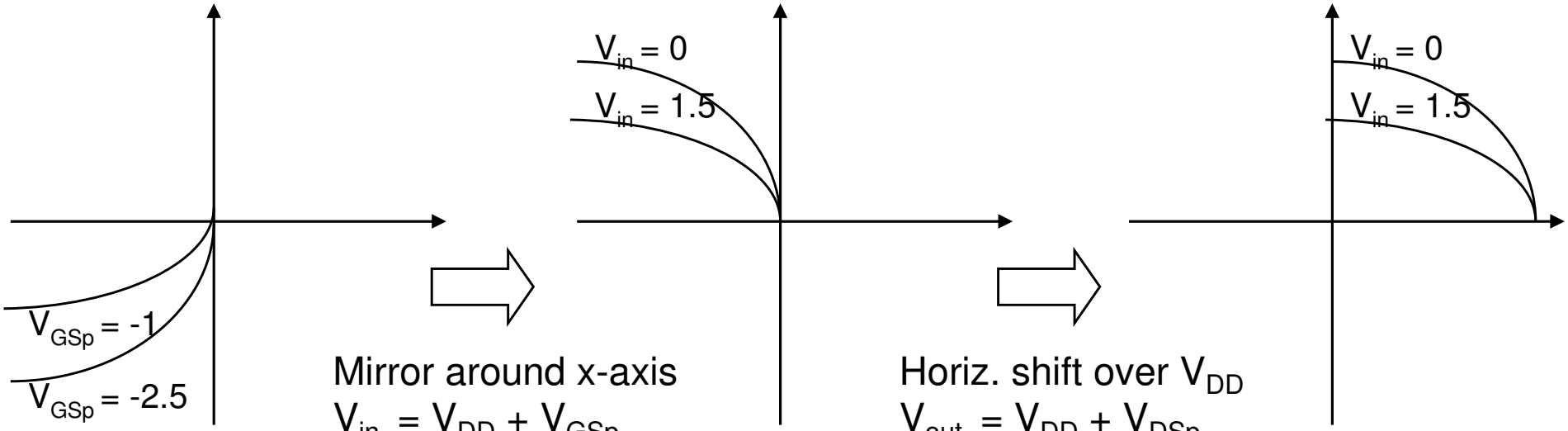


Transforming PMOS I-V Lines

- Want common coordinate set V_{in}, V_{out}, and I_{Dn}

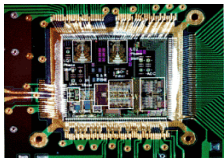
$$I_{DSp} = -I_{DSn}$$
$$V_{GSn} = V_{in} \; ; V_{GSp} = V_{in} - V_{DD}$$
$$V_{DSn} = V_{out} \; ; V_{DSp} = V_{out} - V_{DD}$$



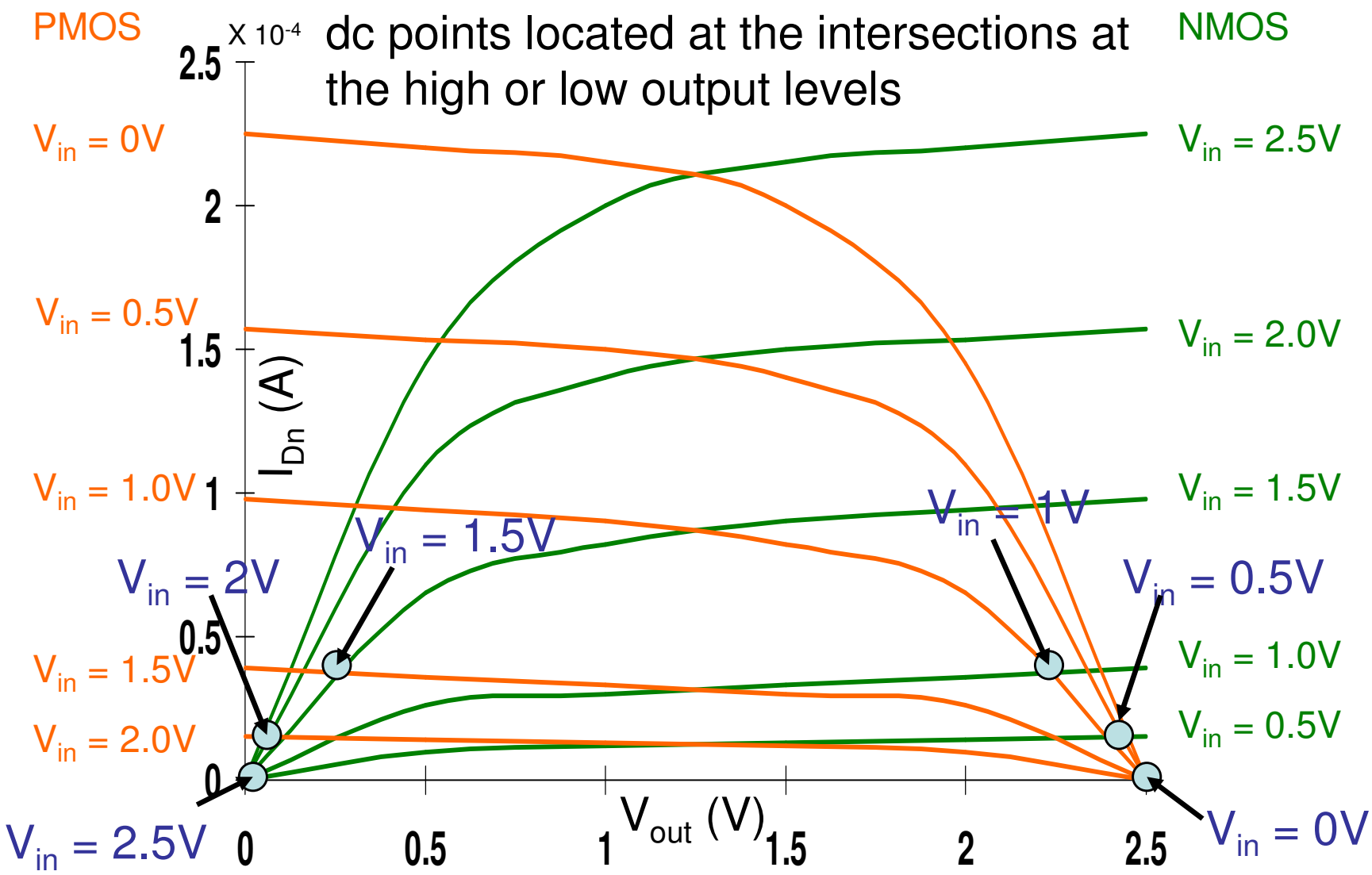


Mirror around x-axis
$V_{in} = V_{DD} + V_{GSp}$
$I_{Dn} = -I_{Dp}$

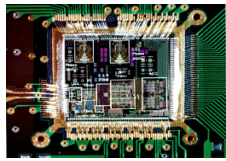
Horiz. shift over V_{DD}
$V_{out} = V_{DD} + V_{DSp}$



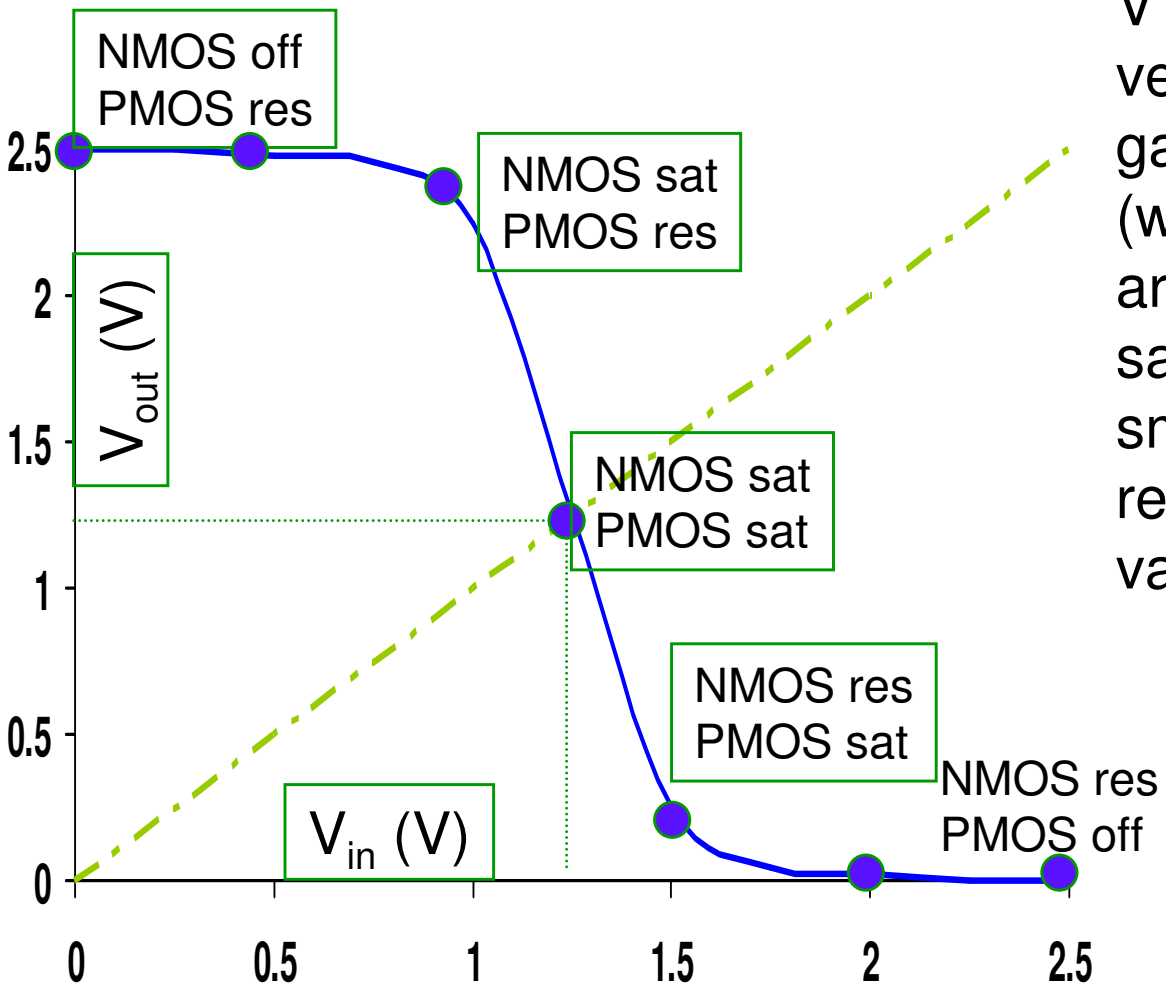
CMOS Inverter Load Lines



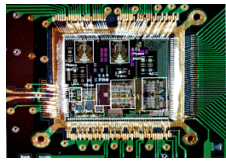
0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$



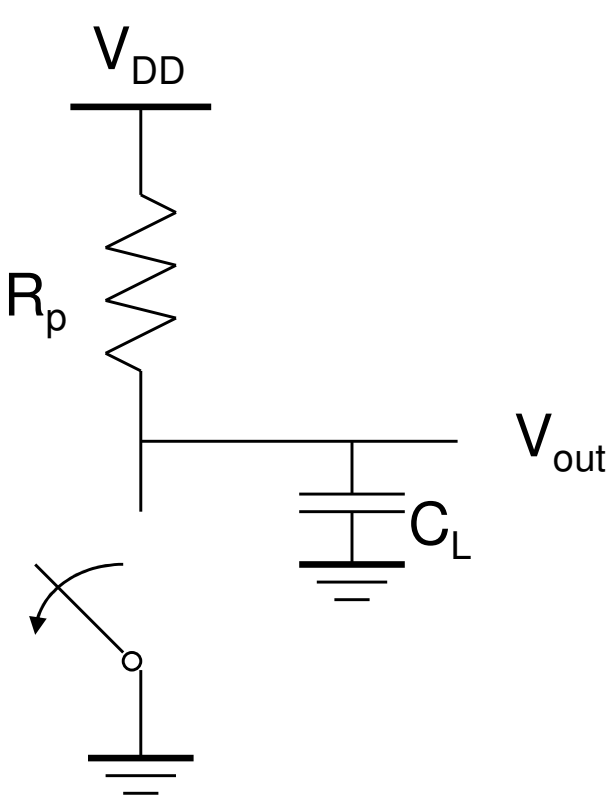
CMOS Inverter VTC



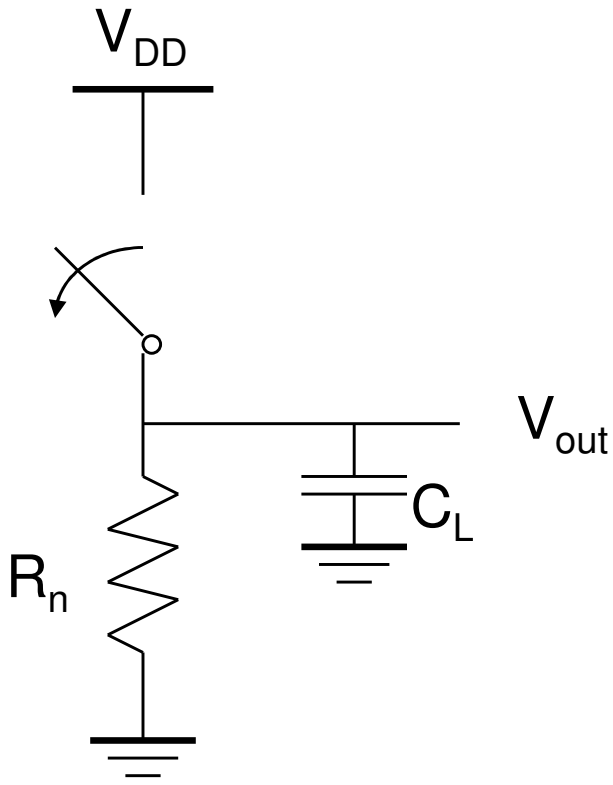
VTC of the inverter exhibits a very narrow transition zone; high gain during switching transient (when both PMOS and NMOS are simultaneously on and in saturation). In that region, a small change in input voltage results in a large output voltage variation.



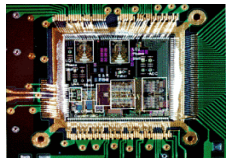
CMOS Inverter:
Switch Model of Dynamic Behavior



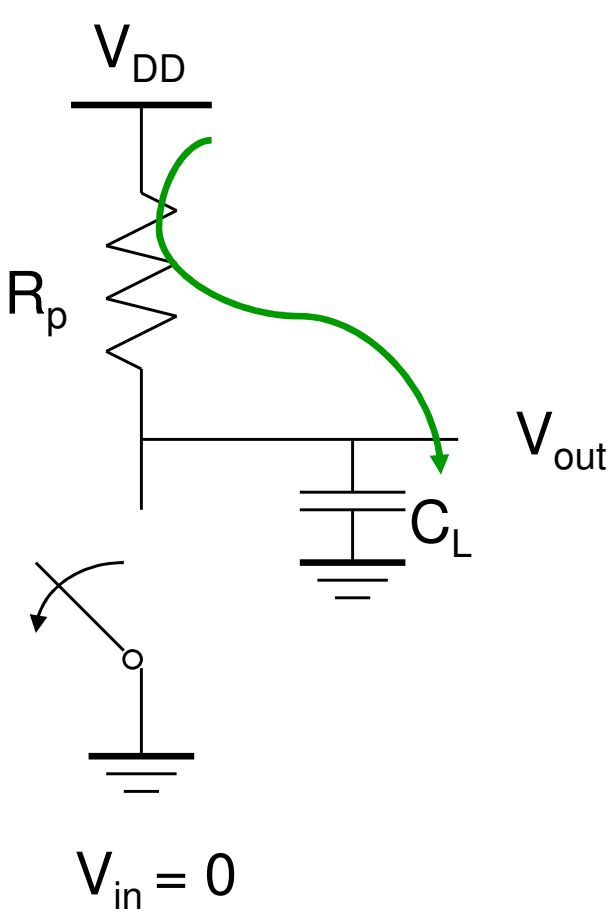
$V_{in} = 0$

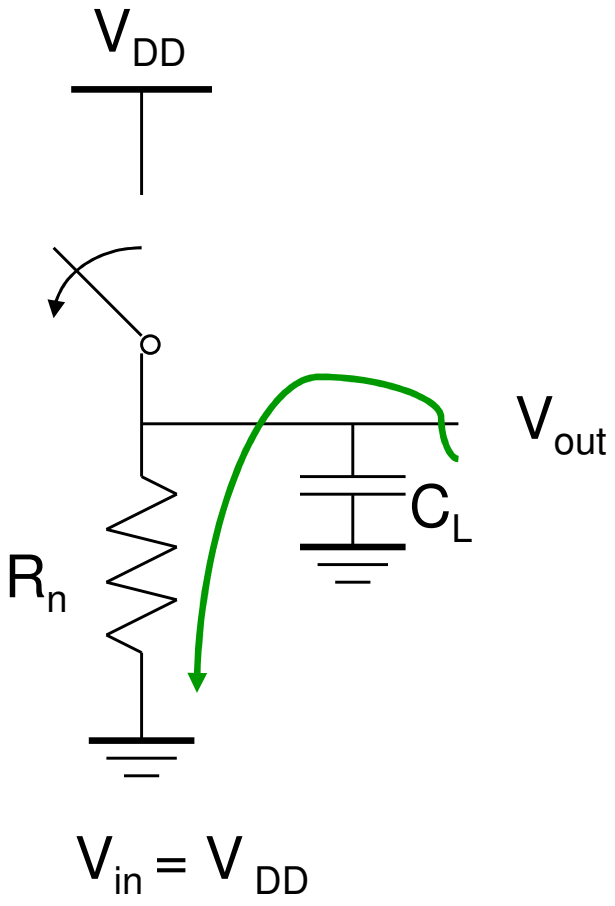


$V_{in} = V_{DD}$

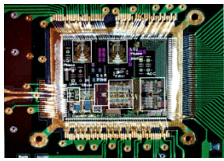


CMOS Inverter:
Switch Model of Dynamic Behavior



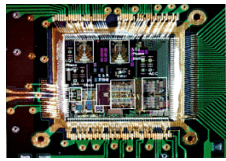


- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)



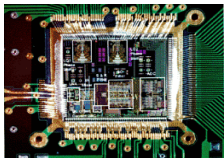
CMOS Inverter:
Switch Model of Dynamic Behavior

- Response determined mainly by the output capacitance of the gate, drain diffusion capacitance of NMOS and PMOS; the connecting wires, and input capacitances of the fan-out gates
- A fast gate is built either by keeping the output capacitance small or by decreasing the on-resistance or the transistor (or both)
- Decreasing the on-resistance achieved by increasing the W/L ratio of the device
- On-resistance of the NMOS and PMOS transistors is not constant; rather it is a nonlinear function of the voltage across the transistor



Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

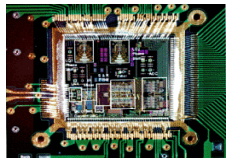


Switching Threshold

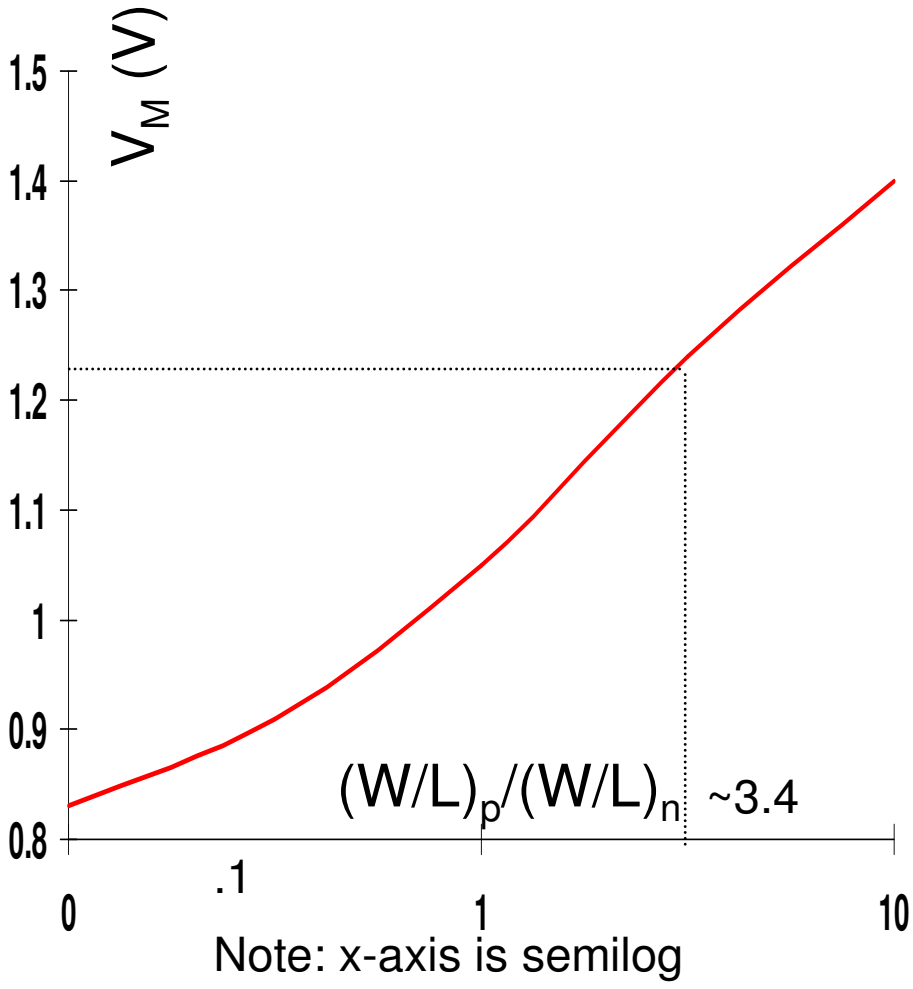
- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$), $V_M \approx rV_{DD}/(1 + r)$ where $r = k_pV_{DSATp}/k_nV_{DSATn}$
- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS
- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n'V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k_p'V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

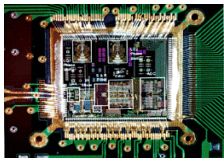
- Assumes: Supply voltage is high enough so that the devices are velocity-saturated (VDSAT < VM – VT) and ignores channel length modulation.
- Reminder: k = k'W/L and k' = mu Cox (mu is carrier mobility)
- Larger r to move VM upwards means making the PMOS wider
- Smaller r to move VM downwards means making the NMOS wider



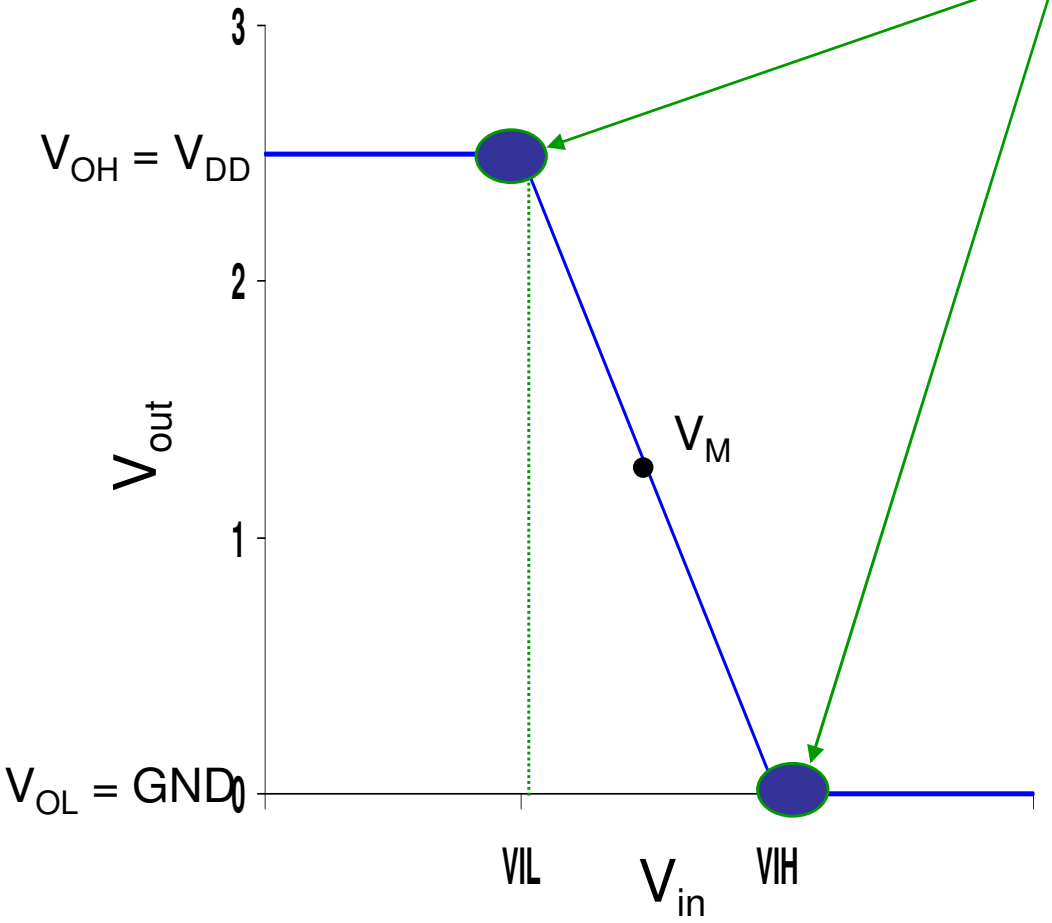
Simulated Inverter V_M



- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}
- Increasing the width of the NMOS moves V_M toward GND
- Small variations in ratio don't make a lot of difference
- To move the VM to 1.5V requires a ratio of 11 !!!



Noise Margins Determining V_{IH} and V_{IL}



A piece-wise linear approximation of VTC

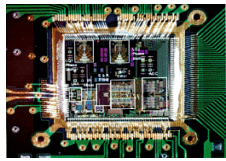
By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL} - GND$

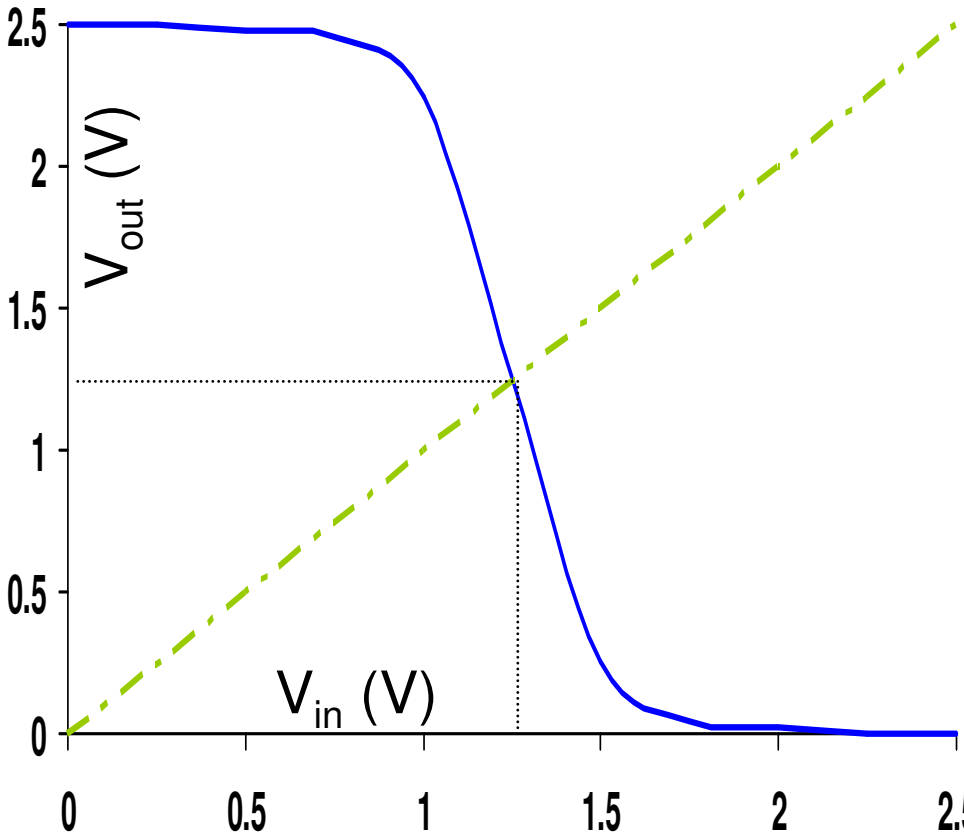
Approximating:

$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

So high gain in the transition region is very desirable



CMOS Inverter VTC from Simulation



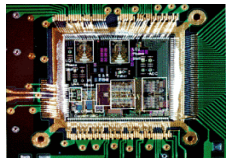
0.25um, $(W/L)_p/(W/L)_n = 3.4$
$(W/L)_n = 1.5$ (min size) $V_{DD} = 2.5V$

$V_M \approx 1.25V$, g = -27.5

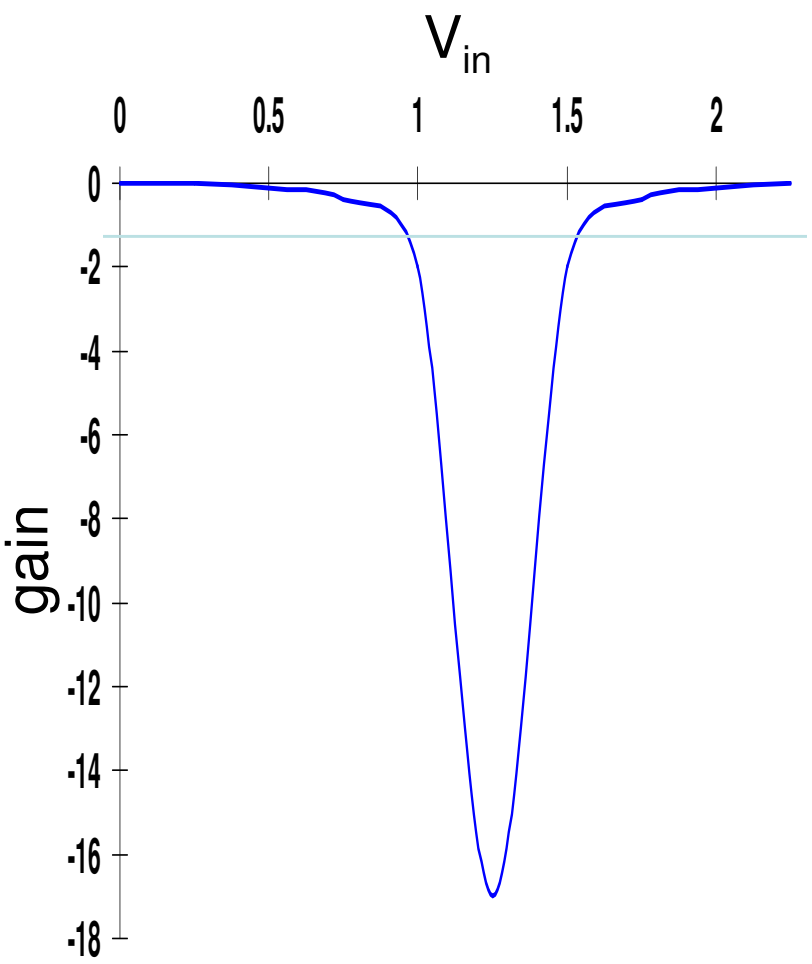
$V_{IL} = 1.2V$, $V_{IH} = 1.3V$
$NM_L = NM_H = 1.2$
(actual values are $V_{IL} = 1.03V$, $V_{IH} = 1.45V$ $NM_L = 1.03V$ & $NM_H = 1.05V$)

Output resistance low-output = 2.4kΩ
high-output = 3.3kΩ

- simulation overestimates the gain, the maximum gain (at VM) is only -17
- piece-wise linear approximation model is optimistic wrt noise margins.
- Low output resistance is a good measure of the sensitivity of the gate wrt noise induced at the output and should be as low as possible.



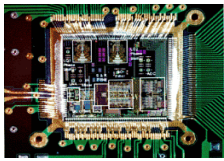
Gain Determinates



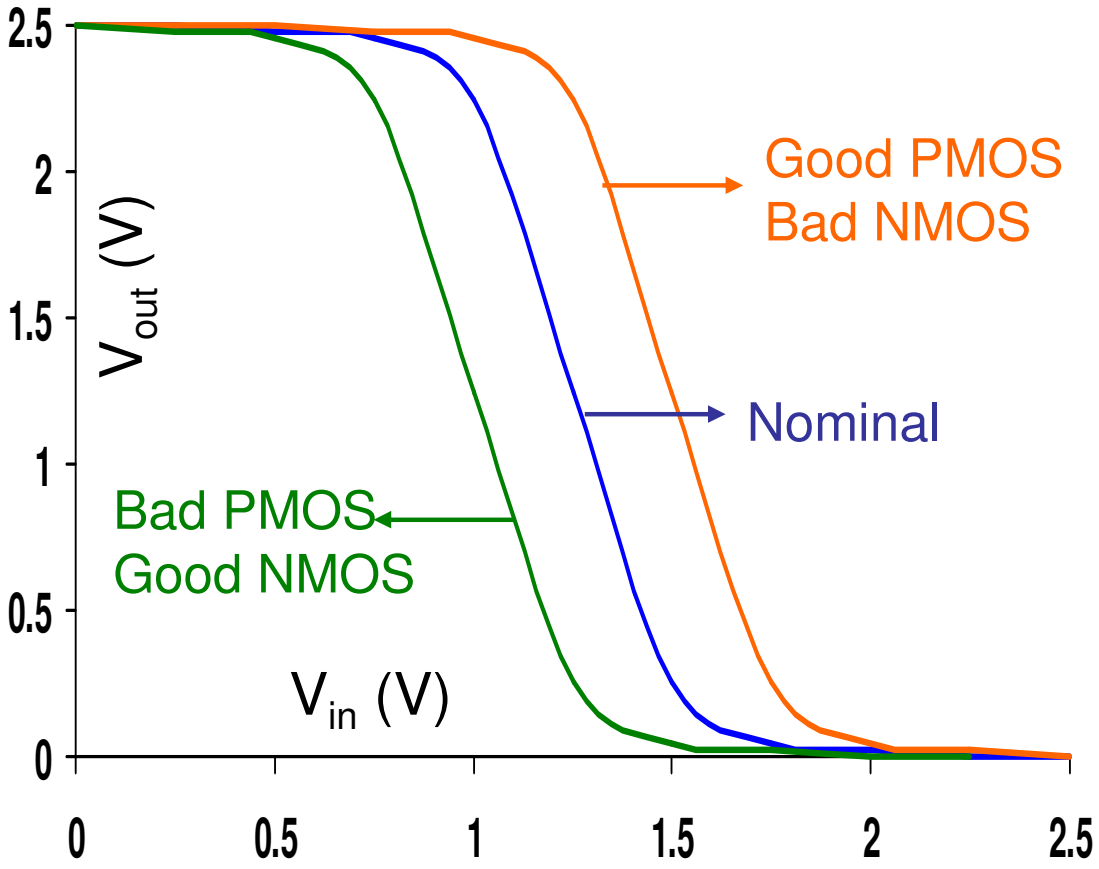
Gain is a strong function of the slopes of the currents in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

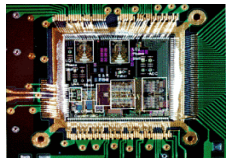
Determined by technology parameters, especially channel length modulation (λ). Only designer influence through supply voltage and V_M (transistor sizing).



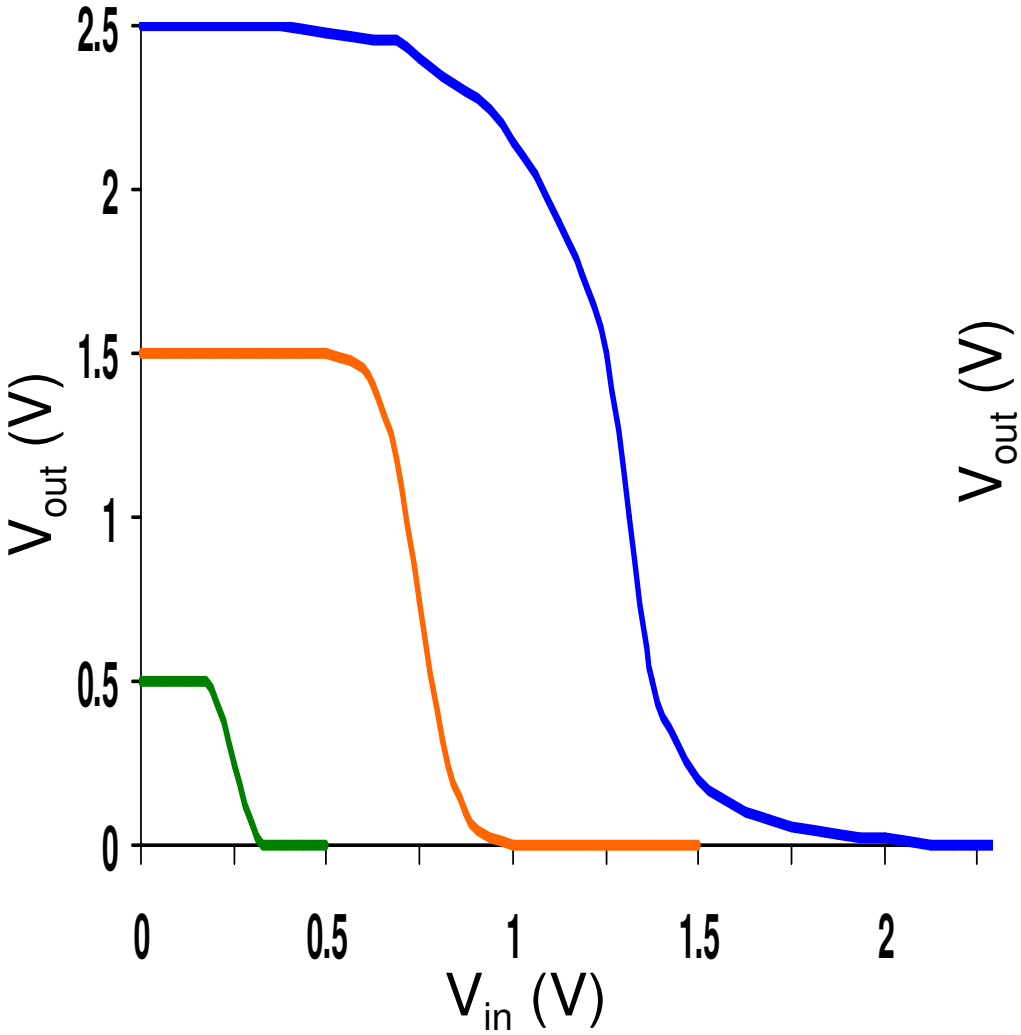
Impact of Process Variation on VTC



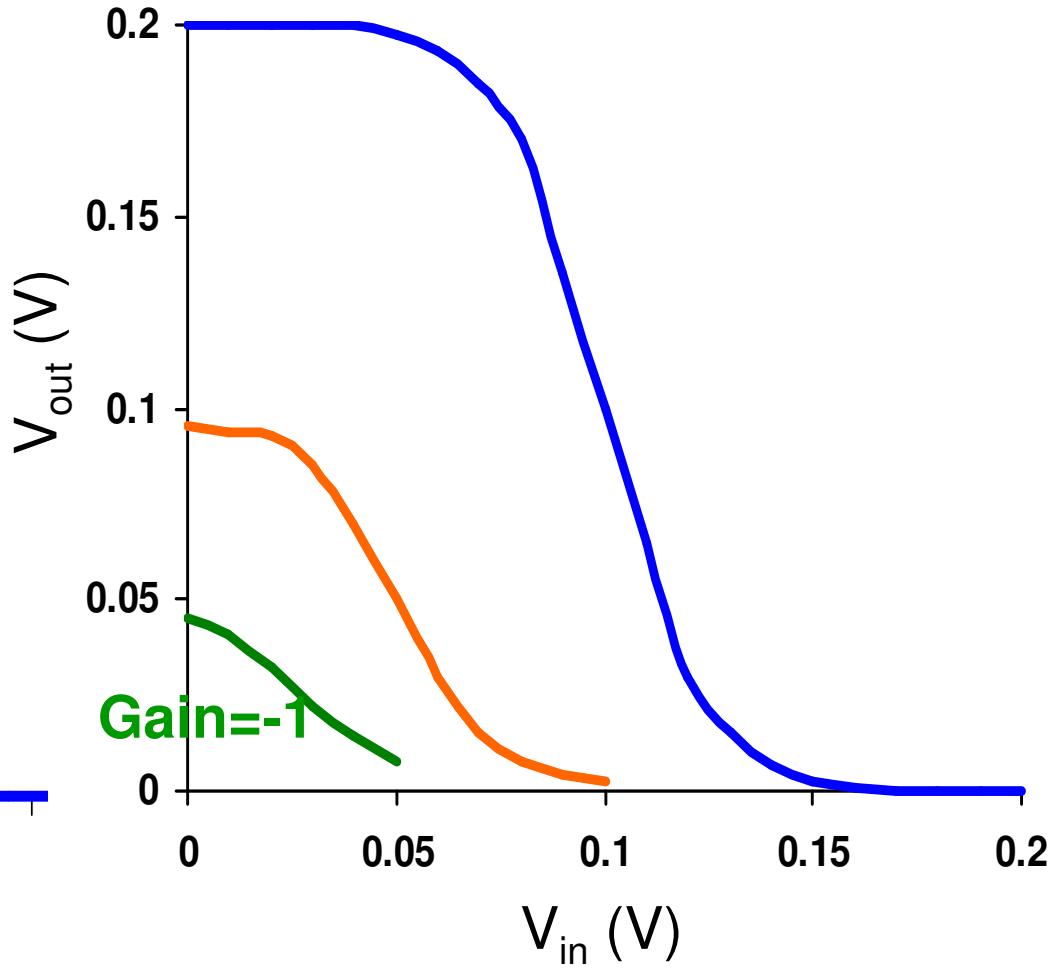
- Process variations (mostly) cause a shift in the switching threshold
- A good device has a small oxide thickness (-3nm), a small length (-25nm), a higher width (+30nm) and a smaller threshold (-60mV). The opposite is true for a bad device.



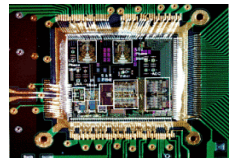
Scaling the Supply Voltage



Device threshold voltages are kept (virtually) constant



Device threshold voltages are kept (virtually) constant



Scaling the Supply Voltage

Observations

- Gain of the inverter in the transition region increases with a reduction in Vdd. For a fixed r, VM is proportional to Vdd.
- At a voltage of 0.5V (just 100mV above the threshold of the transistors) the width of the transition region measures only 10% of the supply voltage (and a gain of -35), while it widens to 17% for 2.5V

But, reducing the supply

- Is absolutely detrimental to the performance of the gate
- The dc characteristics become increasingly sensitive to variations in the device parameters (e.g., VT)
- Scaling the supply means reduced signal swing making the gate more sensitive to external noise sources

Note, in plot on the right, we still obtain an inverter even though the supply voltage is not large enough to turn the transistors on! The subthreshold current is sufficient to switch the gate between low and high levels, as well as to provide enough gain to produce an acceptable VTC.

- The ultimate show stopper is when the gain in the transition region approaches 1 (as in the green curve on the right plot) – giving the true lower bound on supply scaling (without cooling the chip).