CSCE 5730: Digital CMOS VLSI Design

Assignment 1, Assigned Dated: 13th Sep 2007 (Thu), Due Date: 20th Sep 2007 (Thu)
Instructor: Dr. Saraju P. Mohanty

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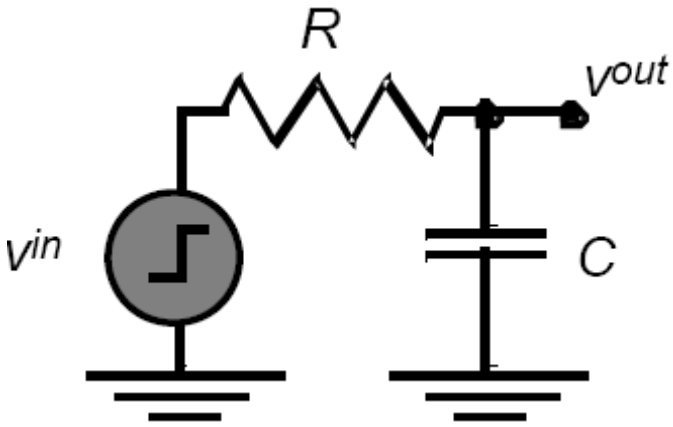
1. Assume a wafer size of 15 inches, a die size of 3.5 cm^2, 1.2 defects/cm^2, and α=3. Determine the die yield of this CMOS process run.
2. Consider the following RC circuit.



Find the transient response of the circuit for output voltage. What is the time to reach 50% point? What is the time to reach 90% point?