Lecture 5: Manufacturing

CSCE 5730
Digital CMOS VLSI Design

Instructor: Saraju P. Mohanty, Ph. D.

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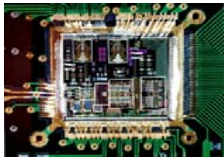
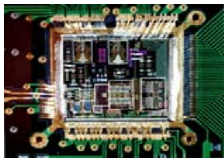


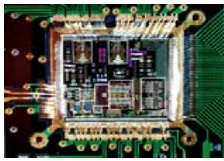
Lecture Outline

- CMOS Fabrication
- Packaging
- Testing

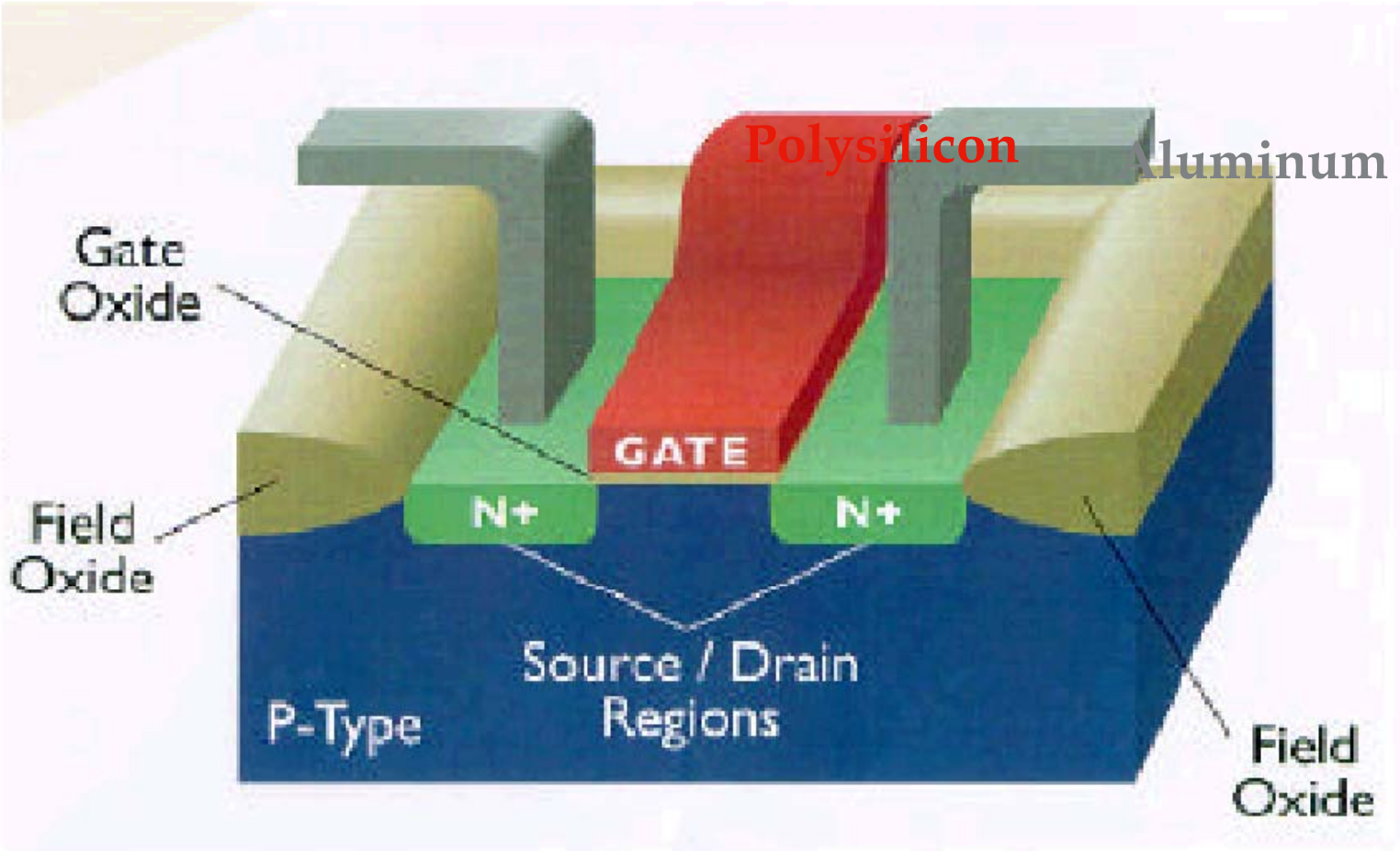


Introduction

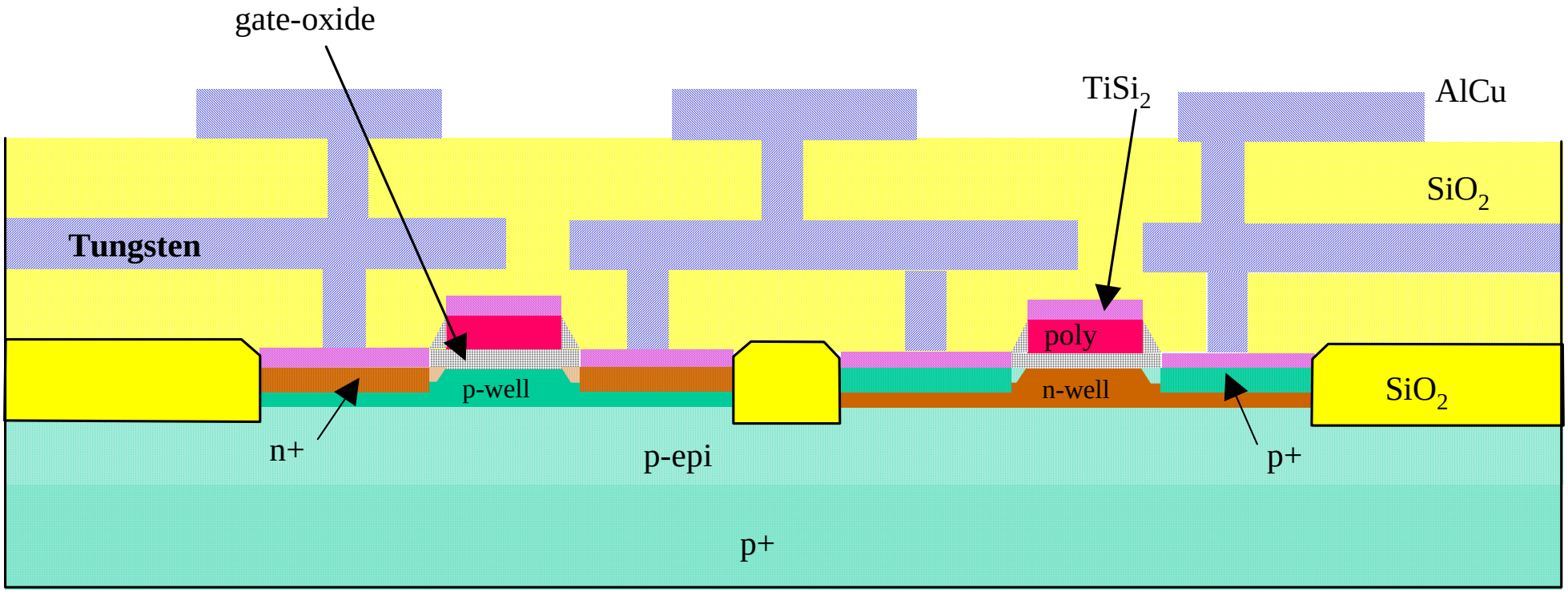
- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication



MOSFET: 3D Perspective

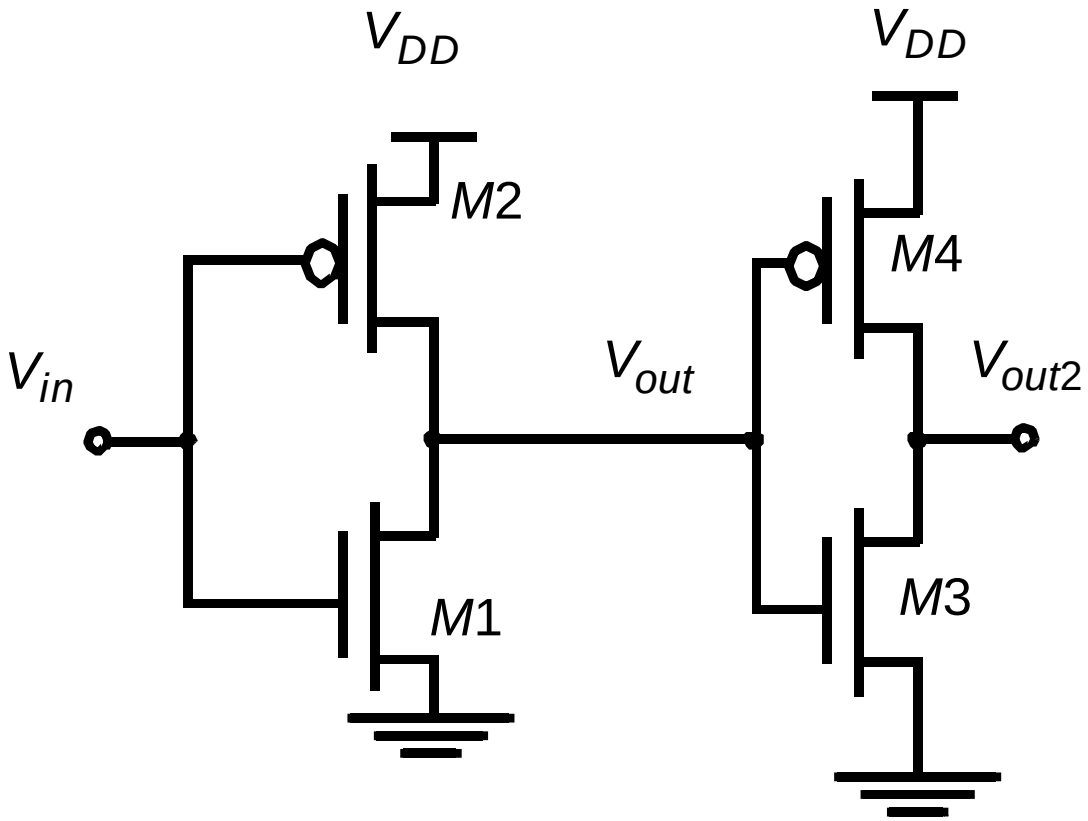


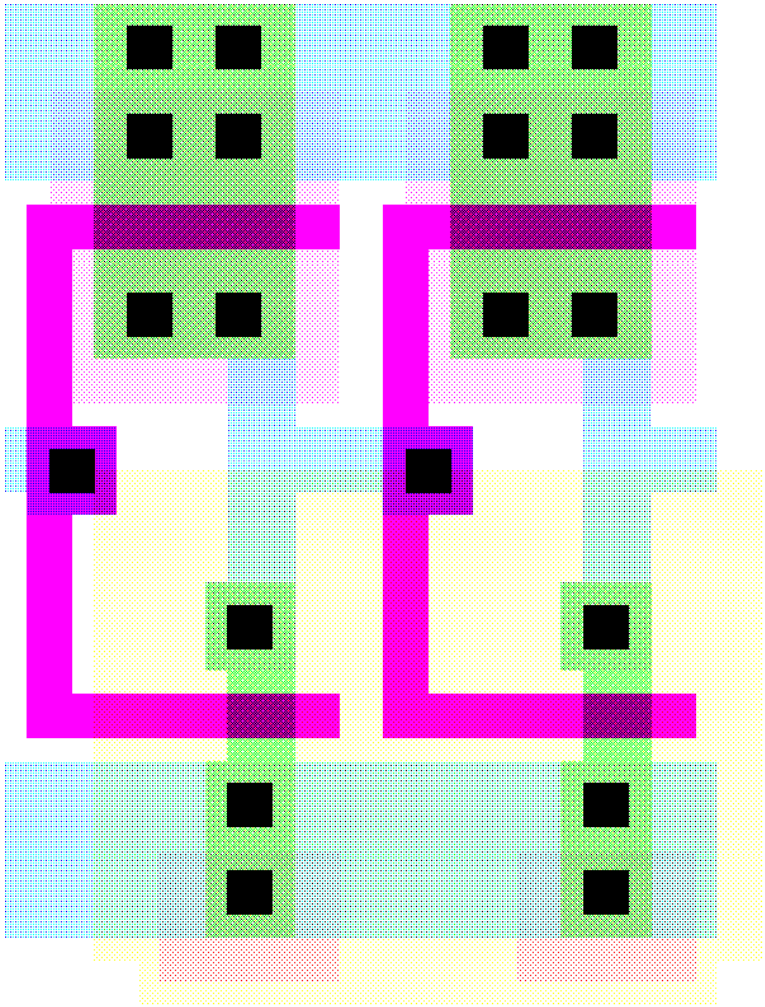
A Modern CMOS Process

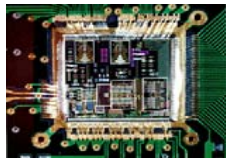


Dual-Well Trench-Isolated CMOS Process

Circuit Under Design and Its Layout







CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer.
- Lithography process similar to printing press is used for the fabrication.
- On each step, different materials are deposited or etched.
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process.

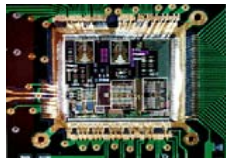
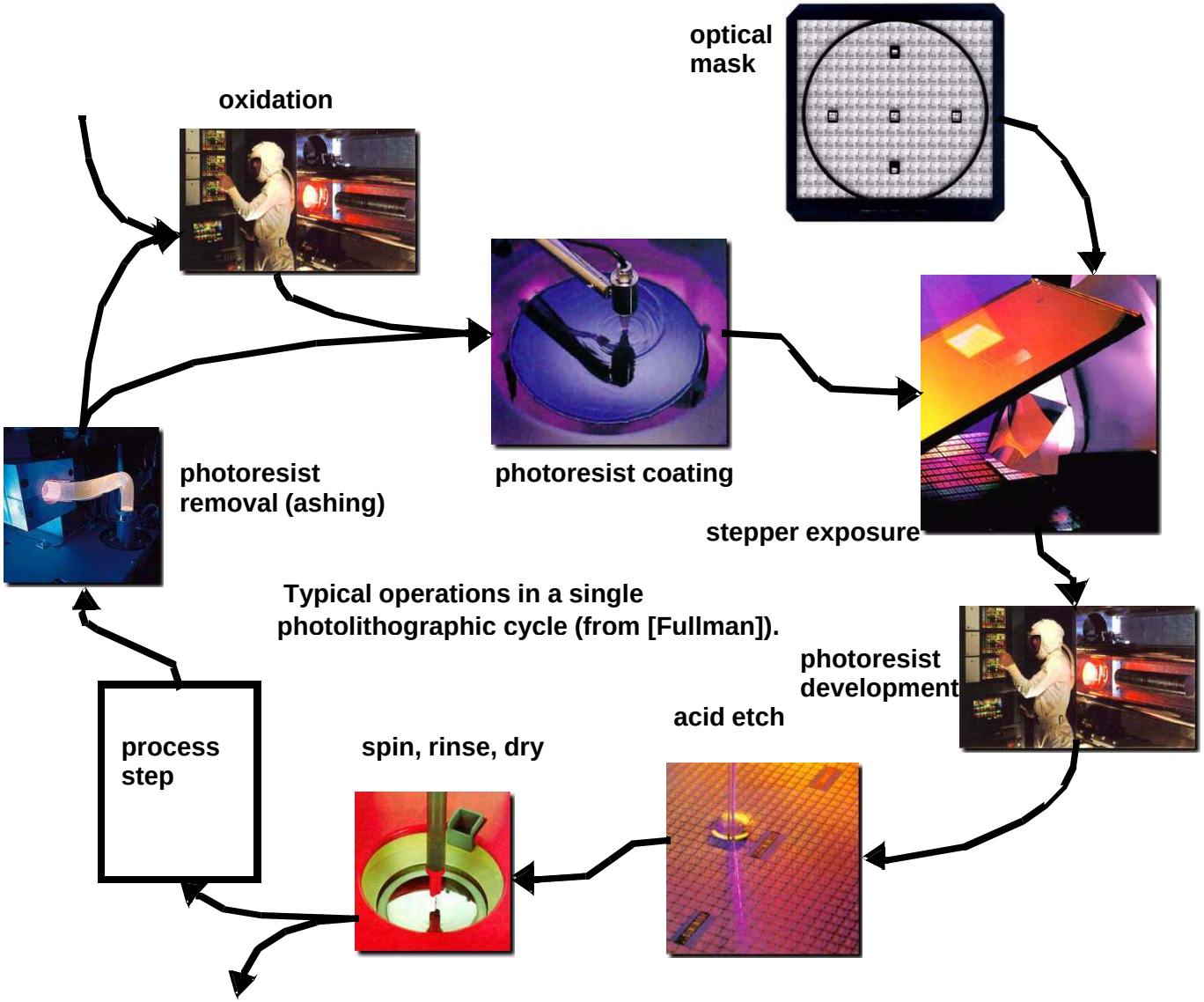
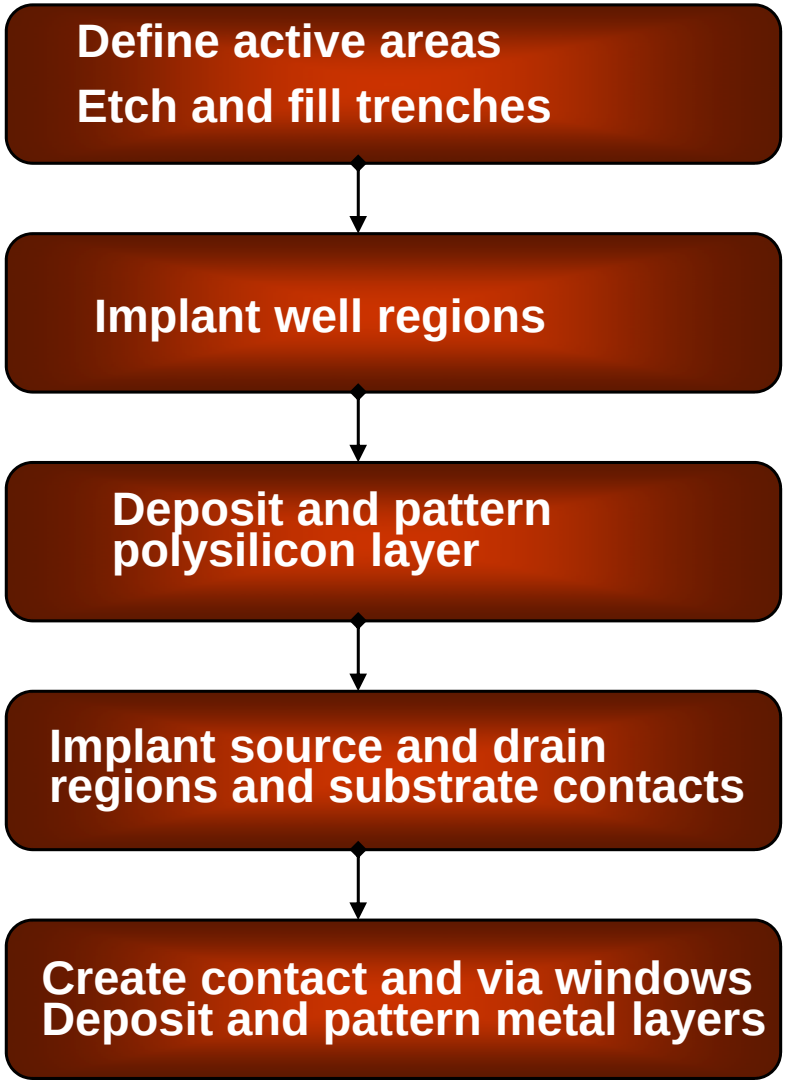


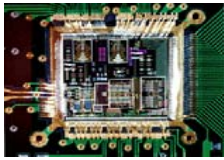
Photo-Lithographic Process



Typical operations in a single photolithographic cycle (from [Fullman]).

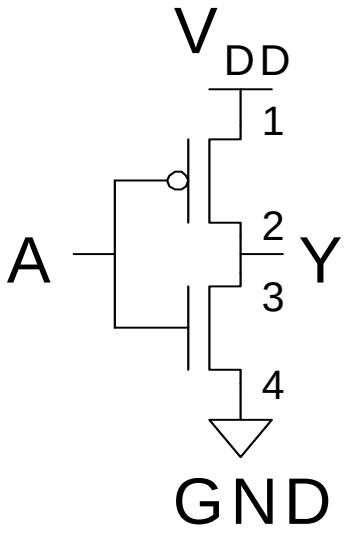
CMOS Process at a Glance

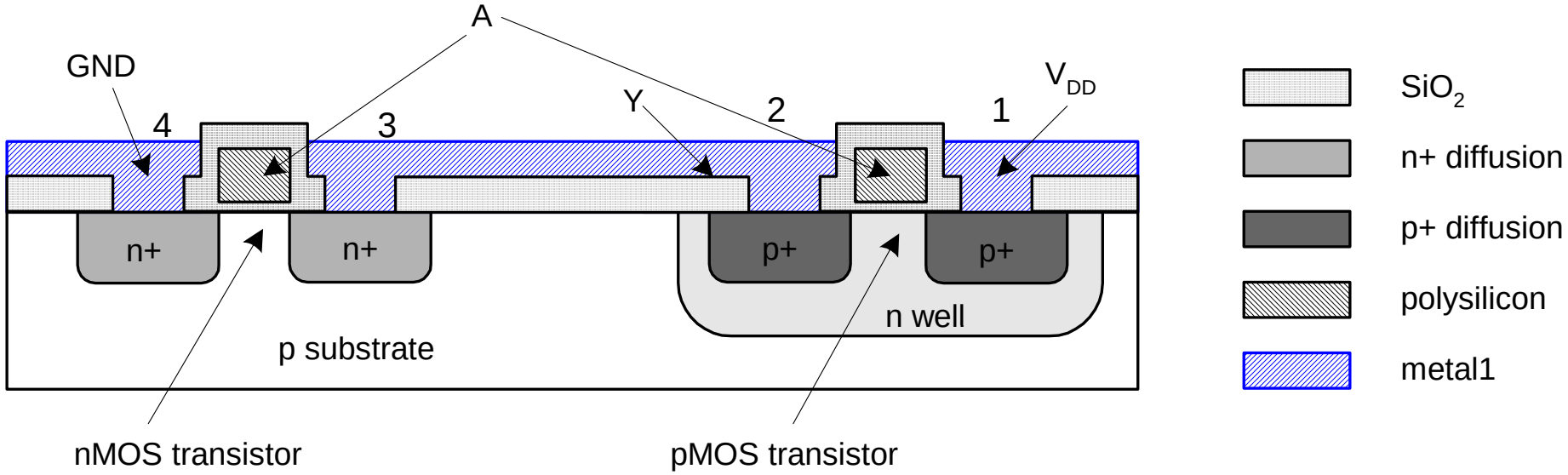




Inverter Cross-section

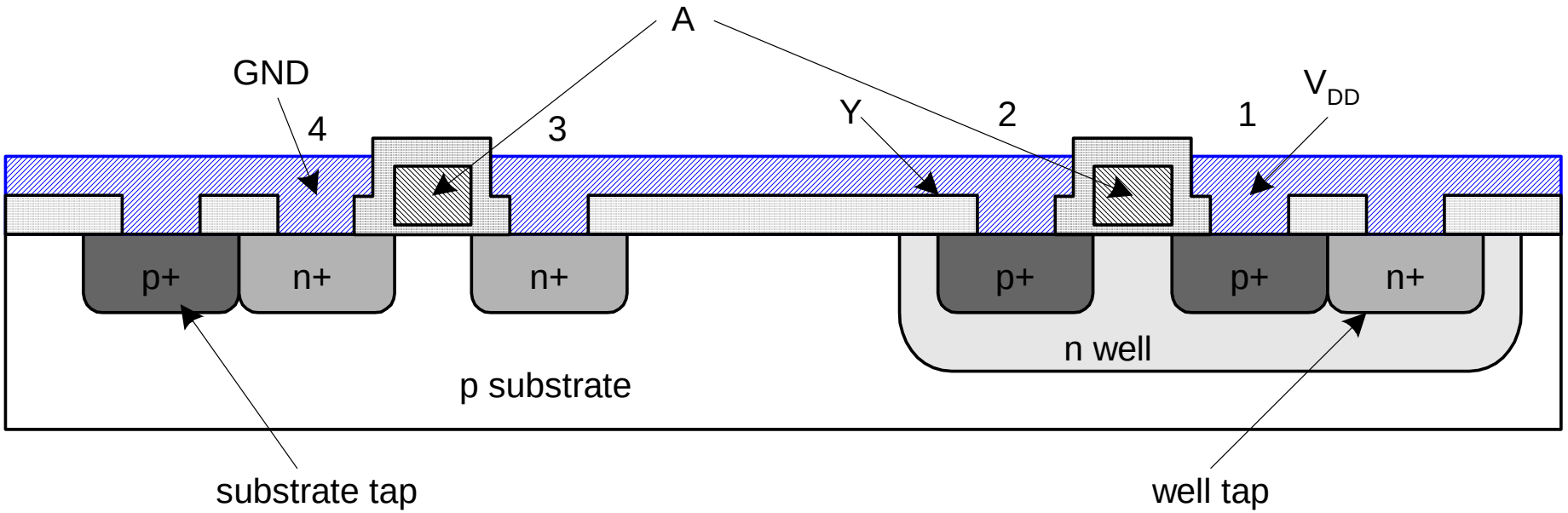
- Typically use p-type substrate for nMOS transistors.
- Requires n-well for body of pMOS transistors.





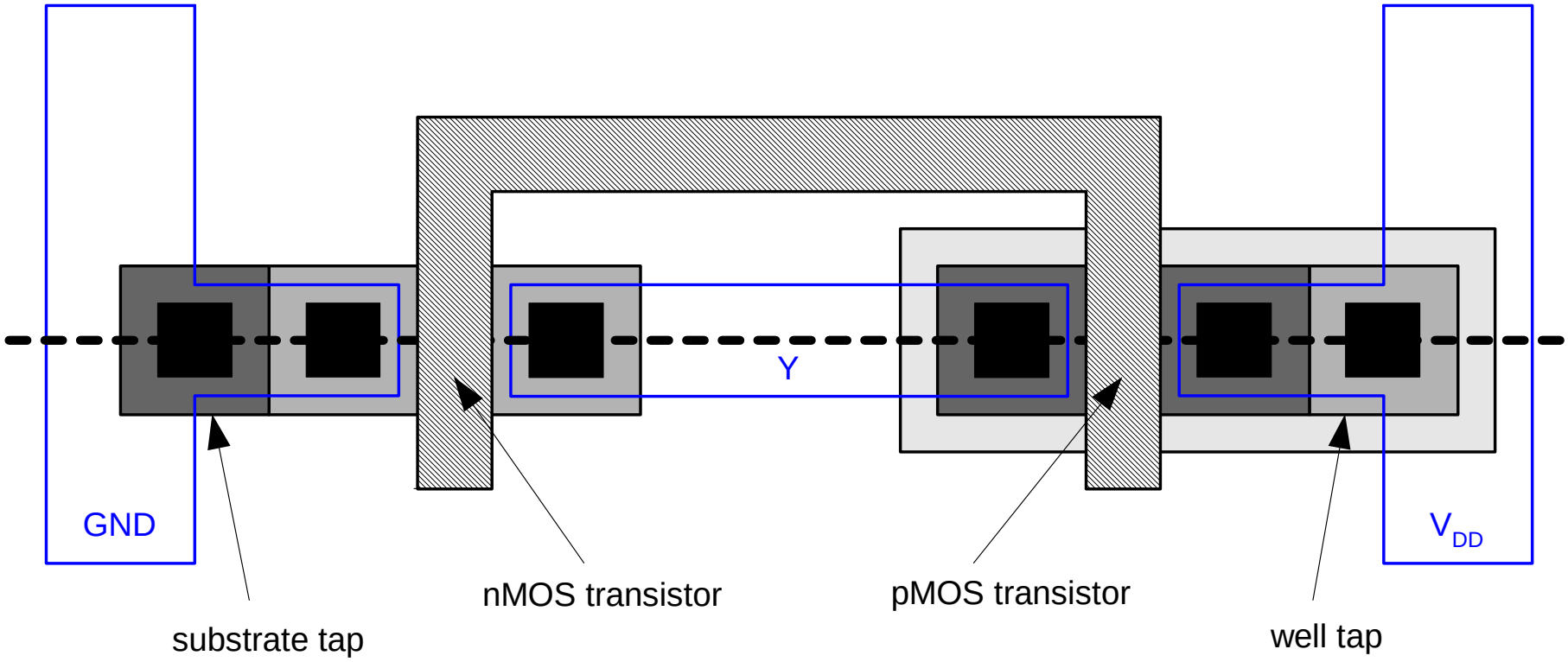
Well and Substrate Taps

- Substrate must is tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Heavily doped well and substrate contacts or taps form good ohmic contacts.



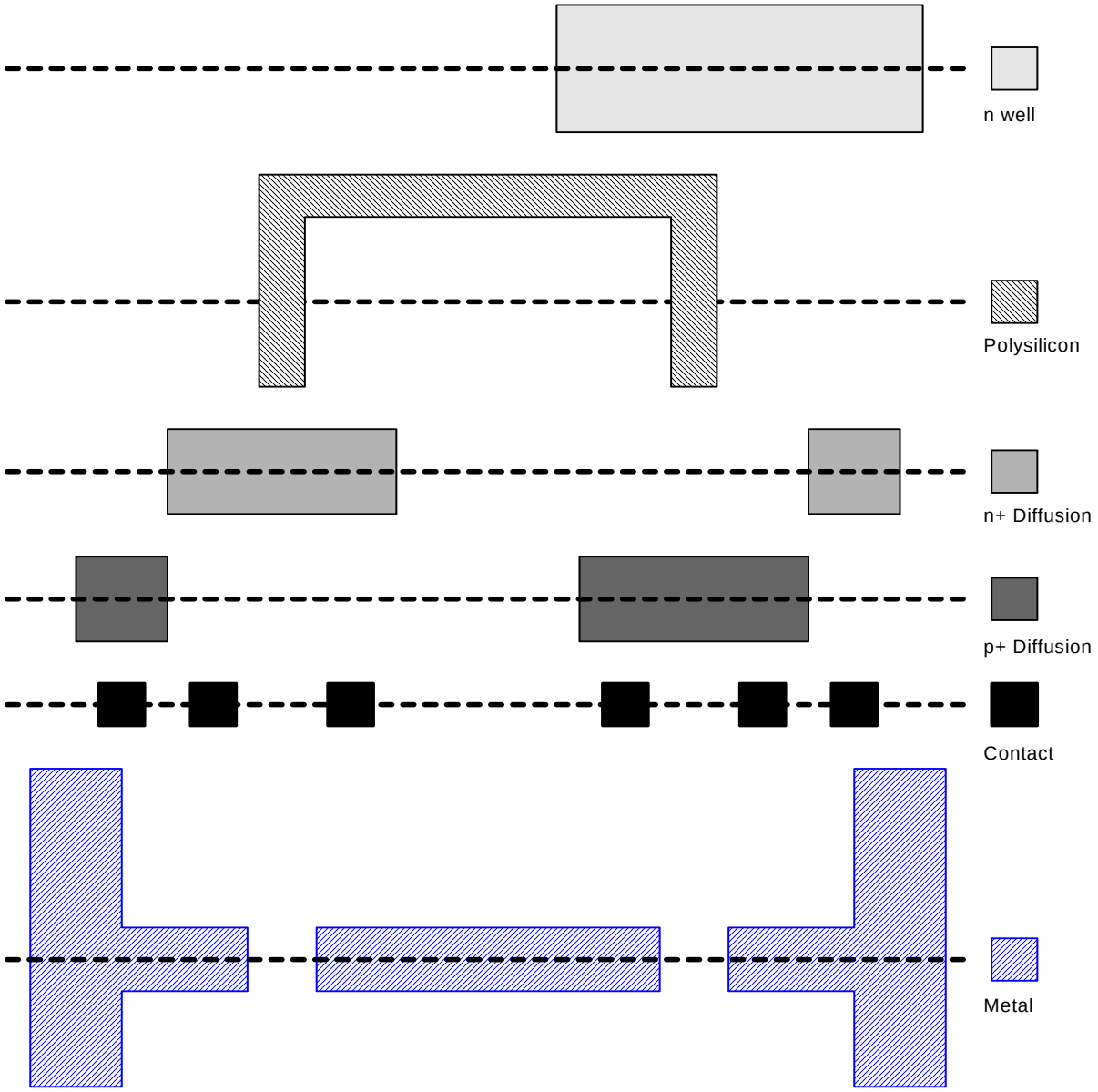
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



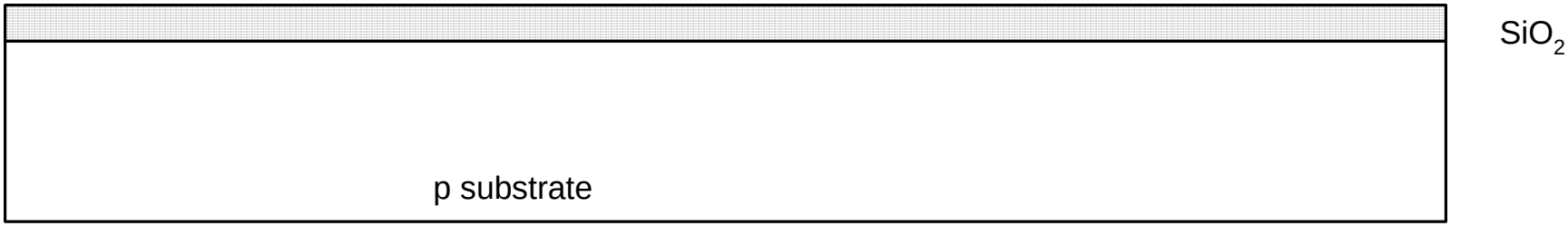
Fabrication Steps: Creation of n-well

- Objective is to build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

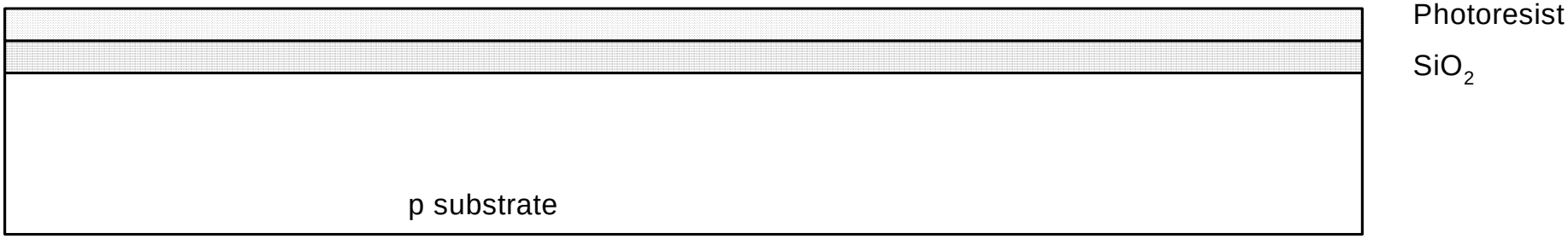
- n-well : Start with blank p-type silicon wafer

Fabrication Steps: Creation of n-well

- n-well: Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace
  - The oxide is patterned to define n-well.

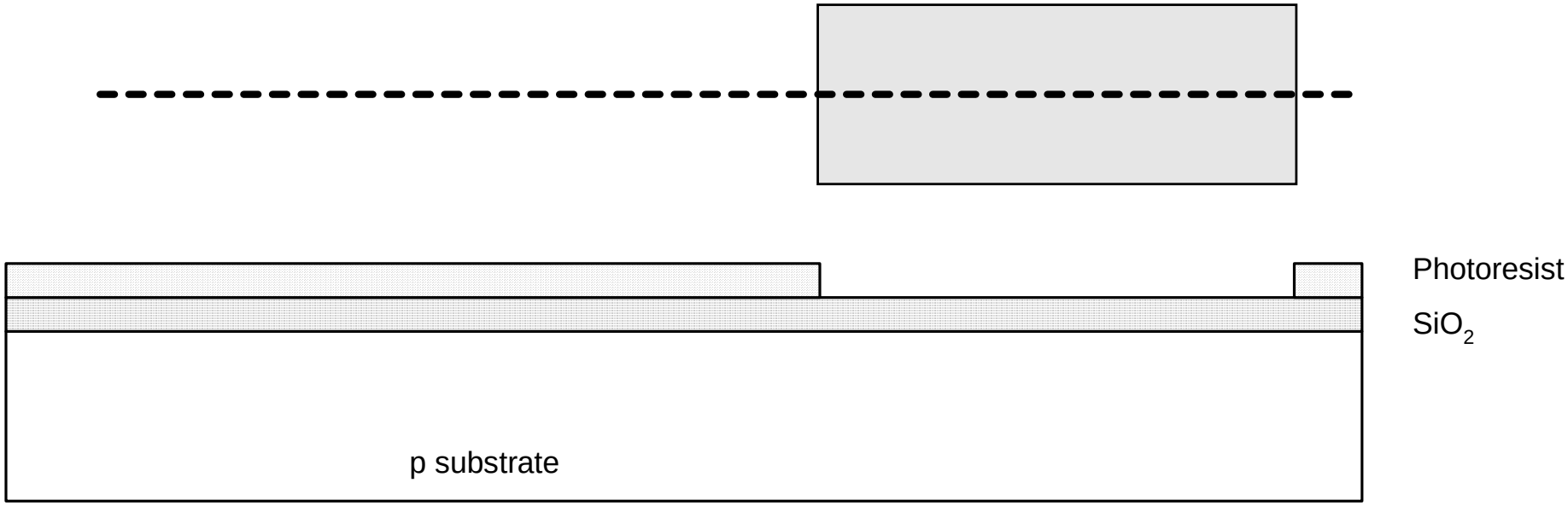


- n-well: Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



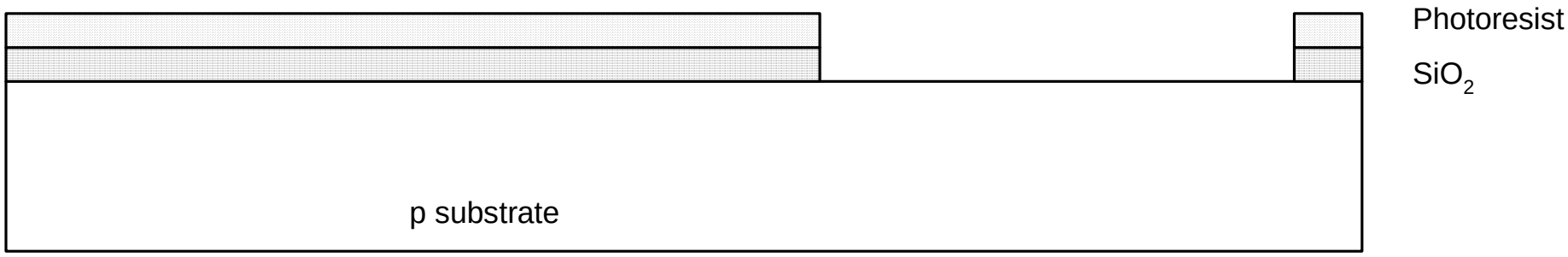
Fabrication Steps: Creation of n-well

- n-well: Expose photoresist through n-well mask
  - Allows light to pass through only where the n-well need to be created.
  - Strip off exposed photoresist

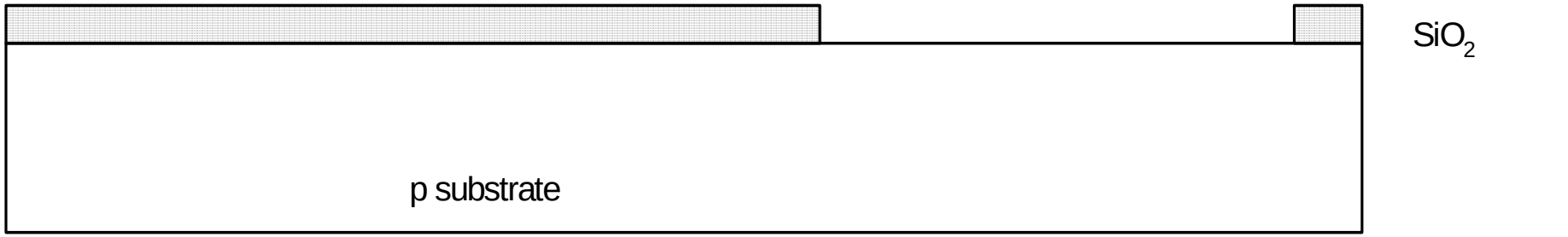


Fabrication Steps: Creation of n-well

- n-well: Etch oxide with hydrofluoric acid (HF)
  - Only attacks oxide where resist has been exposed

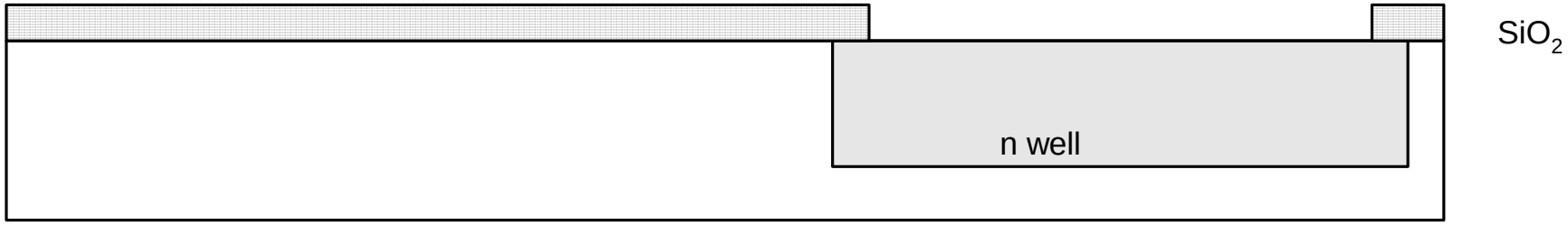


- n-well: Strip off remaining photoresist
  - Use mixture of acids called piranah etch
  - Necessary so resist doesn't melt in next step

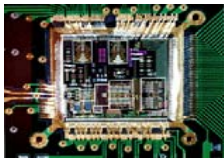


Fabrication Steps: Creation of n-well

- n-well: created with diffusion or ion implantation
  - Diffusion: Place wafer in furnace with arsenic gas and heat until As atoms diffuse into exposed Si
  - Ion Implantation: Blast wafer with beam of As ions

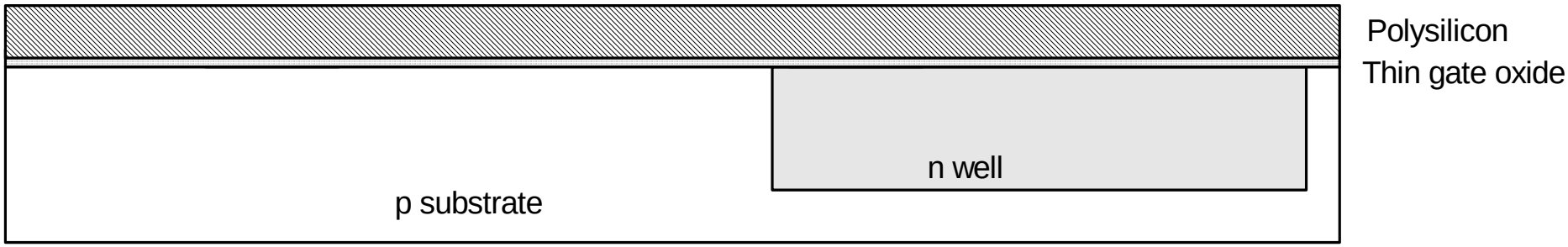


- n-well: Strip off the remaining oxide using HF
  - Back to bare wafer with n-well
  - Subsequent steps involve similar series of steps



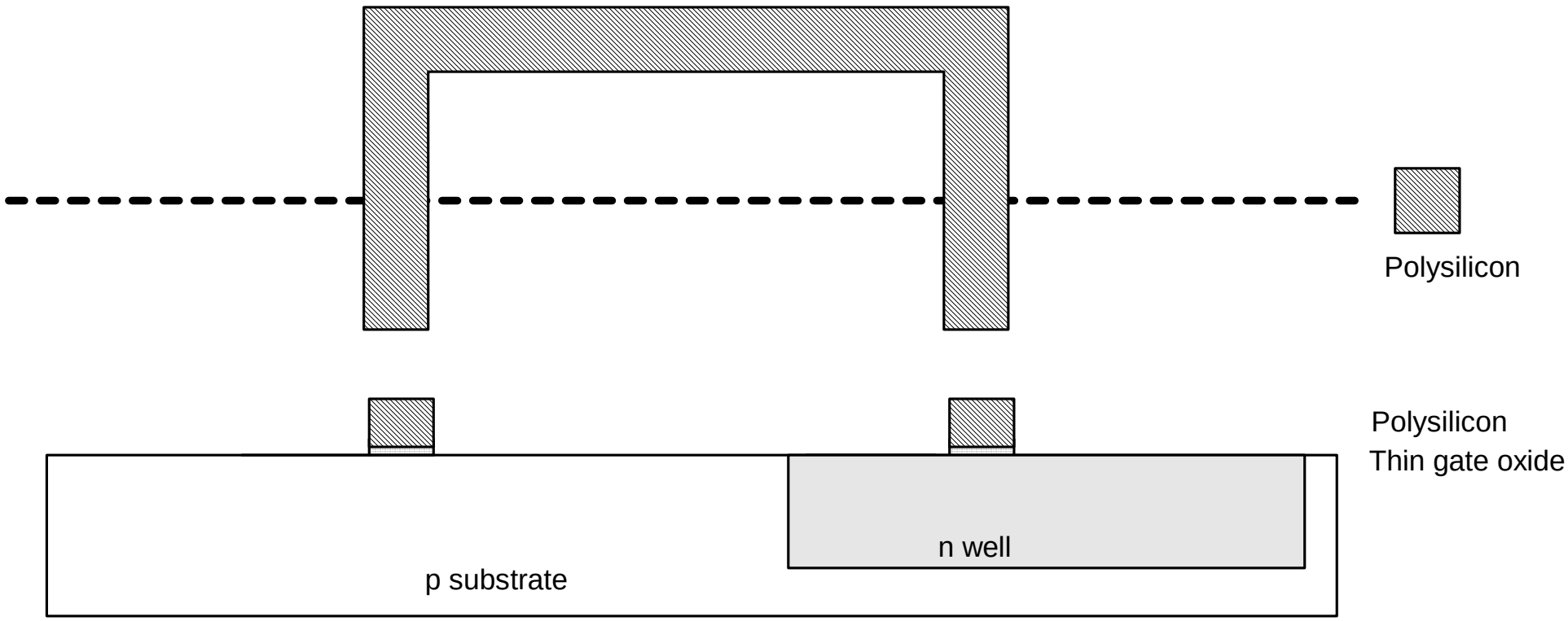
Fabrication Steps: Creation of Gates

- Gate consists of polysilicon over thin layer of silicon oxide.
- Very thin layer of gate oxide is grown in furnace
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer for polysilicon deposition
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Polysilicon is heavily doped to be a good conductor



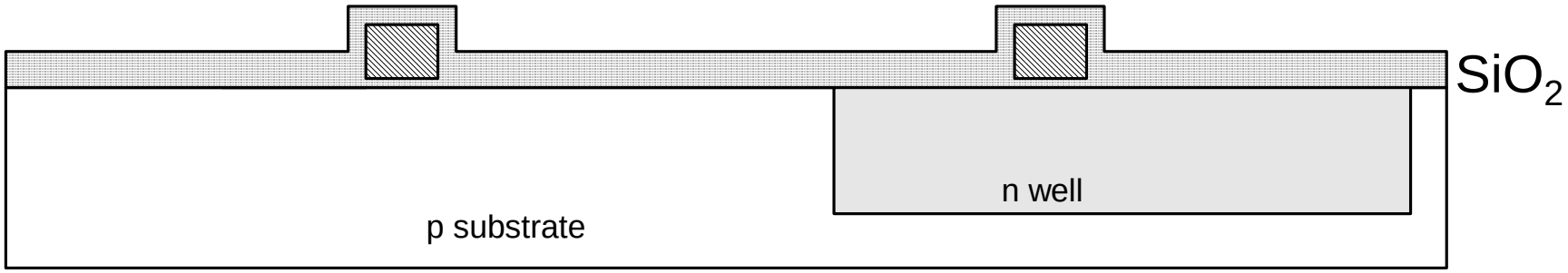
Fabrication Steps: Creation of Gates

- Use same lithography process that used to create n-well to pattern polysilicon using photoresist and the polysilicon mask.



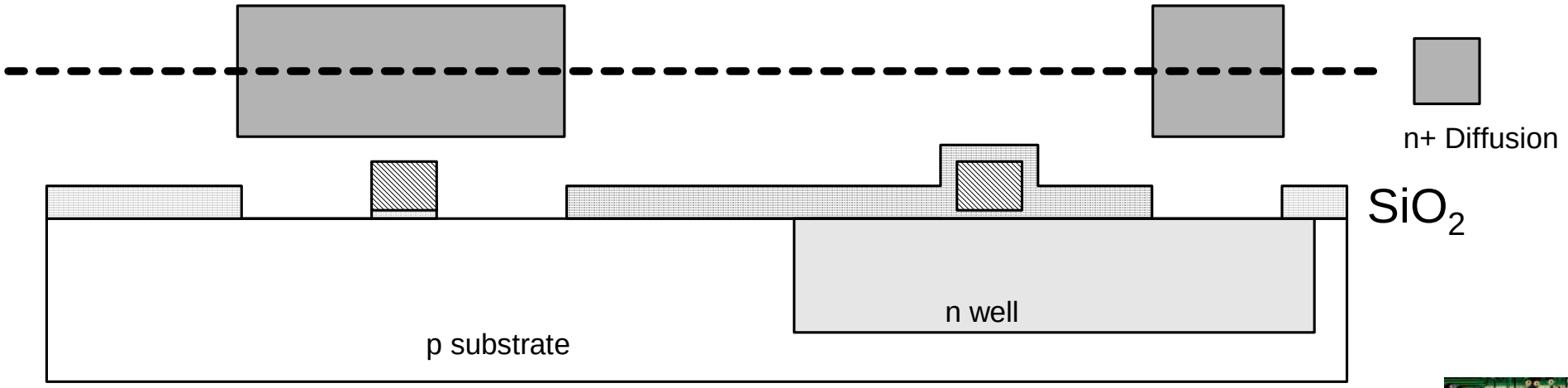
Fabrication Steps: Creation of n+

- Transistor active area and well contact are n+.
- N-diffusion forms nMOS source, drain, and n-well contact
- Use oxide and masking to expose where n+ dopants should be diffused or implanted



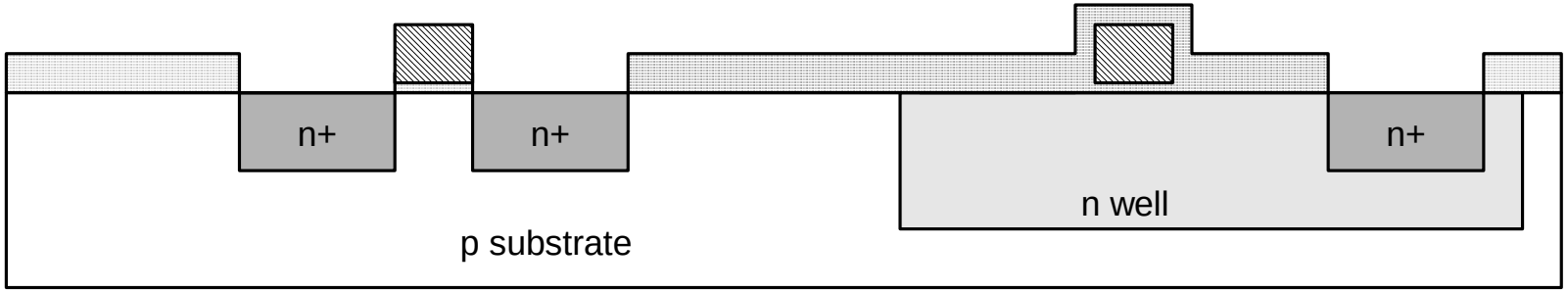
Fabrication Steps: Creation of n+

- Pattern oxide with the n-diffusion mask and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing

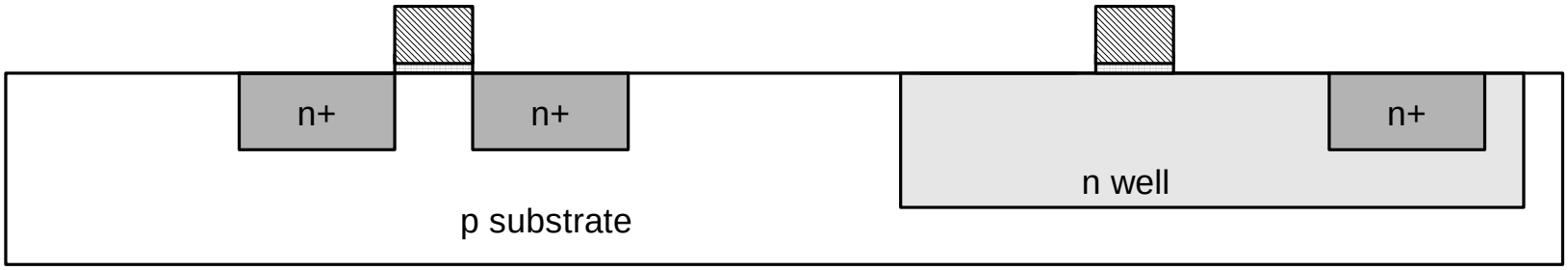


Fabrication Steps: Creation of n+

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

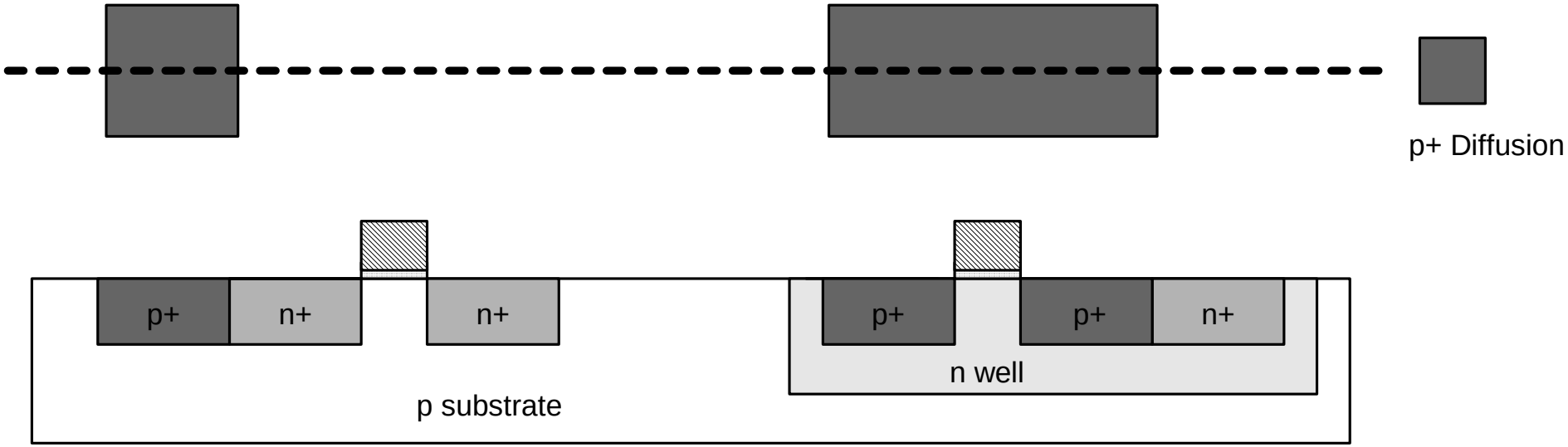


- Strip off oxide to complete patterning step



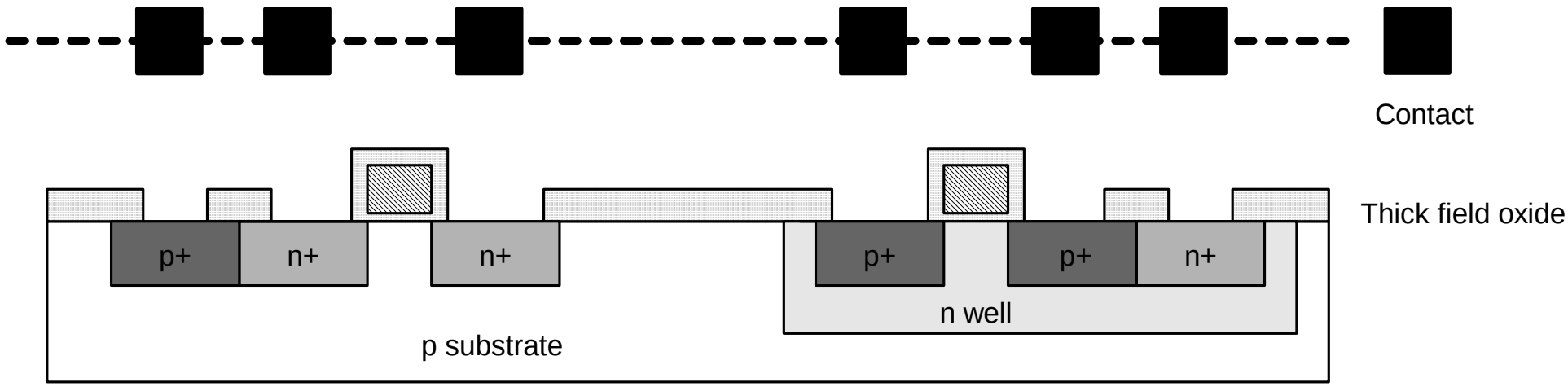
Fabrication Steps: Creation of p+

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact
- Pattern oxide with the p-diffusion mask and form p+ regions



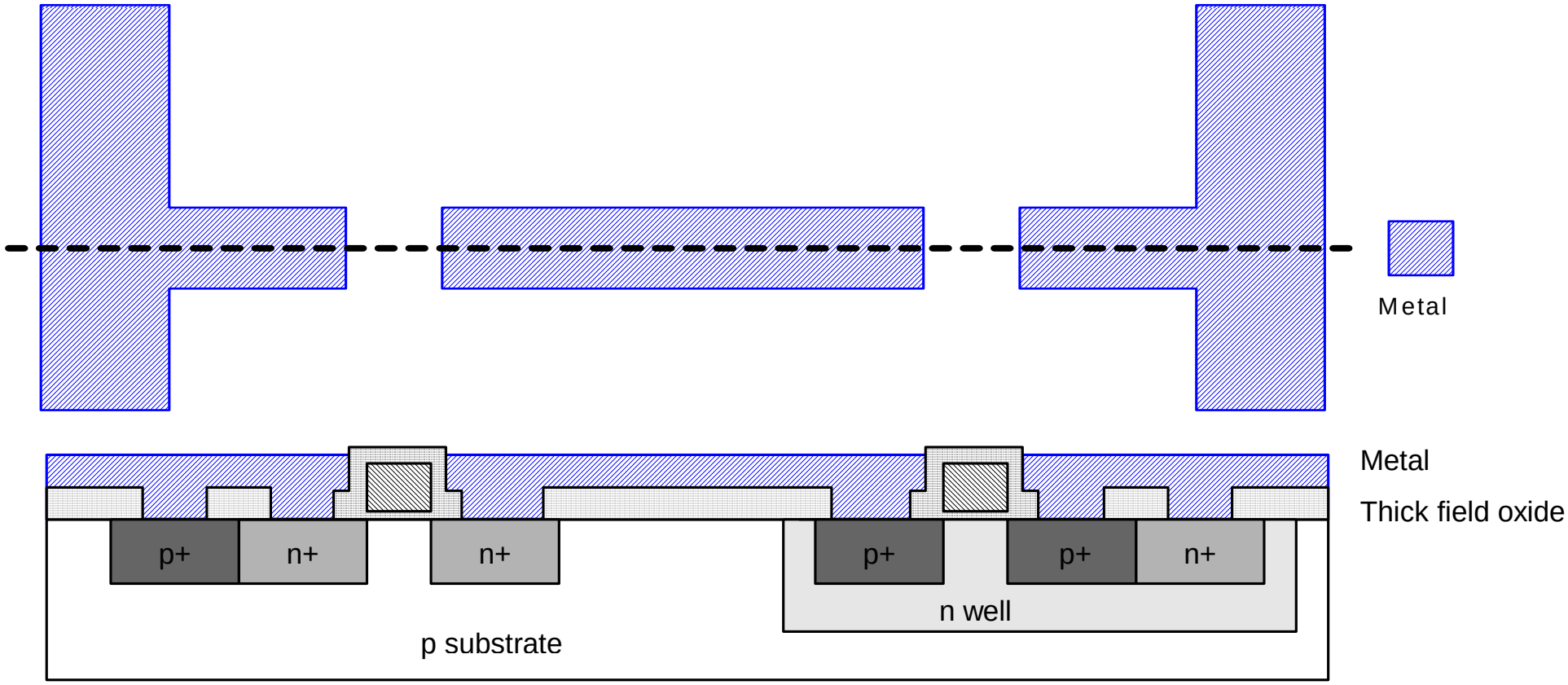
Fabrication Steps: Creation of Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed using contact mask.

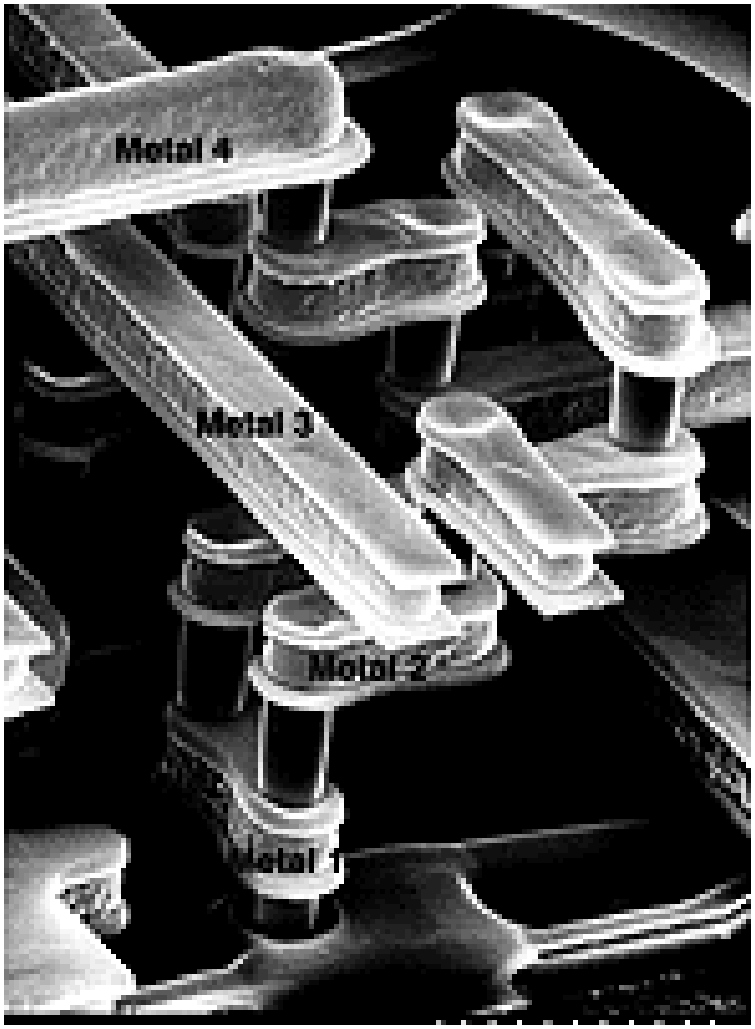


Fabrication Steps: Metalization

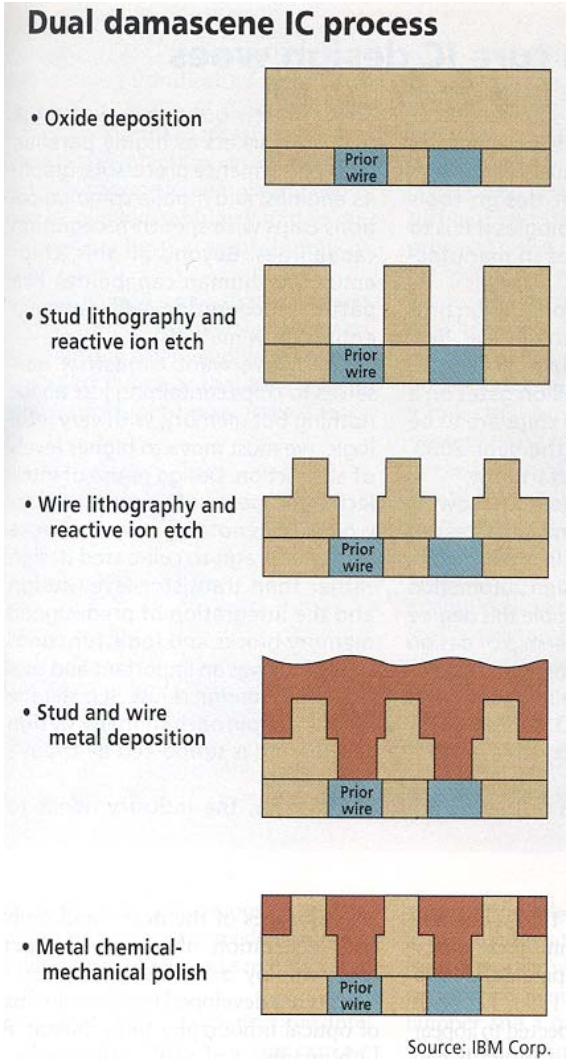
- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires
- Metal mask is used during this step.

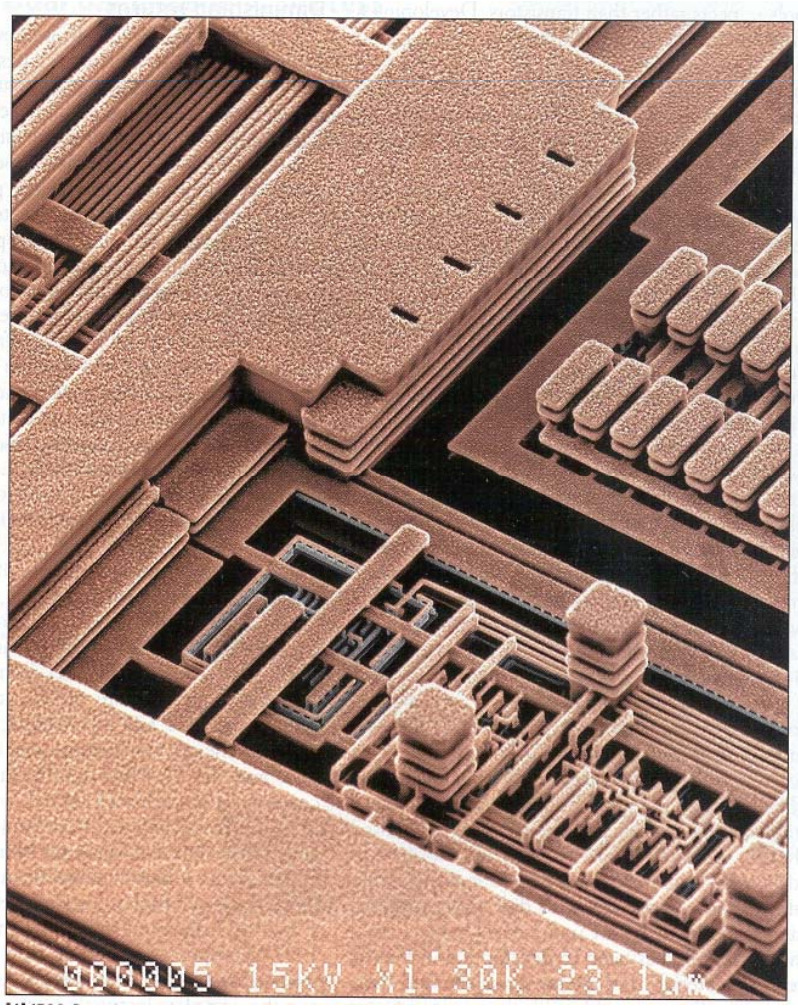


Advanced Metallization



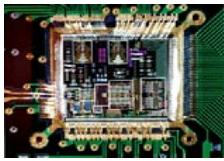
Advanced Metallization





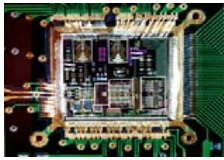
Layout Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)



Layout Design Rules

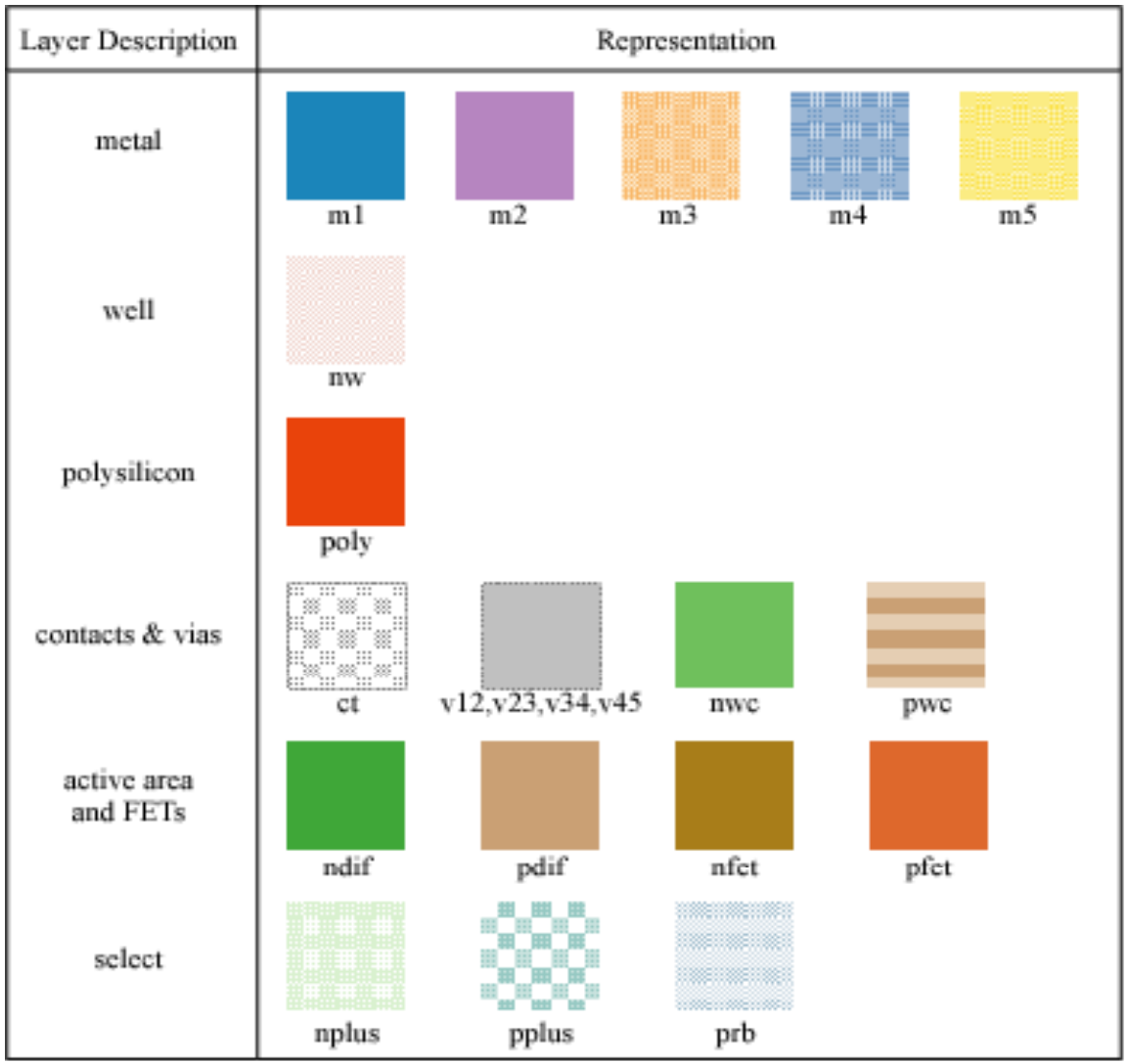
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - e.g. λ = 60 nm in 120 nm process

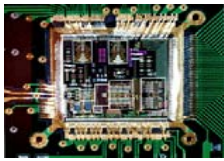


CMOS Process Layers

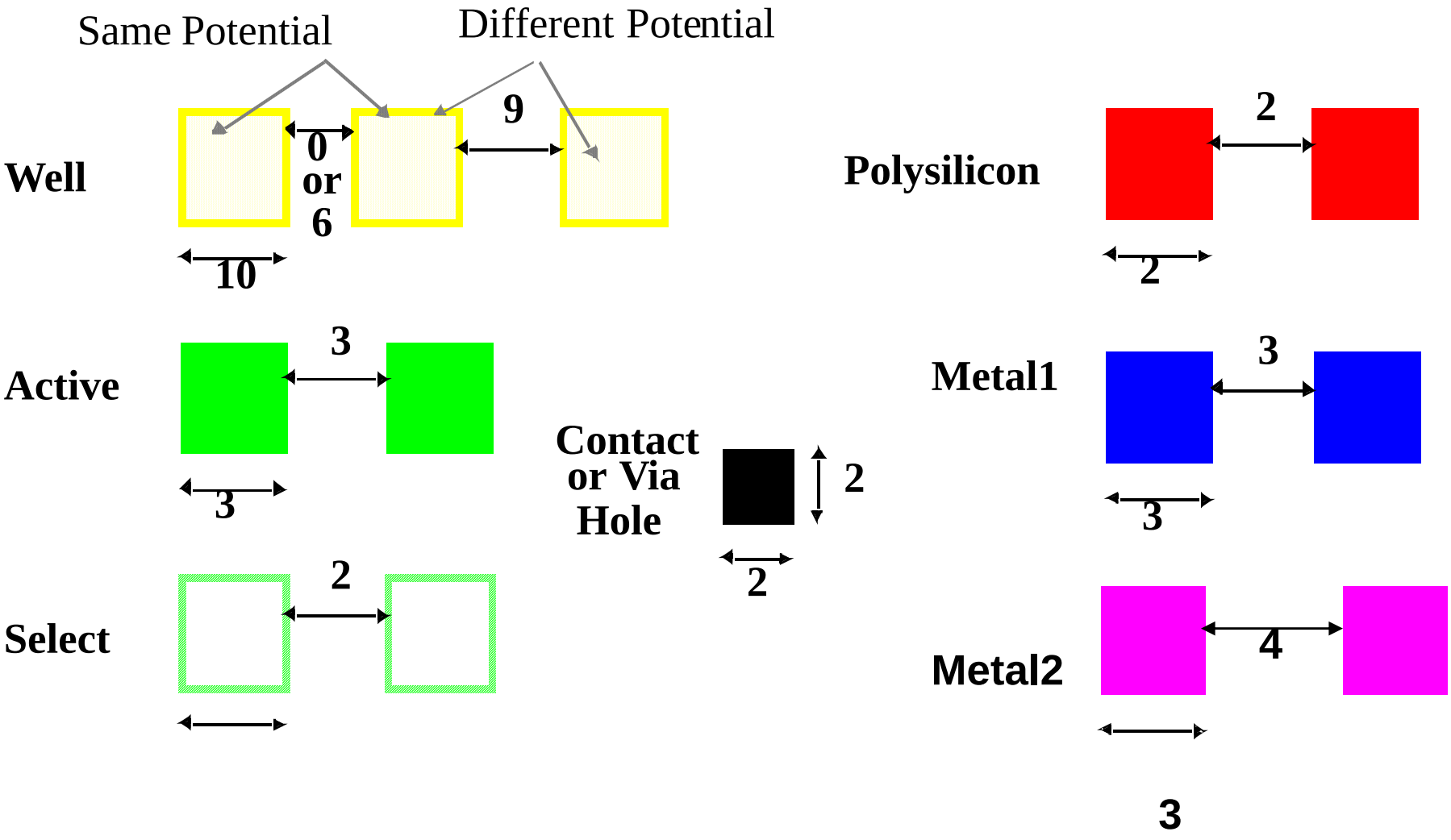
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process

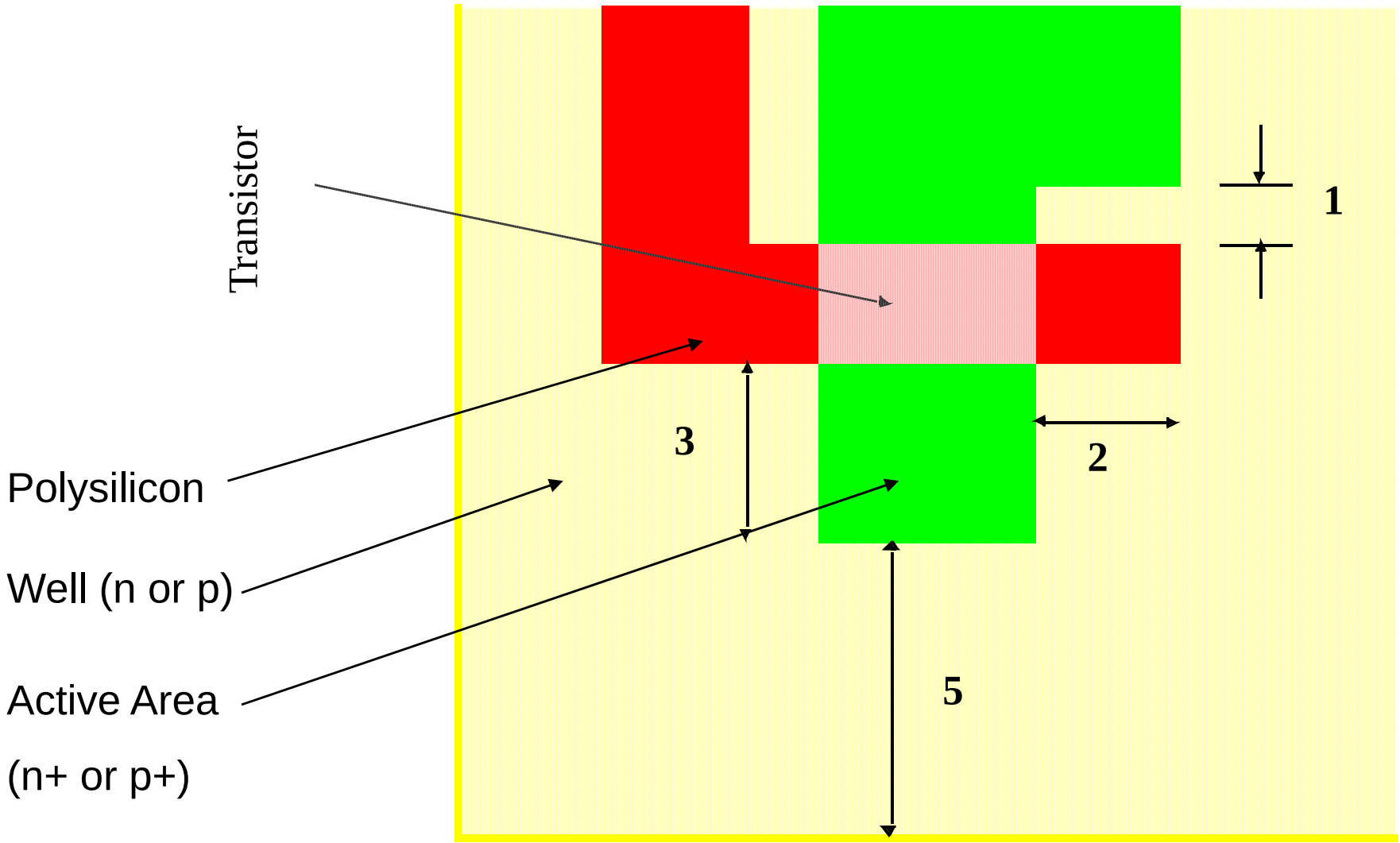




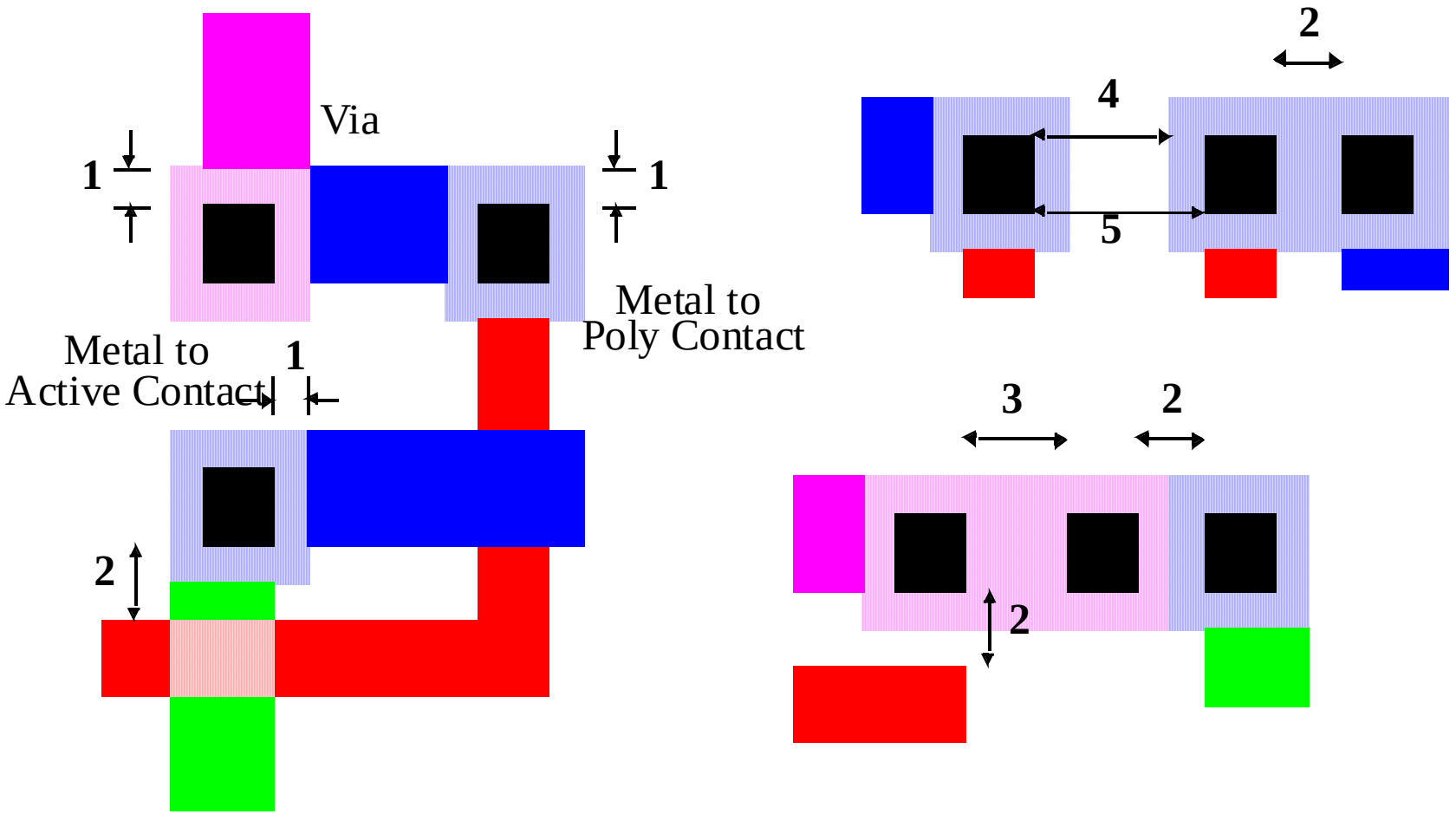
Intra-Layer Design Rules



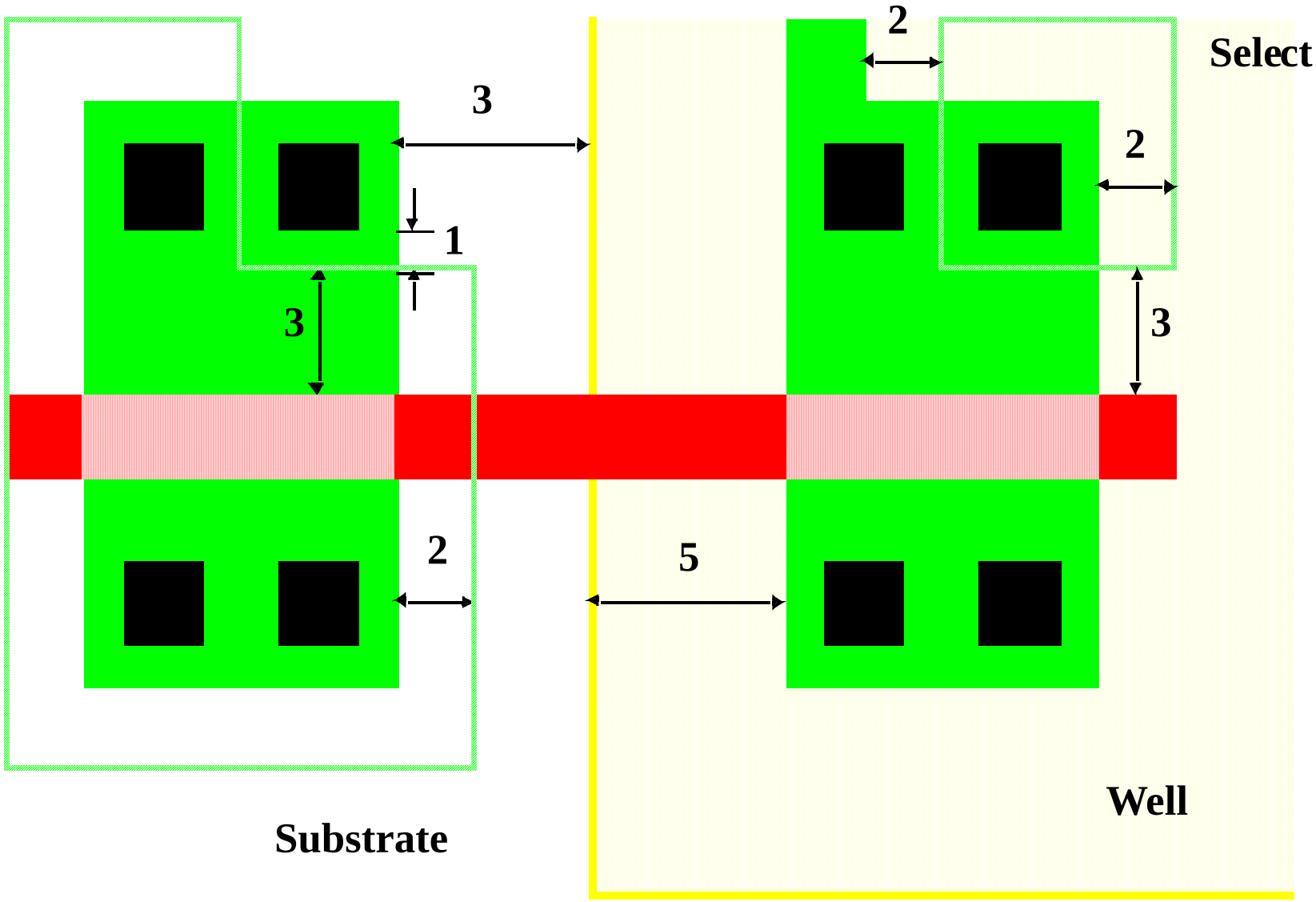
Transistor Layout



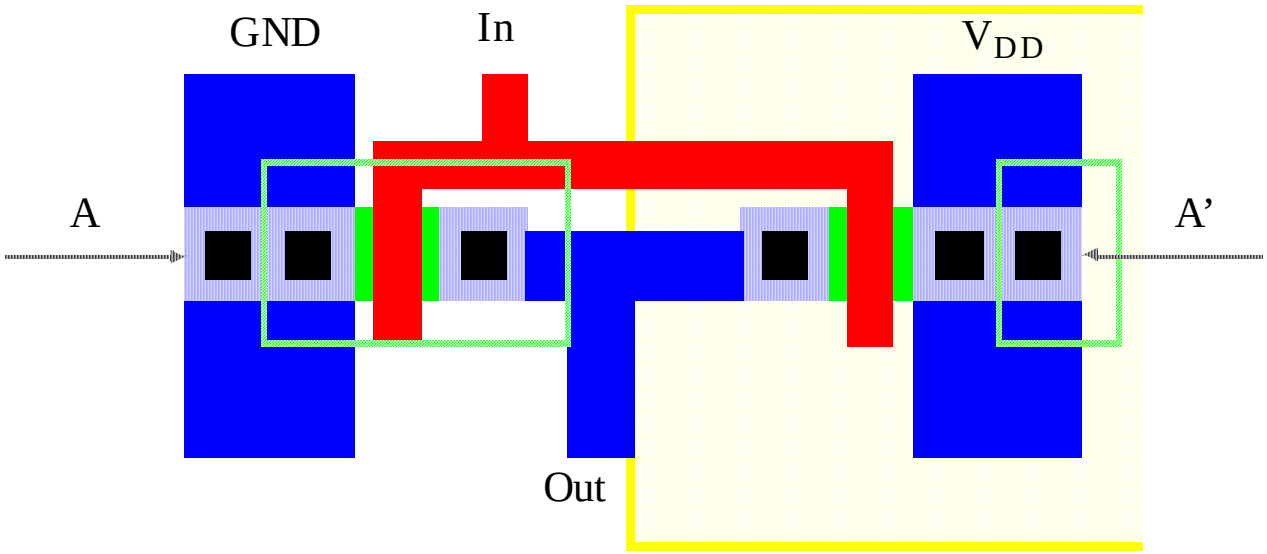
Vias and Contacts



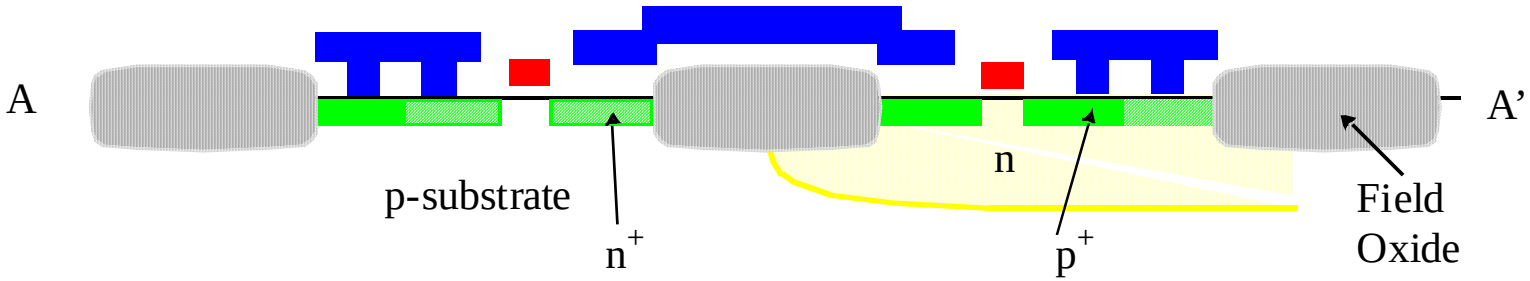
Select Layer



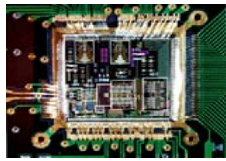
CMOS Inverter Layout



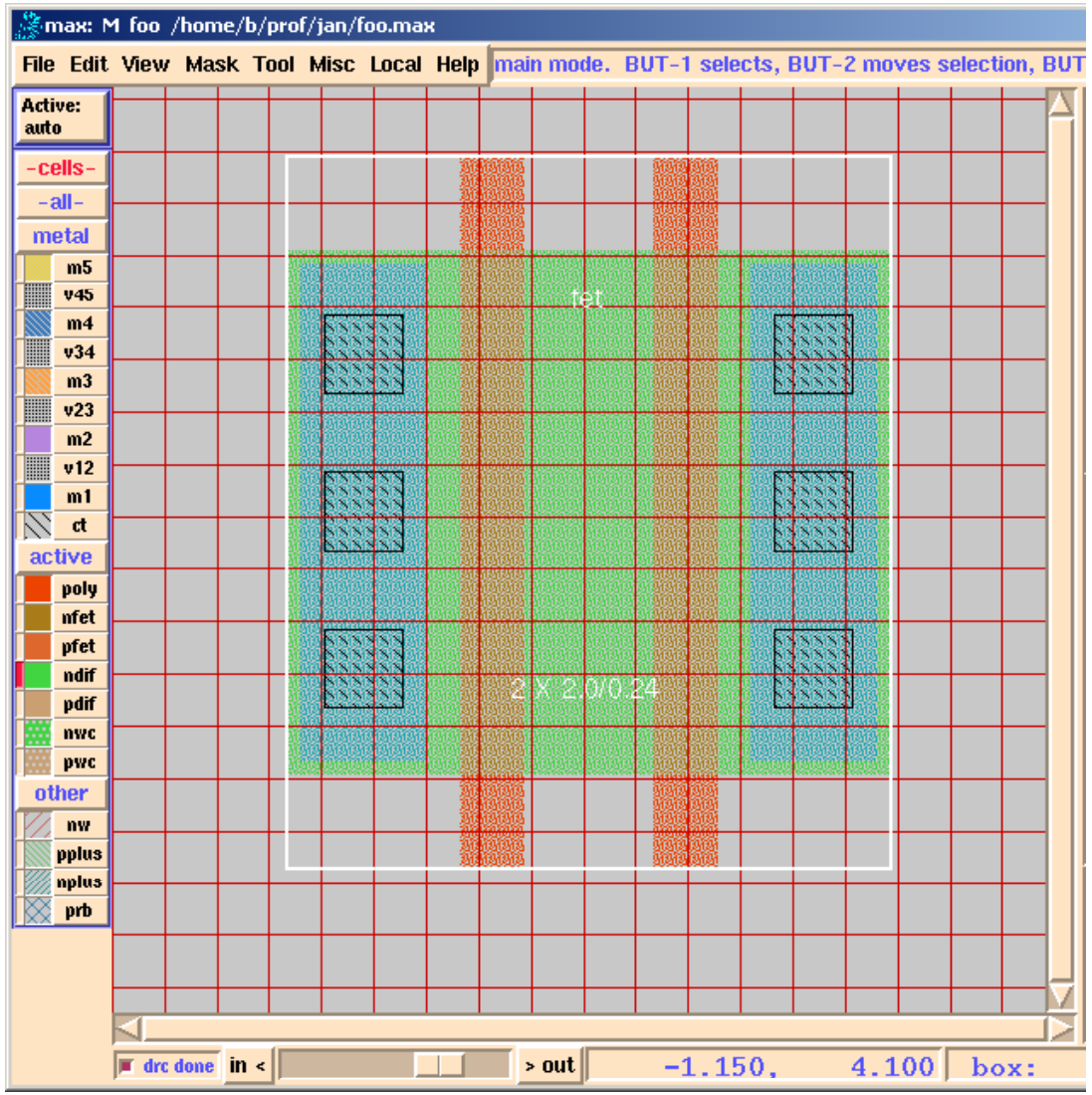
(a) Layout

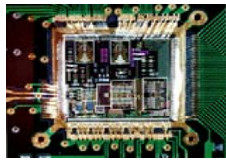


(b) Cross-Section along A-A'

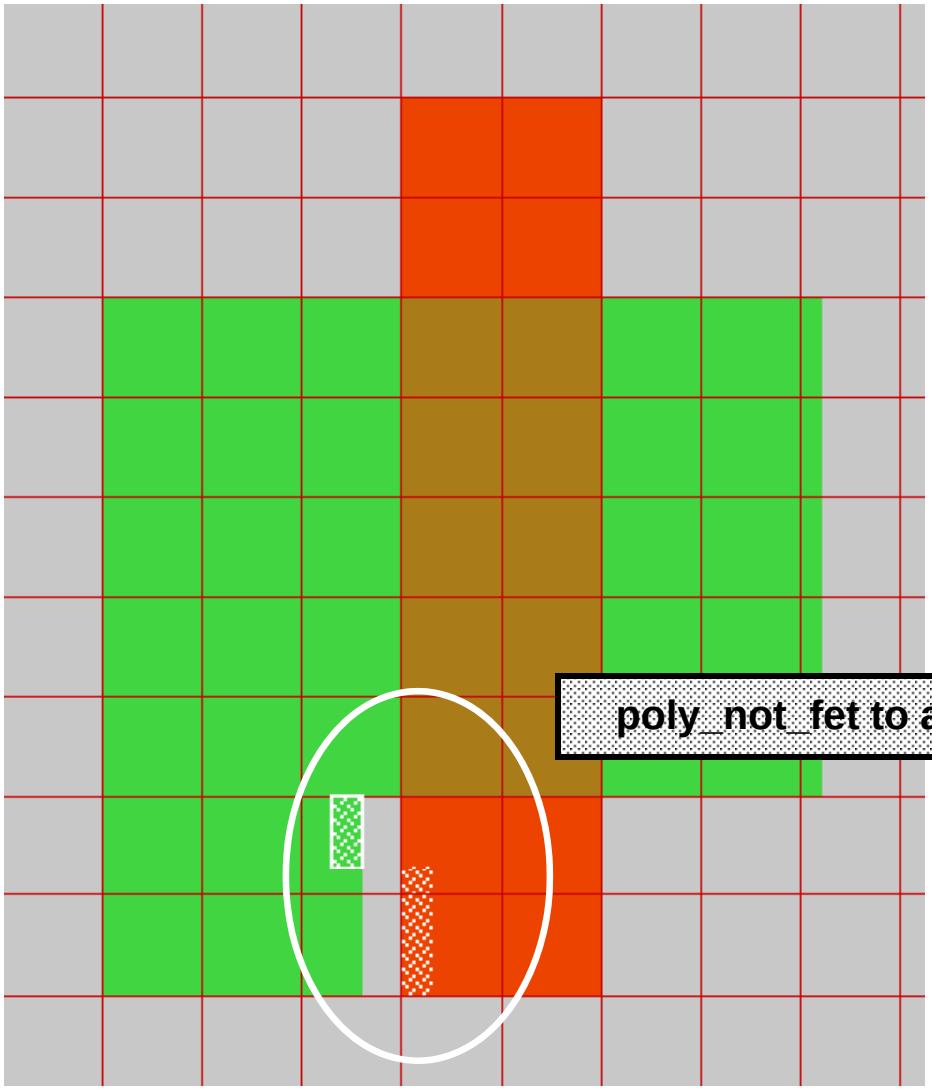


Layout Editor

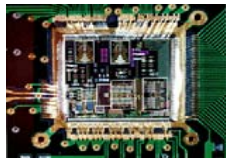




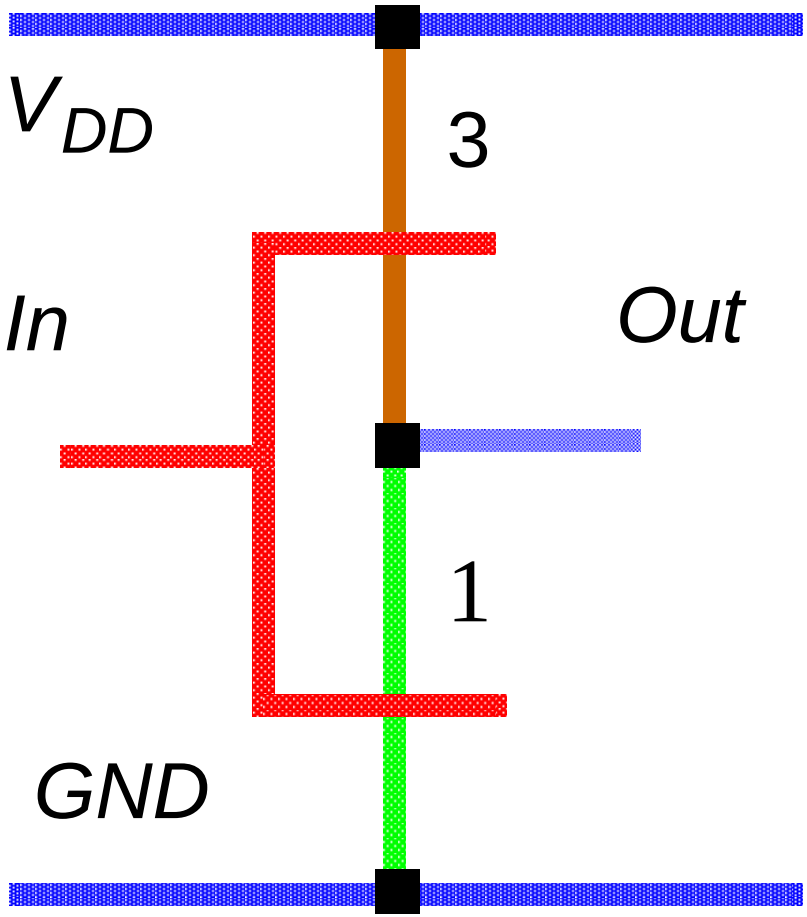
Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

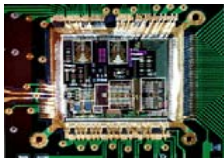


Sticks Diagram



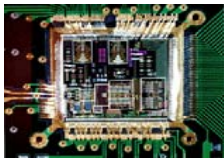
Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program



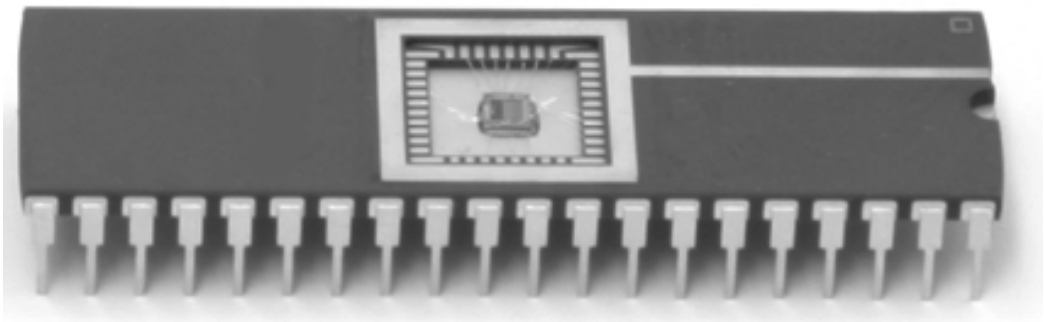
Logic Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts



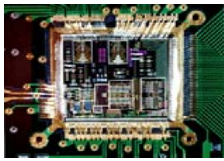
Packaging

- Tapeout final layout
- Fabrication
  - 6, 8, 12” wafers
  - Optimized for throughput, not latency (10 weeks!)
  - Cut into individual dice
- Packaging
  - Bond gold wires from die I/O pads to package



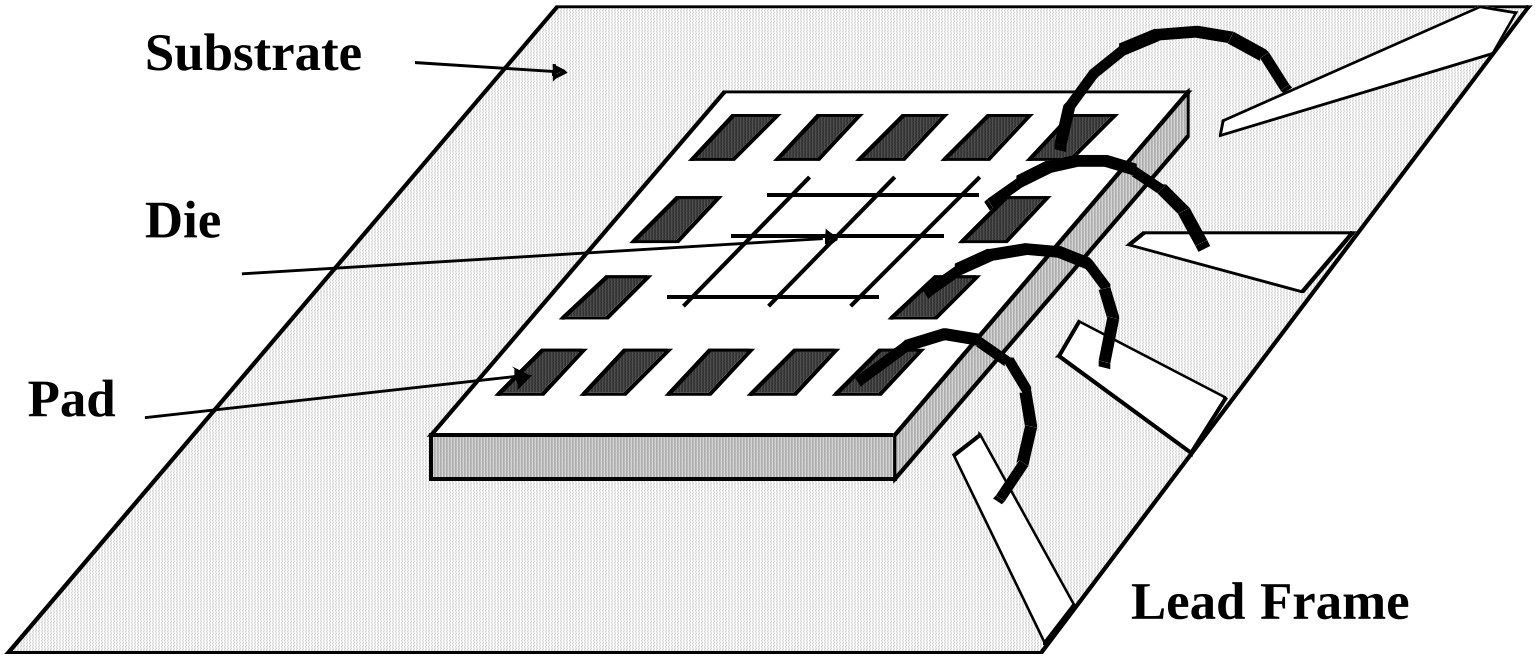
Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

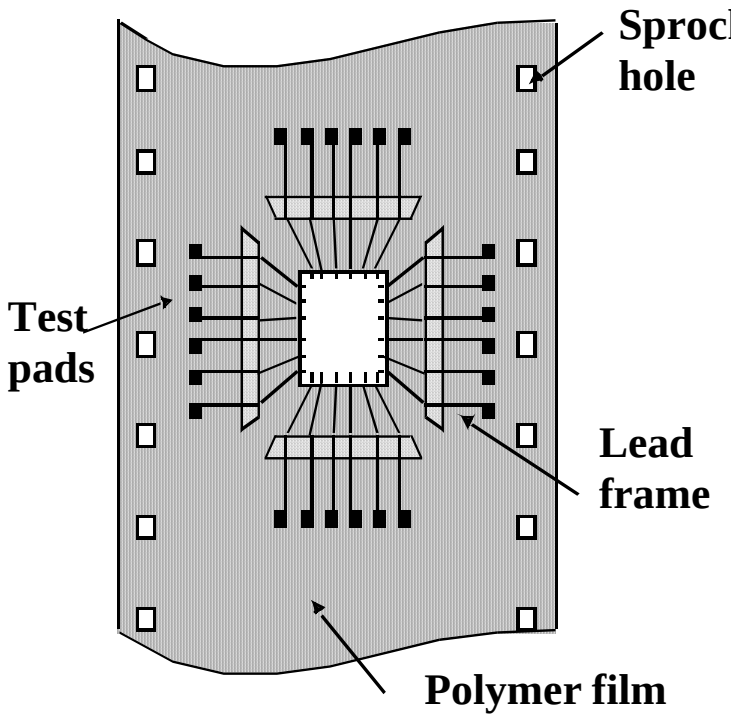


Bonding Techniques

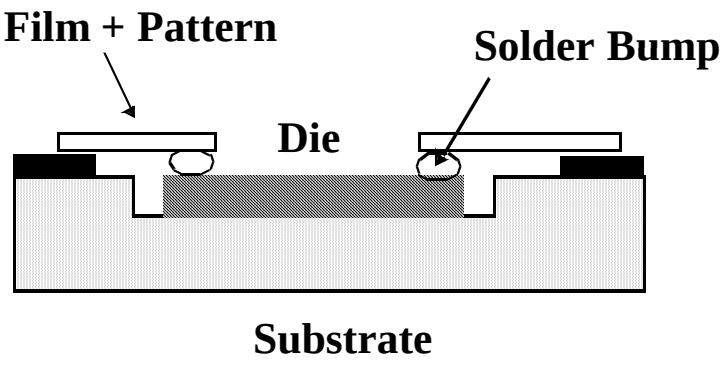
Wire Bonding



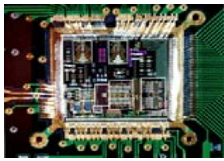
Tape-Automated Bonding (TAB)



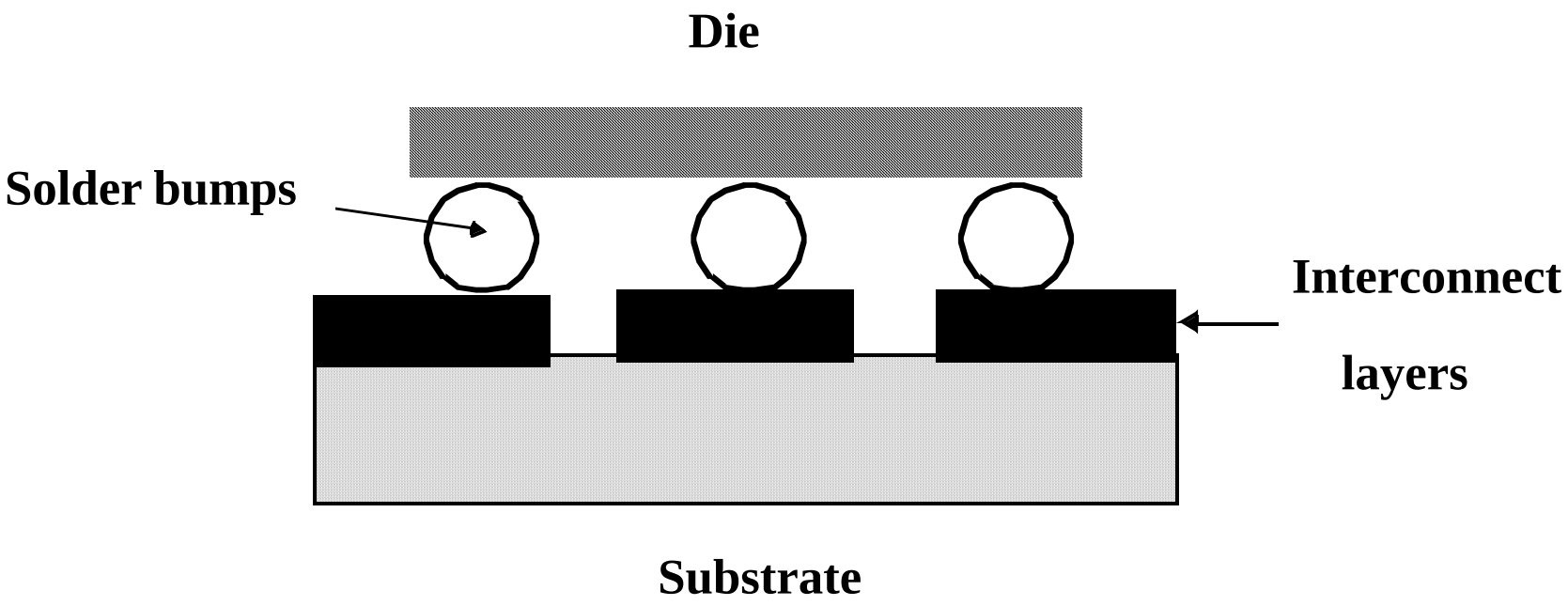
(a) Polymer Tape with imprinted wiring pattern.



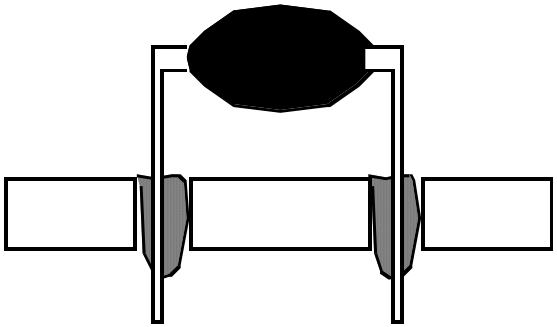
(b) Die attachment using solder bumps.



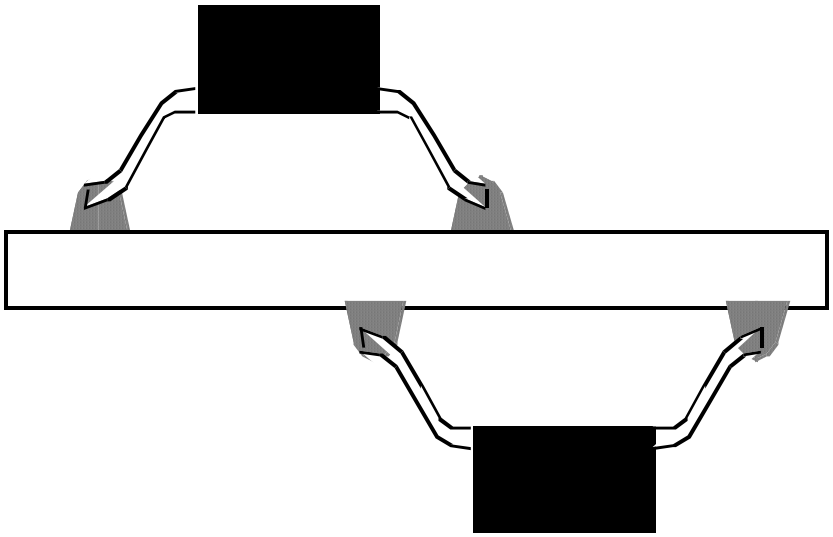
Flip-Chip Bonding



Package-to-Board Interconnect

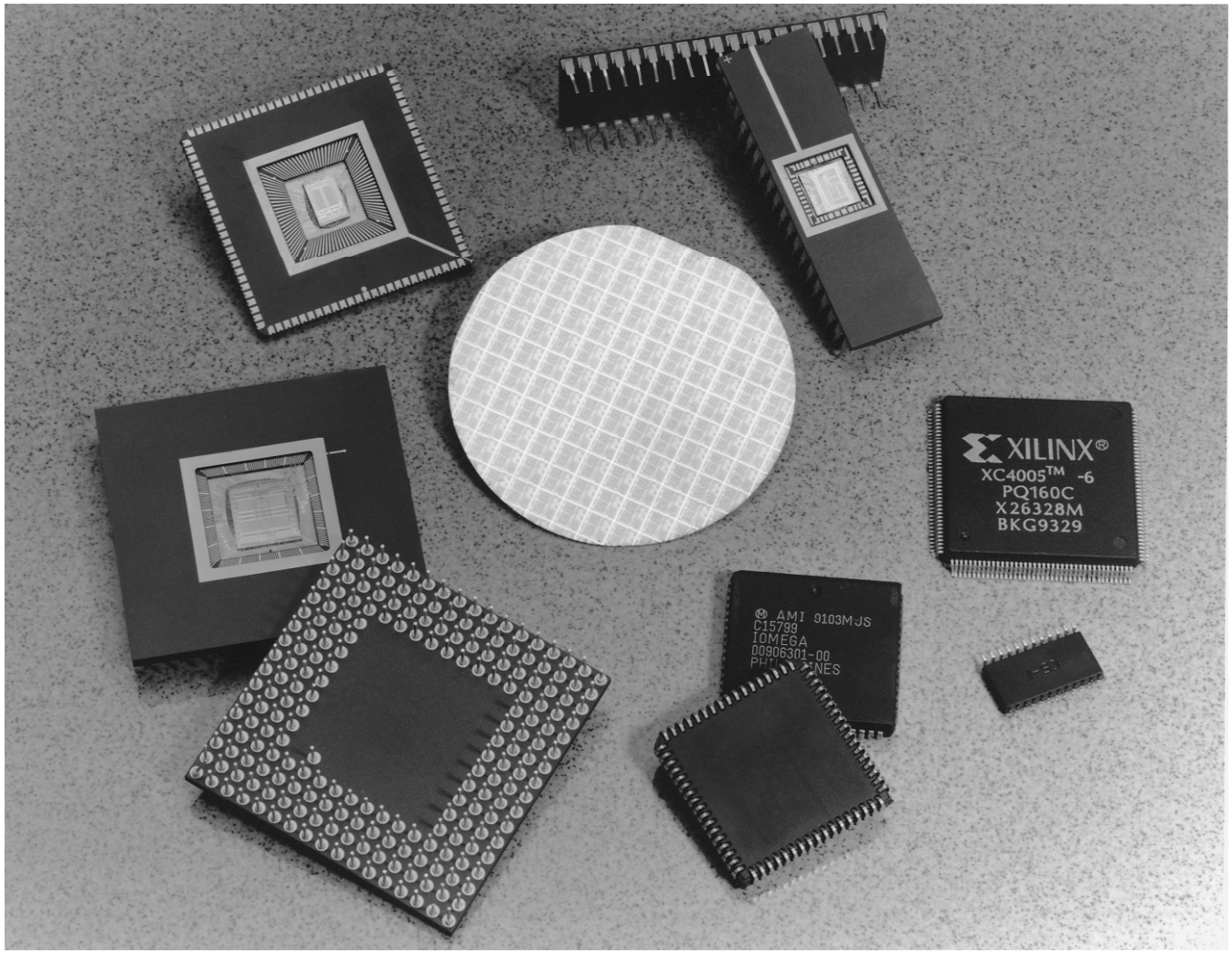


(a) Through-Hole Mounting



(b) Surface Mount

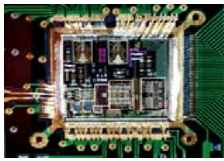
Package Types



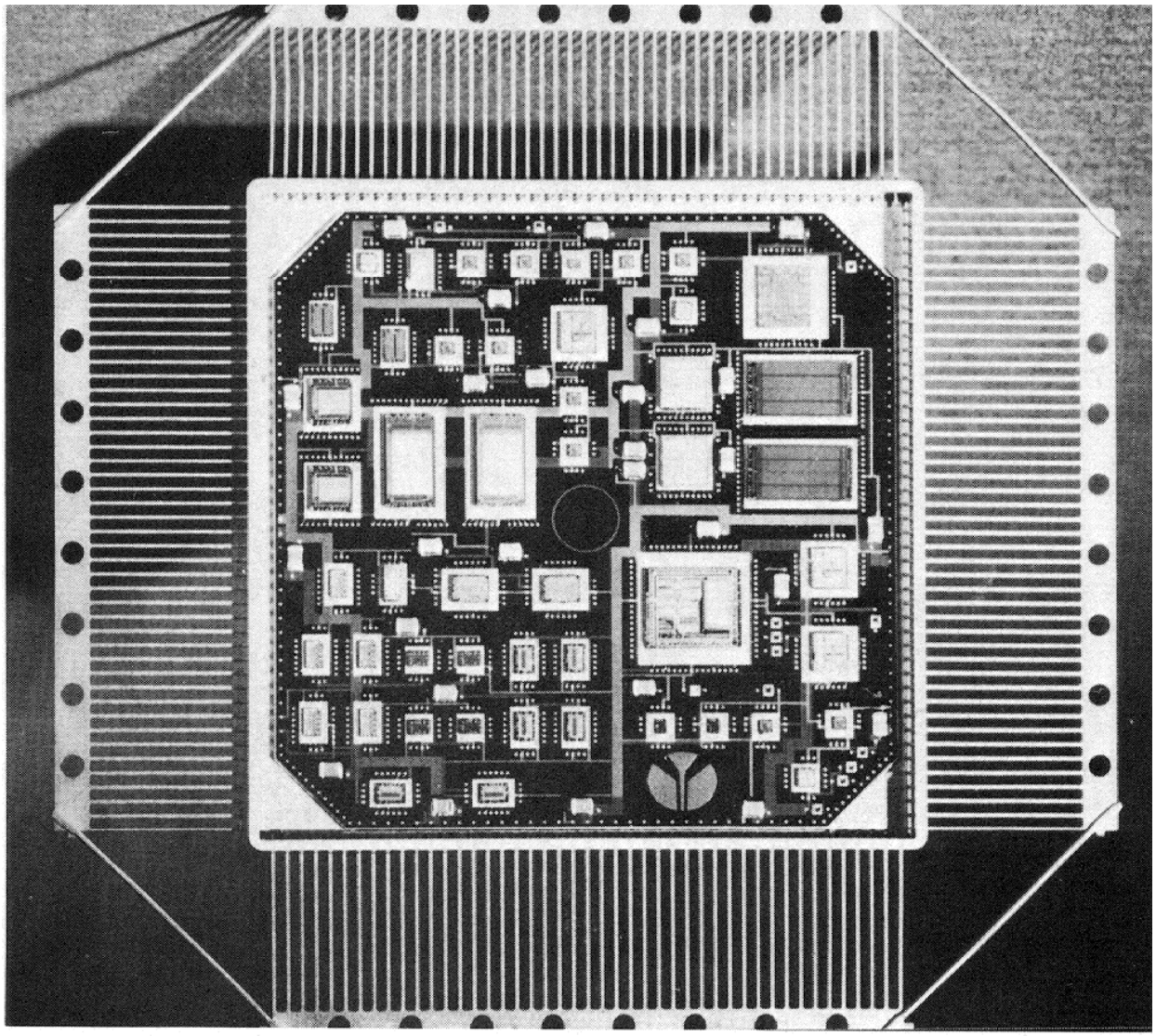
Package Parameters

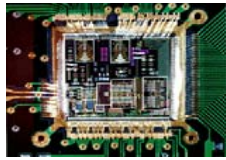
Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])



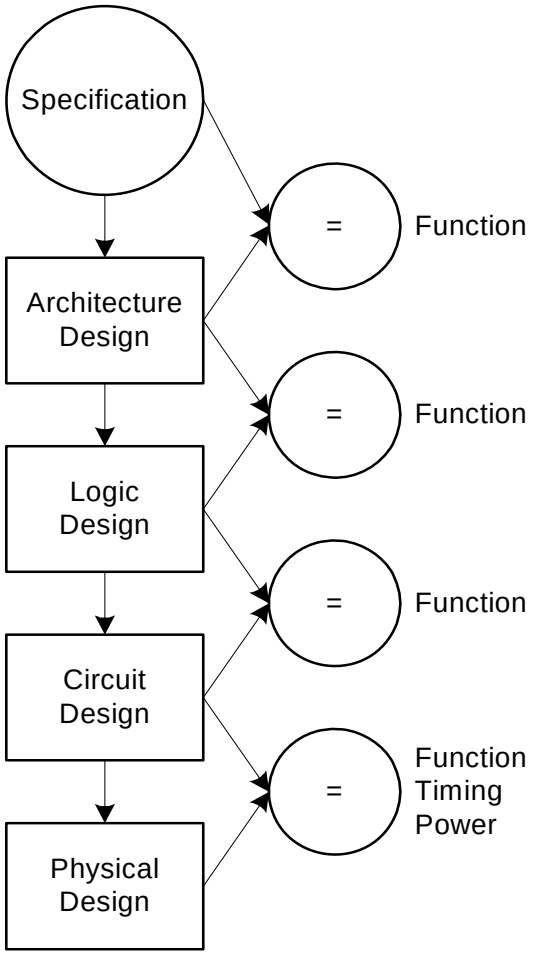
Multi-Chip Modules

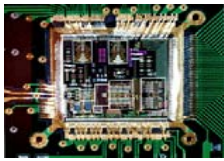




Design Verification

- Fabrication is slow & expensive
  - MOSIS 0.6μm: $1000, 3 months
  - State of art: $1M, 1 month
- Debugging chips is very hard
  - Limited visibility into operation
- Prove the design before building!
  - Logic simulation
  - Ckt. simulation / formal verification
  - Layout vs. schematic comparison
  - Design & electrical rule checks
- Verification is > 50% of effort on most chips!





Testing

- Test that chip operates
  - Design errors
  - Manufacturing errors
- A single dust particle or wafer defect kills a die
  - Yields from 90% to < 10%
  - Depends on die size, maturity of process
  - Test each part before shipping to customer