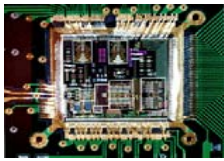
Lecture 1: Introduction

CSCE5610 Computer System Architecture
CSCE4610 Computer Architecture

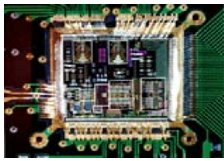
Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.



Things To Do

- Instructor's Introduction
- Student's Introduction
- Course Introduction

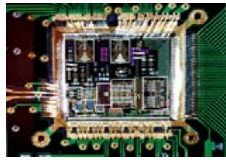


Class Time and Venue

- **Course Homepage:**
  http://www.cse.unt.edu/~smohanty/teaching/ComputerArchiSpring07/

- **Class Timing and Venue:**
  TuTh 4:00-5:20pm and NTRP B142

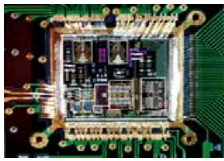
- **Instructor's Office:**
  Office Hours: MW 4:00-5:00pm (any other time possible by appointment through email)
  Room: NTRP F277
  Email: smohanty@cse.unt.edu
  Homepage URL: http://www.cse.unt.edu/~smohanty/



Course Syllabus and Description

Course objectives:

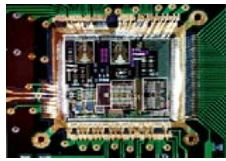
- Solid foundation in architecture of general purpose computers.
- Background to further study and research in architecture of modern computer systems.
- Idea of different approaches to designing a single CPU.
- Introduction to Instruction level parallelism, branch prediction techniques, various cache organization, multithreaded architectures, cache coherency and their impact on parallel processing.



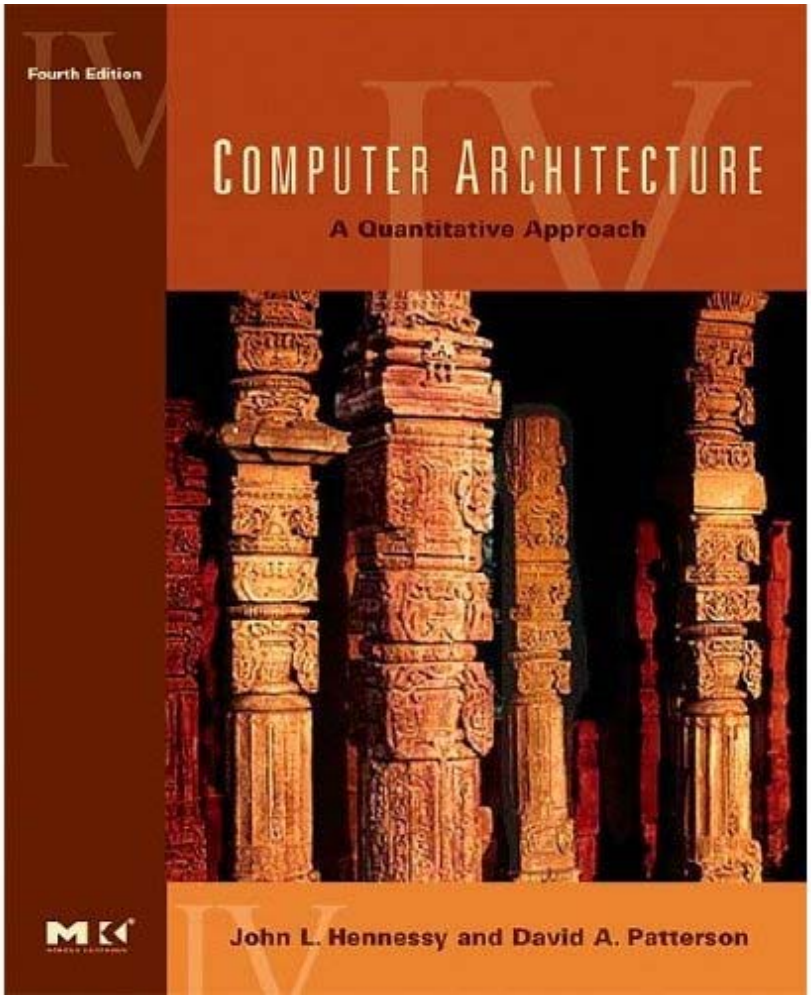
Course Syllabus and Description ….

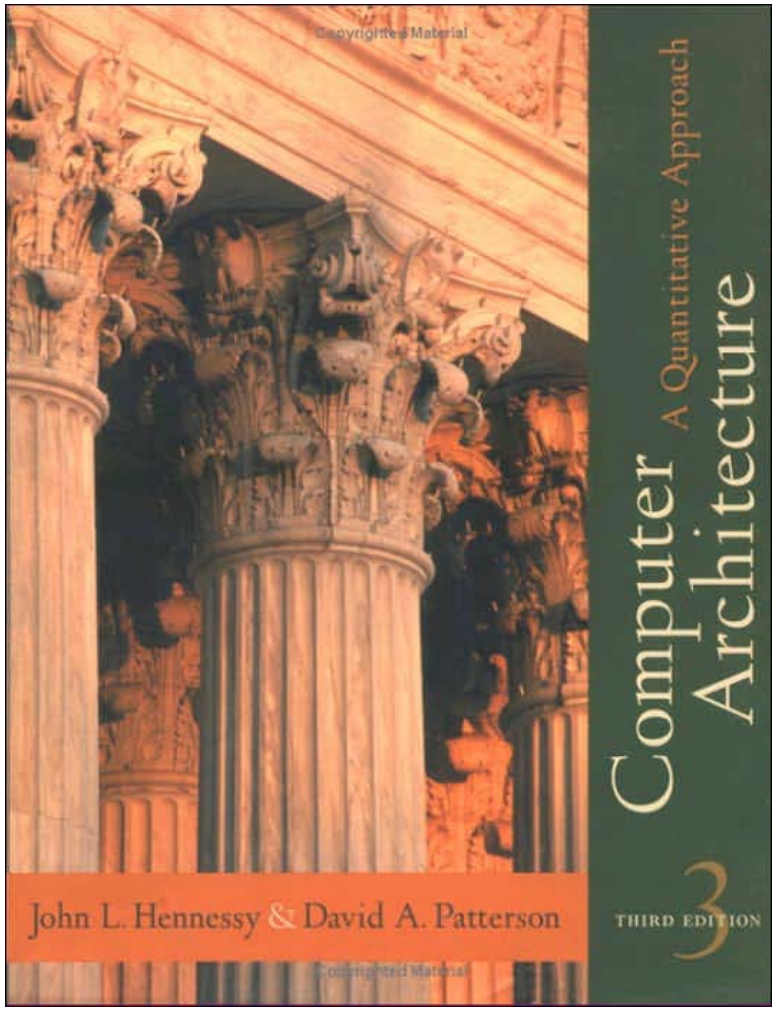
- **Prerequisites:** Computer Organization and Systems Programming.

- **Level of the Course:** The course is designed for first year graduate students or advanced undergraduate students.



Course Syllabus and Description ….



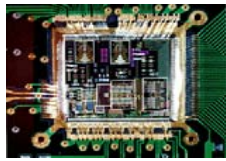


Text Book: Computer Architecture: A Quantitative Approach by J. Hennessy and D. Patterson, Morgan Kaufmann Publishing, 4th/3rd Edition.

Course Syllabus and Description ….

Selected Topics (Tentative):

- CPU design
- Instruction sets
- Control
- Processors
- ALU
- Memory and memory hierarchies
- Pipelined computers
- Multiprocessors
- Benchmarks to reveal and compare the performance of alternative design choices in system design
- Network-oriented interconnections



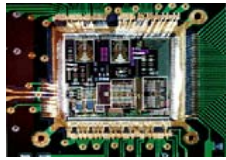
Course policy

- **Attendance for this course is mandatory** . In the case of absence due to unavoidable reasons, substantial documented evidence must be provided.

- Several **assignments** including exercise problems and design works will be given. The written or typed solutions for exercise problems and reports for design works must be submitted in the class **at the beginning of lecture** of the announced deadline, else **there will be late penalty of 20%** . Under no circumstances late assignment will be accepted two days after deadline and score for such assignment will be zero.

- Several surprise **quizzes** will be given in the class. There will be no make up quiz for any student under any circumstances.

- **There will be three tests of equal weightage.** There will be no final test. The tests will be approximately evenly spaced throughout the semester. The tests will be conducted in the same lecture room. The dates of the tests will be announced right on the 1st lecture, and the test dates will not be changed under any circumstances.



Course policy …..

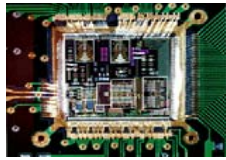
- Any makeup test will not be given unless substantial documented evidence is provided for a reasonable excuse of absence. In the absence of the documented evidence the score for the test will be zero.

- Any questions regarding the test grades should be clarified **a week of returning the test**. If no complaint is formulated within one week after the grades are posted on the course web page, **it will be considered that the student accepted the grade and the corresponding grades are considered definite** .

- No student shall be compelled to attend class or sit for a test on a day or time prohibited by his or her religious belief.

- Dishonesty in this class will be handled as per the University of North Texas policy (http://www.unt.edu/csrr).

- If a students needs any special accommodations according to the American Disability Act, he or she should let the instructor know.

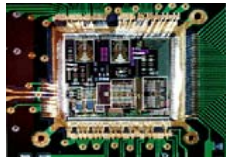


Tests Dates

Test No.	Date	% of Final Grade (for CSCE 5610)	% of Final Grade (for CSCE 4610)
Test 1	1st Mar (Thu)	15	20
Test 2	5th Apr (Thu)	15	20
Test 3	3rd May (Thu)	15	20

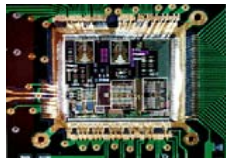
NOTE:

- Tests will be closed book and closed notes, and calculators are not allowed.
- Test dates will not be changes under any circumstances.



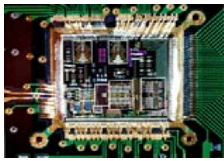
Grading Procedure

Items	% of Final Grade (for CSCE 5610)	% of Final Grade (for CSCE 4610)
Tests	45	60
Assignments	20	20
Quizzes	10	10
Project/Survey	15 (Abstract + Report + Presentation - 5+5+5) Deadlines: 1.Abstract: 3rd Apr (Tue) 2.Report: 1st May (Tue) 3.Presentation: 8th May (Tue) and 10th May (Thu)	**NA**
Discretion	10	10



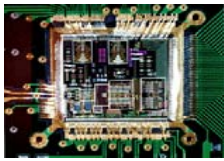
Assignments: Exercises

- Exercise problems from text book and other sources.



Projects

- All projects are individual projects.
- Any topic can be chosen by a student and can be assigned by instructor.
- Important: Start from the first day of class ☺



Survey

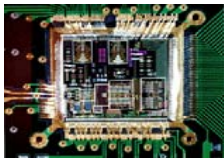
- Intended to make the student learn a particular area of current research.
- Needs to be done individually.
- Any topic can be chosen by a student and can be assigned by instructor.
- Important: Start from the first day of class ☺

Grading Policy

A >= 90
90 > B >= 80
80 > C >= 70
70 > D >= 60
60 > F

NOTE: (i) Grading policy may change if University or Dept. decide so.

(ii) There will be no border grade concessions.

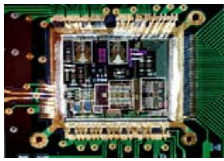


What is a digital Computer ?

A fast electronic machine that accepts digitized input information, processes it according to a list of internally stored instruction, and produces the resulting output information.

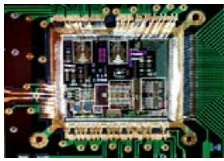
List of instructions → Computer program

Internal storage → Memory



Different Types and Forms of Computer

- Personal Computers (Desktop PCs)
- Notebook computers (Laptop computers)
- Handheld PCs
- Pocket PCs
- Workstations (SGI, HP, IBM, SUN)
- ATM (Embedded systems)
- Supercomputers



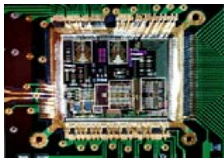
What is “Computer Architecture”?

Computer Architecture =

Instruction Set Architecture

+

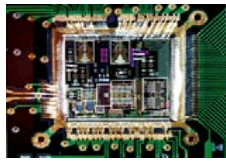
Machine Organization



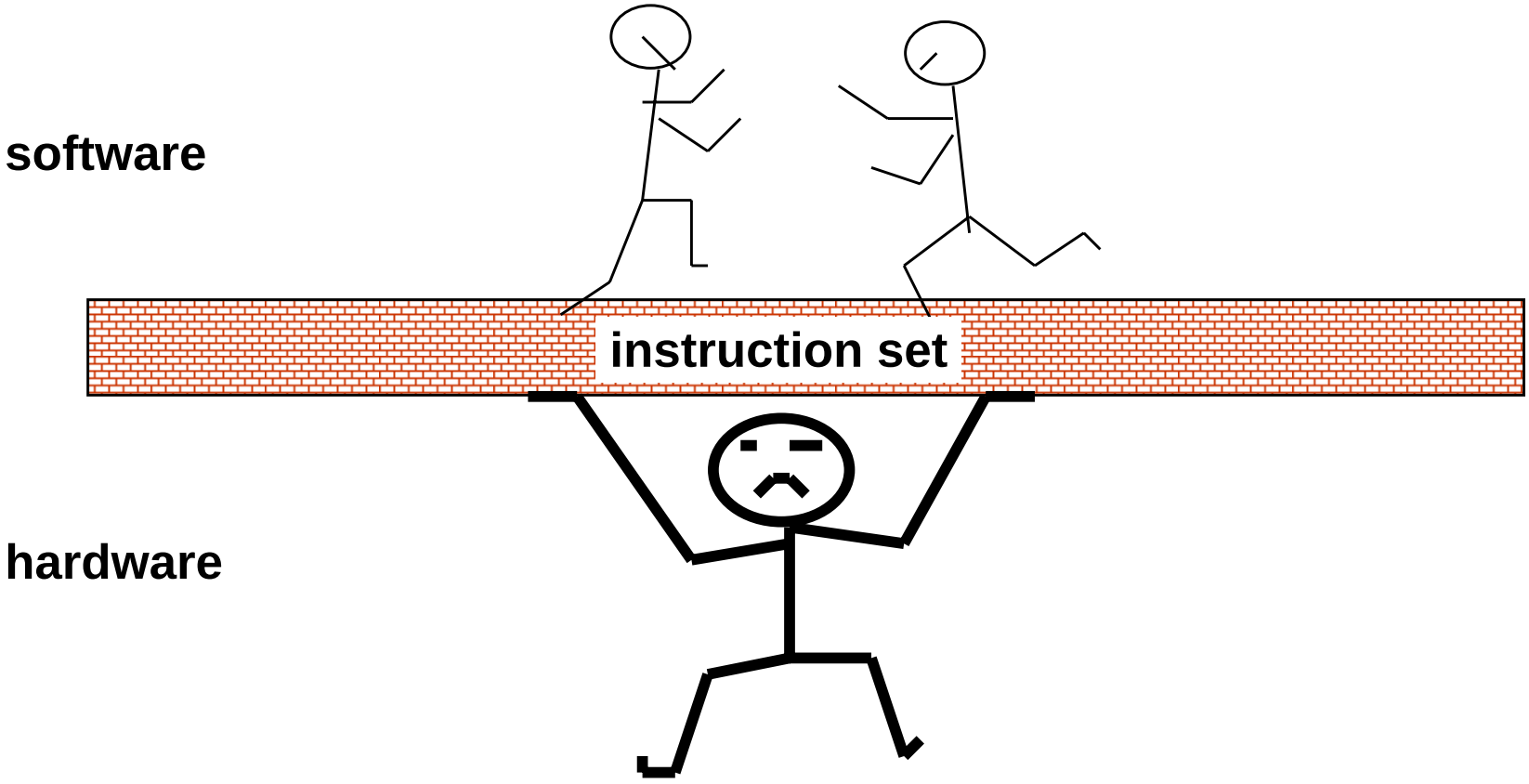
Instruction Set Architecture

... the attributes of a [computing] system as seen by the programmer, *i.e.* the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls the logic design, and the physical implementation. – Amdahl, Blaaw, and Brooks, 1964

- **Organization of Programmable Storage**
- **Data Types & Data Structures: Encodings & Representations**
- **Instruction Set**
- **Instruction Formats**
- **Modes of Addressing and Accessing Data Items and Instructions**
- **Exceptional Conditions**

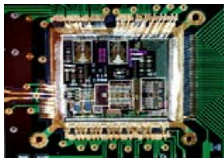


The Instruction Set: a Critical Interface



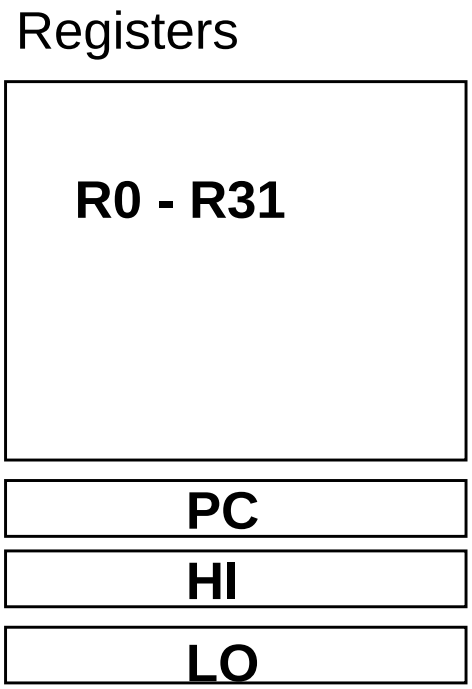
Example Instruction Set Architectures

- Digital Alpha (v1, v3) 1992-97
- HP PA-RISC (v1.1, v2.0) 1986-96
- Sun Sparc (v8, v9) 1987-95
- SGI MIPS (MIPS I, II, III, IV, V) 1986-96
- Intel (8086,80286,80386, 80486,Pentium, MMX, ...) 1978-96

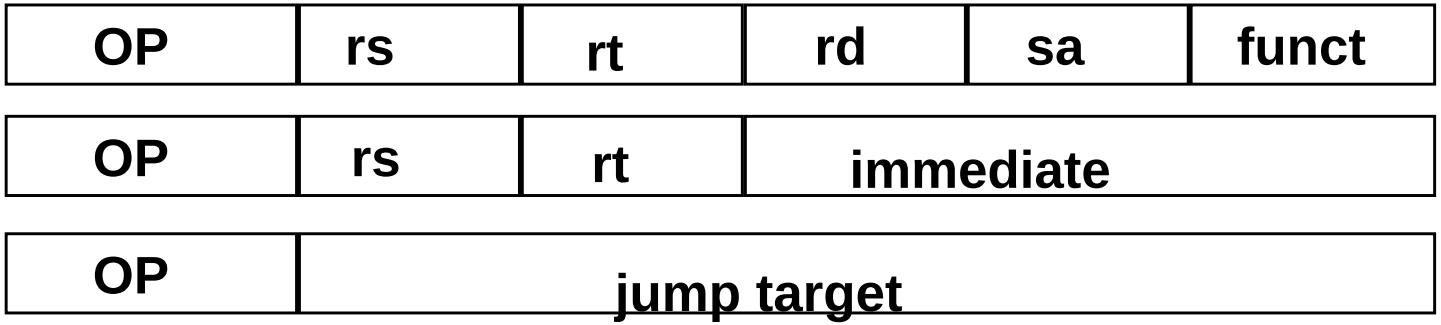


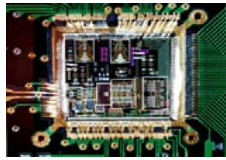
MIPS R3000 Instruction Set Architecture

- Instruction Categories
  - Load/Store
  - Computational
  - Jump and Branch
  - Floating Point
    - coprocessor
  - Memory Management
  - Special



3 Instruction Formats: all 32 bits wide





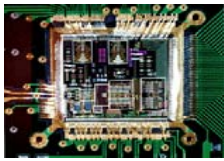
Computer Organization

- Capabilities & Performance Characteristics of Principal Functional Units
  - (e.g., Registers, ALU, Shifters, Logic Units, ...)
- Ways in which these components are interconnected
- Information flows between components
- Logic and means by which such information flow is controlled.
- Choreography of FUs to realize the ISA
- Register Transfer Level (RTL) Description

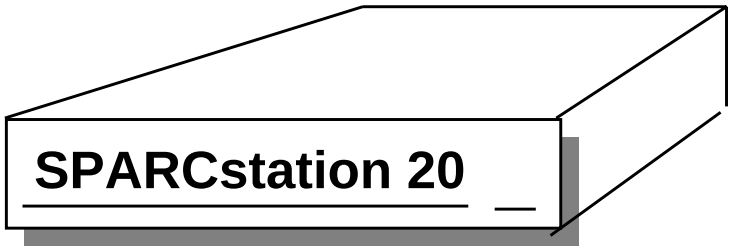
Logic Designer's View

ISA Level

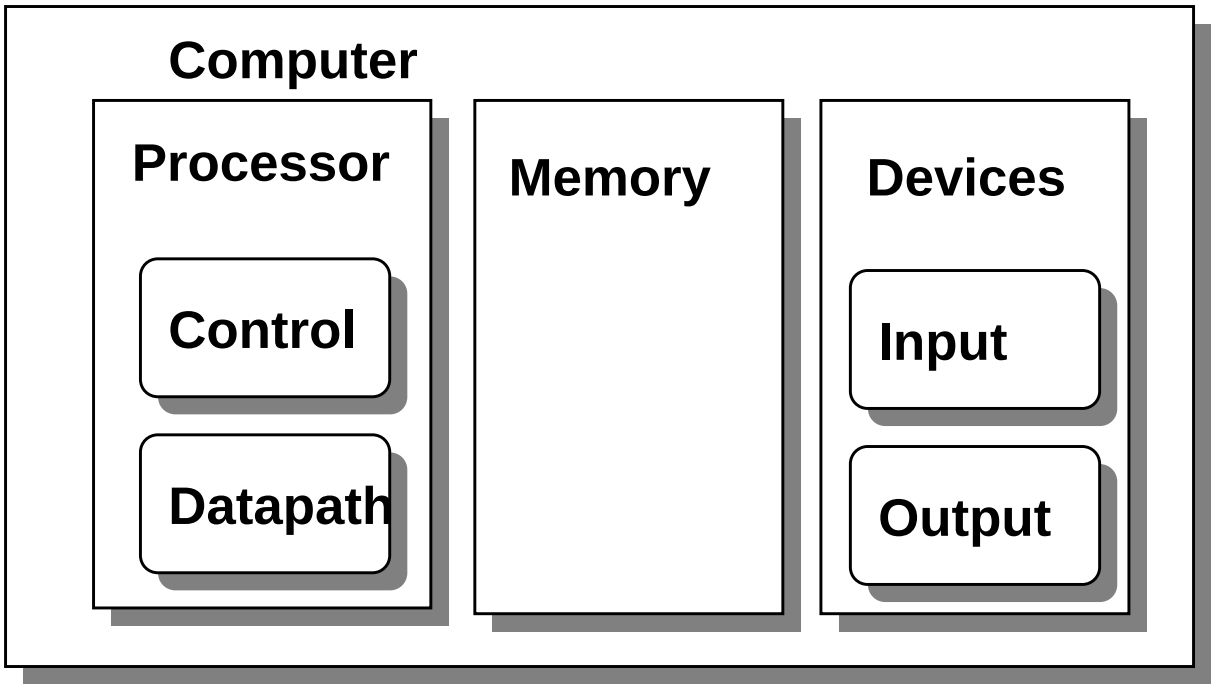
FUs & Interconnect



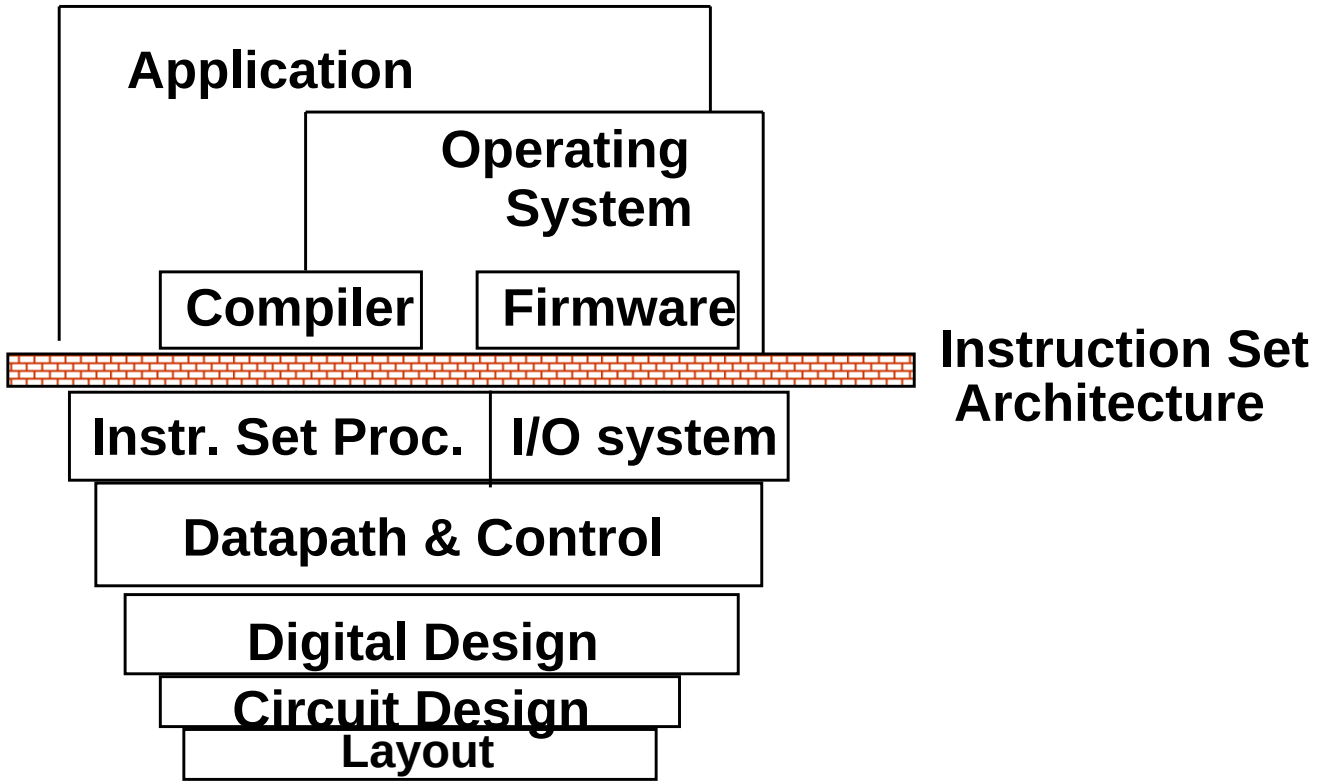
Levels of Organization



Workstation Design Target:
25% of cost on Processor
25% of cost on Memory (minimum memory size)
Rest on I/O devices, power supplies, box



What is “Computer Architecture”?

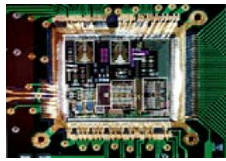


- Coordination of many *levels of abstraction*
- Under a rapidly changing set of forces
- Design, Measurement, *and* Evaluation

Computer Architecture and Engineering

Computer Architecture and Engineering

Instruction Set Design	Computer Organization
Interfaces	Hardware Components
Compiler/System View	Logic Designer's View
-"Building Architect"	-"Construction Engineer"

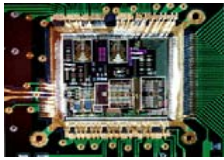


What is a microprocessor ?

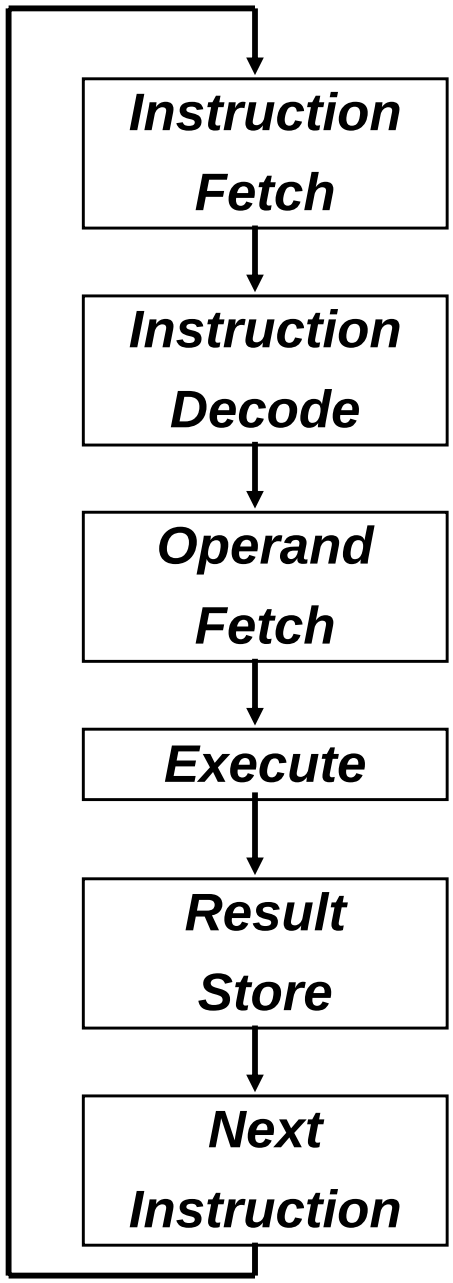
- **A microprocessor is an integrated circuit (IC) built on a tiny piece of silicon.** It contains thousands, or even millions, of transistors, which are interconnected via superfine traces of aluminum. The transistors work together to store and manipulate data so that the microprocessor can perform a wide variety of useful functions. The particular functions a microprocessor performs are dictated by software. (source : Intel)

- Simply speaking, microprocessor is the CPU on a single chip. CPU stands for “central processing unit” also known as processor.

- Processor can be “general purpose” or “special purpose”. A special purpose processor is also known as “application specific integrated circuit” (ASIC).



Execution Cycle



Obtain instruction from program storage

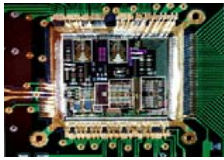
Determine required actions and instruction size

Locate and obtain operand data

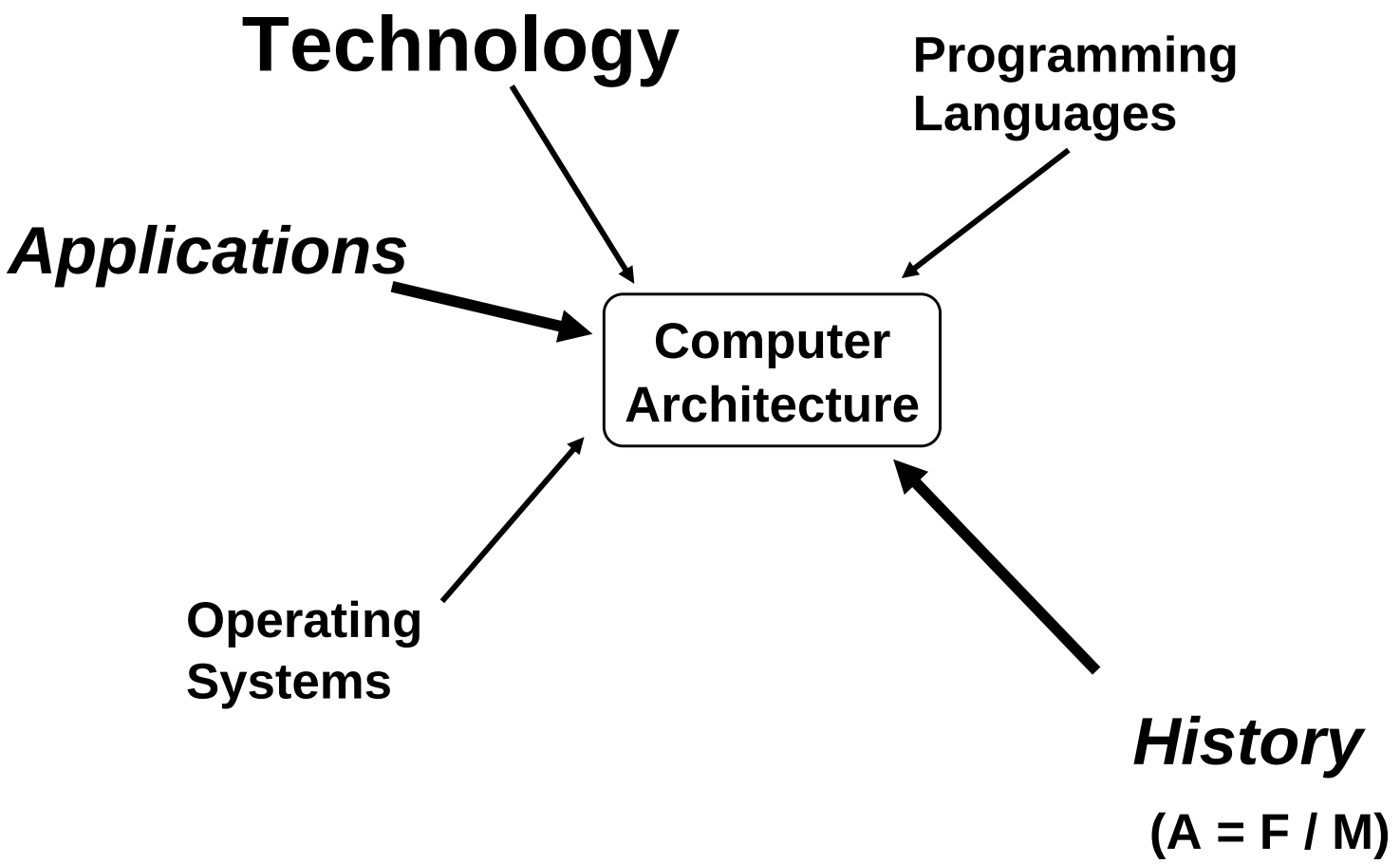
Compute result value or status

Deposit results in storage for later use

Determine successor instruction

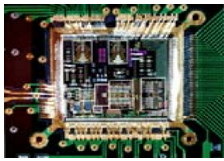


Forces on Computer Architecture



Technology => dramatic change

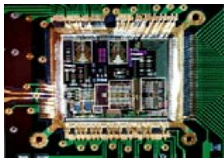
- Processor
  - logic capacity: about 30% per year
  - clock rate: about 20% per year
- Memory
  - DRAM capacity: about 60% per year (4x every 3 years)
  - Memory speed: about 10% per year
  - Cost per bit: improves about 25% per year
- Disk
  - capacity: about 60% per year



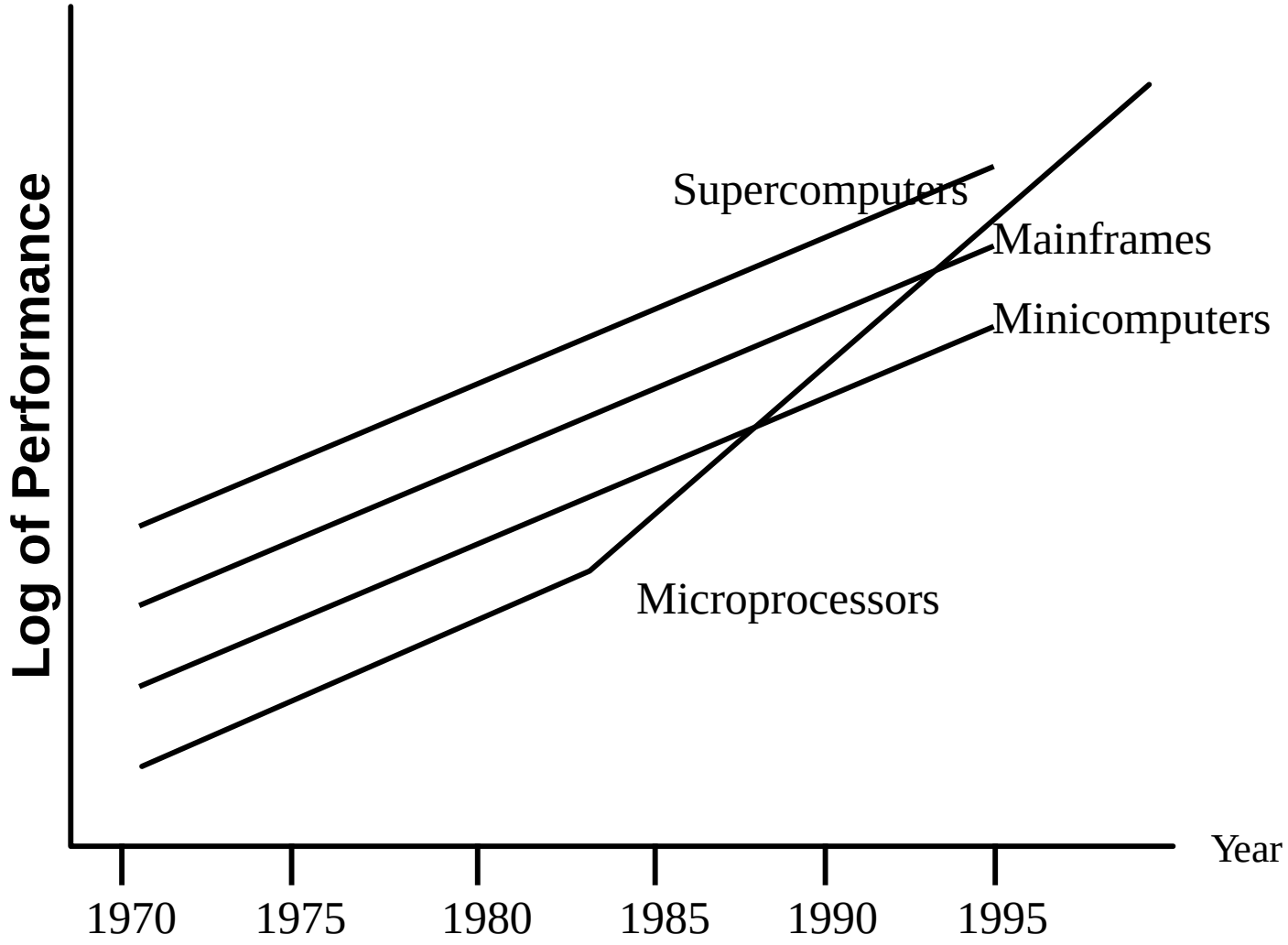
Moore's Law

- 1965: Gordon Moore plotted transistor on each chip
  - Transistor counts have doubled every 26 months

- Many other factors grow exponentially
  - clock frequency
  - processor performance

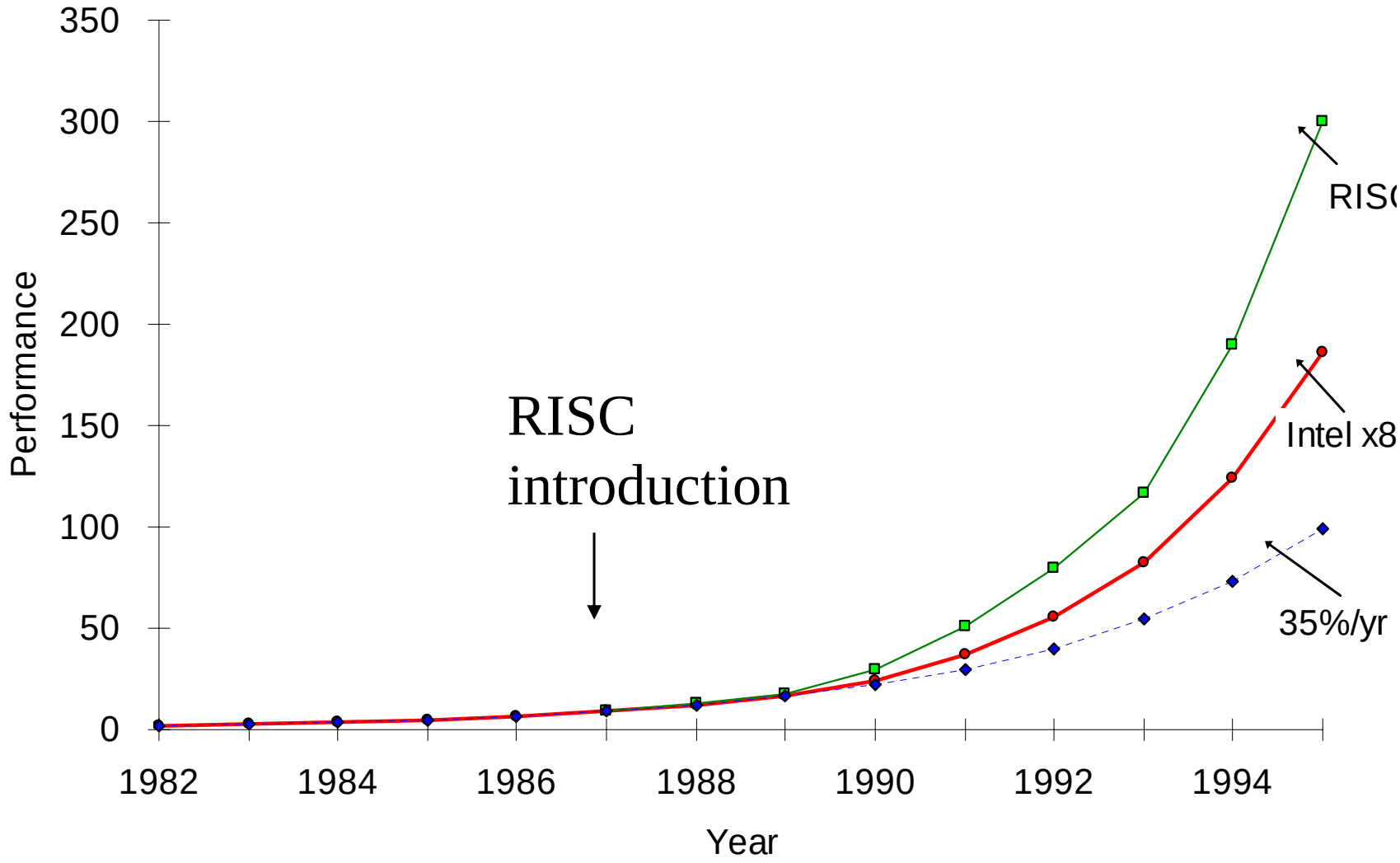


Performance Trends

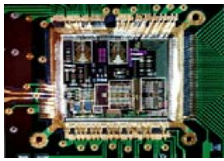


Processor Performance (SPEC)

performance now improves - 50% per year (2x every 1.5 years)

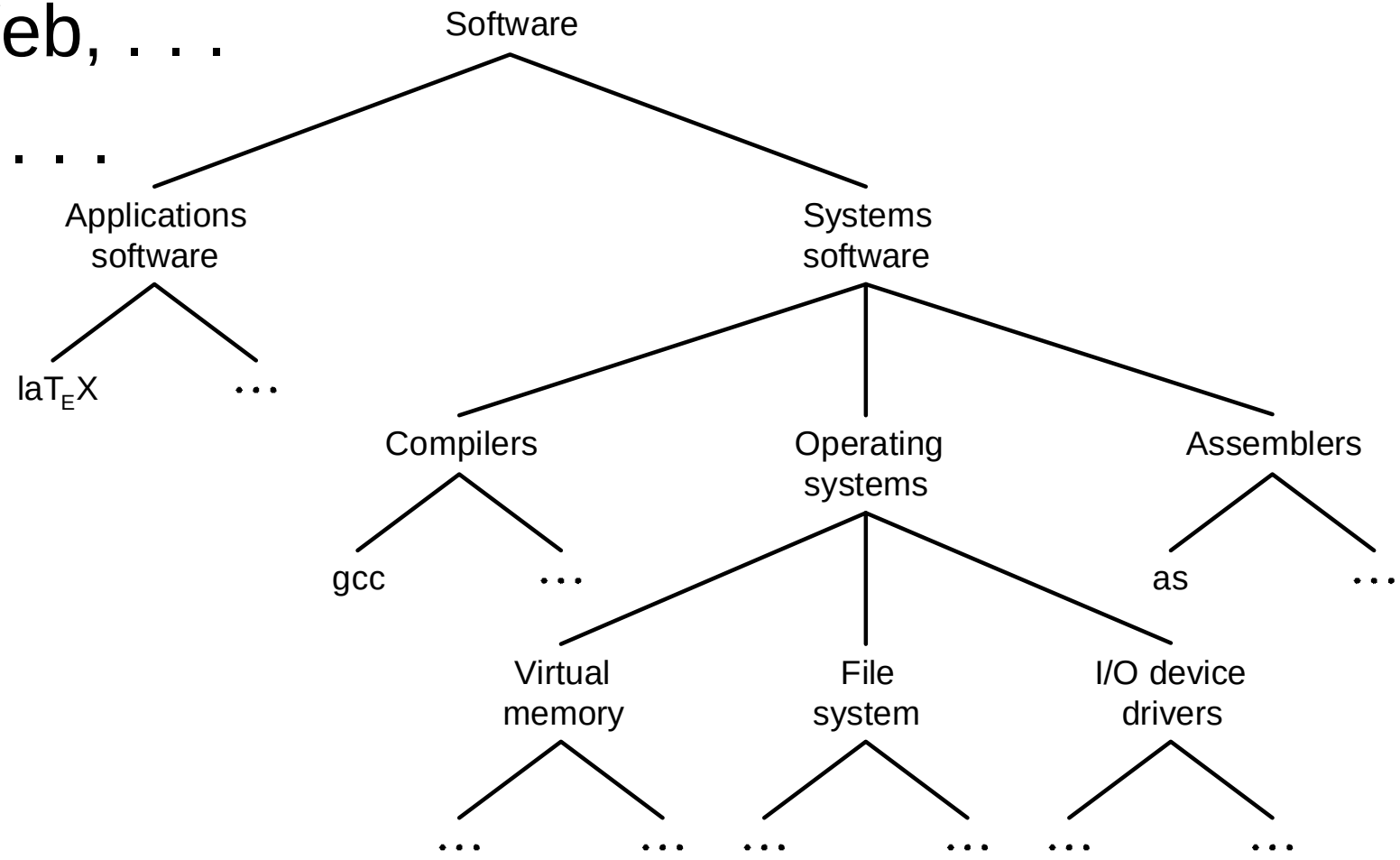


Did RISC win the technology battle and lose the market war?

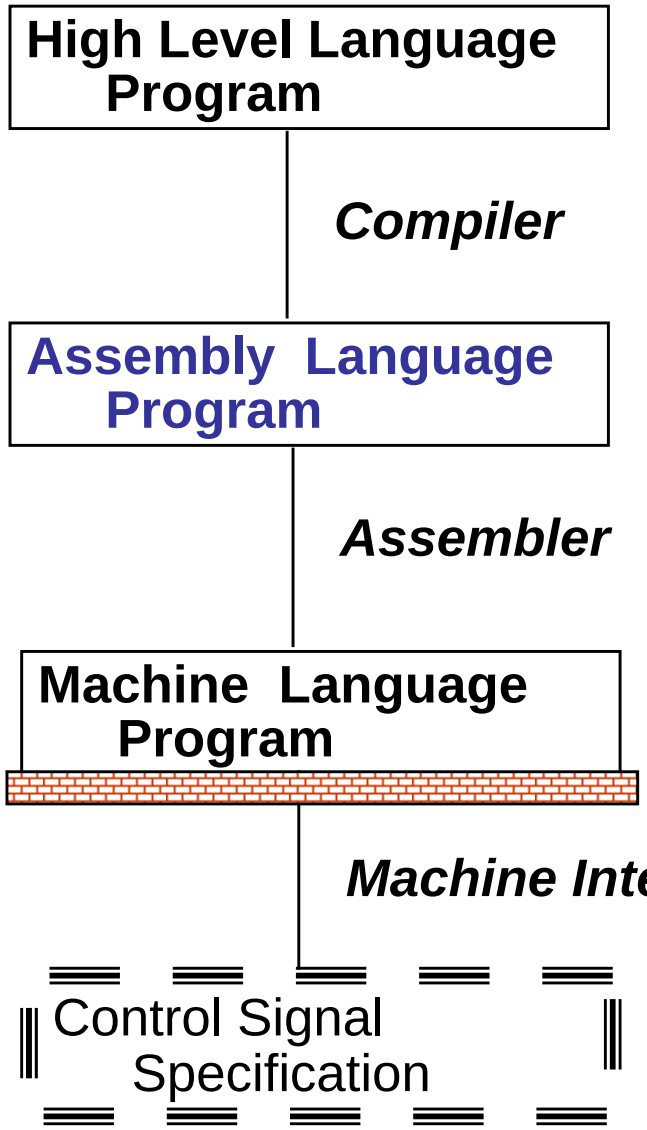


Applications and Languages

- CAD, CAM, CAE, . . .
- Multimedia, . . .
- The Web, . . .
- JAVA, . . .
- ???



Levels of Representation

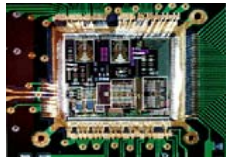



```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

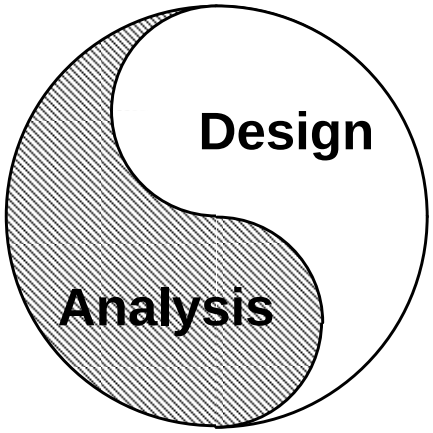
```
lw$15,0($2)
lw$16,4($2)
sw    $16,0($2)
sw    $15,4($2)
```

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

ALUOP[0:3] <= InstReg[9:11] & MASK



Measurement and Evaluation



Architecture is an iterative process
-- searching the space of possible designs
-- at all levels of computer systems