CSCE 5730: Digital CMOS VLSI Design

Assignment 4, Assigned Date: 11th Apr 2007 (Wed), Due Date: 18th Apr 2007 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Consider an aluminum wire of 15cm long and 1.5μm wide routed on the first aluminum layer. Compute the total capacitance by using the data presented in Table 4.2.

2. Consider the aluminum wire of above example, which is 15cm long and 1.5μm wide, is routed on the first aluminum layer. Assuming a sheet resistance for aluminum of 0.080 ohms/m, compute the total resistance of wire.

3. Compute the total propagation delay of a CMOS inverter for a generic 0.25mm CMOS process. For a supply voltage of 3V, the normalized "ON" resistance of NMOS and PMOS transistor equals 15Kohms and 50Kohms, respectively. The W:L ratios for NMOS is 1.5 and for PMOS is 4.5. The value of the load capacitance used is 5fF. Assume that the difference between the drawn and effective dimension is small enough to be ignorable.

4. Compute the energy needed to charge and discharge the capacitor of a CMOS inverter if C_L = 5fF for a supply voltage of 3V. Also, calculate the dynamic power dissipation of the circuit for a t_p of 30ps.