# CSCE 5730: Digital CMOS VLSI Design

Assignment # 1, Total Marks = 5*20 = 100.
Assigned Date: 4th Feb 2008 (Mon), Due Date: 13th Feb 2008 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Give a list of five journals in the area of VLSI, VLSI design automation. Provide their publishers name and also their homepage URL.
2. Give a list of five leading conferences in the area of VLSI, VLSI design automation. Provide their homepage URL and last two years venue.
3. Give a list of five free and/or commercial CAD tools.
4. Assume a wafer size of 16inches, a die size of 3.6$cm^2$, 1.3defects/$cm^2$, and $\alpha$=3. Determine the die yield of this CMOS process run.
5. Draw a cross-section of a MOS transistor. Explain its different materials and physical dimensions.